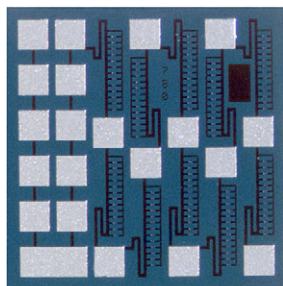


Wire Bondable Thin Film Multi-Tap Resistor Arrays



Product may not be to scale

The MTT multi-tap resistors offer nineteen taps allowing the user to select specified increments and a wide range of values. The desired resistance value is obtained by bonding the wires to the appropriate pads.

These chips are manufactured using Vishay Electro-Films (EFI) sophisticated Thin Film equipment and manufacturing technology. The MTT's are 100 % electrically tested and visually inspected to MIL-STD-883, method 2032 class H or K.

FEATURES

- Wire bondable
- Selectable values by wire bonding
- Resistance range: 1.1 k Ω to 275 k Ω
- Chip size: 0.038" x 0.038"
- Case: 0404
- Resistor material tantalum nitride, self-passivating
- Oxidized silicon substrate for good power dissipation
- Ideally suited for hybrid prototyping
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



APPLICATIONS

The MTT series of multi-tap resistor chips are designed to satisfy the requirements of prototype development and circuit trimming in hybrid packages through selective wire-bonding.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES, AND TOLERANCES

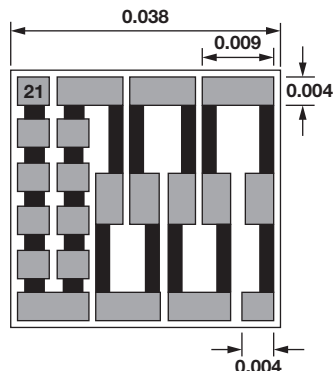
PARAMETER	VALUE	UNIT
Total Resistance Range	1.1K, 2.75K, 5.5K, 11K, 27.5K, 55K, 110K, 275K	Ω
10 Resistors Between Pads 1 and 11 10 Resistors Between Pads 11 and 21	Each 9.1 % of total resistance Each 0.91 % of total resistance	
Standard Tolerances	± 1 , ± 5 , ± 10 , ± 20 of total resistance of all 20 resistors	%
TCR	± 250	ppm/ $^{\circ}$ C

Example:

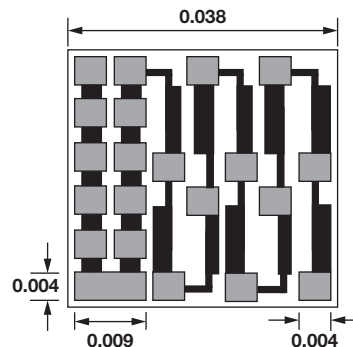
When the total resistance value is 55 k Ω , the resistors between pads 11 and 21 are 500 Ω each, and the resistors between pads 1 and 11 are 5 k Ω each.

STANDARD ELECTRICAL SPECIFICATIONS

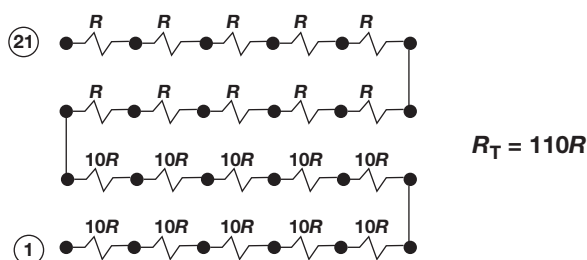
PARAMETER	VALUE	UNIT
TCR Tracking Between Elements	± 5	ppm/ $^{\circ}$ C
Noise, MIL-STD-202, Method 308	-30 typ.	dB
Moisture Resistance, MIL-STD-202, Method 106	± 0.5 max. $\Delta R/R$	%
Stability, 1000 h, +125 $^{\circ}$ C, 125 mW	± 0.5 max. $\Delta R/R$	%
Operating Temperature Range	-55 to +125	$^{\circ}$ C
Thermal Shock, MIL-STD-202, Method 107, Test Condition F	± 0.25 max. $\Delta R/R$	%
High Temperature Exposure +150 $^{\circ}$ C, 100 h	± 0.5 max. $\Delta R/R$	%
Dielectric Voltage Breakdown	200	V
Insulation Resistance	10^{12} min.	Ω
Operating Voltage	100 max.	V
DC Power Rating at +70 $^{\circ}$ C (Derated to Zero at +175 $^{\circ}$ C)	0.250, total R	W
5 x Rated Power Short-Time Overload, +25 $^{\circ}$ C, 5 s	± 0.25 max. $\Delta R/R$	%

DIMENSIONS in inches


TYPICAL RANGE
1.1 k Ω to 5.5 k Ω



TYPICAL RANGE
11 k Ω to 275 k Ω

SCHEMATIC


MECHANICAL SPECIFICATIONS	
PARAMETER	
Chip Size	0.038" x 0.038" $\pm$ 0.002" (0.965 mm x 0.965 mm $\pm$ 0.05 mm)
Chip Thickness	0.010" $\pm$ 0.002" (0.254 mm $\pm$ 0.05 mm)
Chip Substrate Material	Oxidized silicon, 10 k $\text{\AA}$ minimum SiO ₂
Resistor Material	Tantalum nitride, self-passivating
Bonding Pads	0.004" x 0.004" (0.10 mm x 0.10 mm)
Number of Pads	21
Pad Material	10 k $\text{\AA}$ minimum aluminum
Backing	None, lapped semiconductor silicon

GLOBAL PART NUMBER INFORMATION

Global Part Number: MTT11002KMANHWS

Global Part Number Description: MTT 110K 10 %, 250 ppm/°C, Al termination, no back metal, class H, WS

M

T

T

1

1

0

0

2

K

M

A

N

H

W

S

MODEL

RESISTANCE

RESISTANCE MULTIPLIER CODE

TOL. CODE (%)

TCR (ppm/°C)

TERMINATION

BACK METAL

VISUAL CLASS

PACKAGING CODE

MTT

First 4 digits are significant figures of resistance

A = 0.1

0 = 1

1 = 10

2 = 100

F = 1.0

G = 2.0

J = 5.0

K = 10

M = 20

L = 25

C = ± 50

K = ± 100

M = ± 250

R = 0 / -250

G = gold

A = aluminum

G = gold

N = none

H = class H

K = class K

WS = waffle pack

100 min,

1 mult.

Historical Part Number: WMTT00210002K (will continue to be accepted)



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