

Product Overview

NSi6602 is a family of high reliability isolated dual-channel gate driver ICs which can be designed to drive power transistor up to 2MHz switching frequency. Each output could source 4A and sink 6A peak current with fast 25ns propagation delay and 5ns maximum delay matching.

The NSi6602 provides 3000Vrms isolation in SOP16 (150mil) package, and 5700Vrms isolation in SOP16 (300mil) or SOP14 (300mil) package. System robustness is supported by 150kV/us typical common-mode transient immunity (CMTI).

The driver operates with a maximum supply voltage of 25V, while the input-side accepts from 2.7V to 5V supply voltage. Under voltage lock-out (UVLO) protection is supported by all the power supply voltage pins.

Key Features

- Isolated dual channel driver
- Input side supply voltage: 2.7V to 5.5V
- Driver side supply voltage: up to 25V with UVLO
- 4A peak source and 6A peak sink output
- High CMTI: $\pm 150\text{kV/us}$ typical
- 25ns typical propagation delay
- 5ns maximum delay matching
- 6ns maximum pulse width distortion
- Programmable deadtime
- Accepts minimum input pulse width 20ns
- Operation temperature: $-40^{\circ}\text{C} \sim 125^{\circ}\text{C}$
- AEC-Q100 (Grade 1) qualified for auto-motive application

Safety Regulatory Approvals

- UL recognition:
 - SOP16/SOP14(300mil): 5700V_{rms} for 1 minute per UL1577
 - SOP16(150mil): 3000V_{rms} for 1 minute per UL1577
- DIN VDE V 0884-11:2017-01
- CSA component notice 5A
- CQC certification per GB4943.1-2011

Applications

- Isolated DC-DC and AC-to-DC power supplies in server, telecom, and industry
- DC-to-AC solar inverters
- Motor drives and EV charging
- UPS and battery chargers

Functional Block Diagram

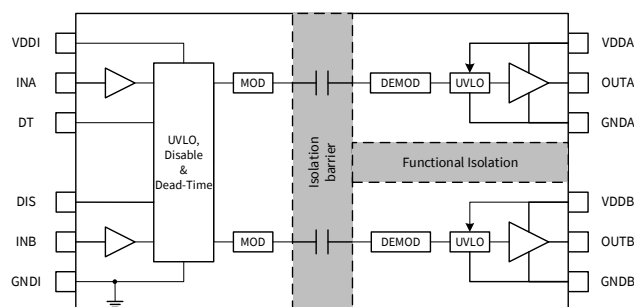


Figure 0.1 NSi6602 Block Diagram

INDEX

1. PIN CONFIGURATION AND FUNCTIONS	3
2. ABSOLUTE MAXIMUM RATINGS	4
3. RECOMMENDED OPERATING CONDITIONS	5
4. THERMAL INFORMATION	5
5. SPECIFICATIONS	6
5.1. ELECTRICAL CHARACTERISTICS.....	6
5.2. SWITCHING CHARACTERISTICS	7
5.3. TYPICAL PERFORMANCE CHARACTERISTICS	8
5.4. PARAMETER MEASUREMENT INFORMATION	12
6. HIGH VOLTAGE FEATURE DESCRIPTION	14
6.1. INSULATION CHARACTERISTICS	14
6.2. SAFETY-LIMITING VALUES	15
6.3. SAFETY-RELATED CERTIFICATIONS.....	17
7. FUNCTION DESCRIPTION	18
7.1. OVERVIEW.....	18
7.2. UNDER VOLTAGE LOCK OUT (UVLO)	18
7.3. INPUT AND OUTPUT LOGIC TABLE	19
7.4. PROGRAMMABLE DEADTIME (DT PIN)	19
7.4.1. PULLING THE DT PIN TO VDDI	19
7.4.2. DT PIN LEFT OPEN OR CONNECTED TO A PROGRAMMING RESISTOR BETWEEN DT AND GND PINS	19
7.5. ESD PROTECTION.....	20
8. APPLICATION NOTE	21
8.1. TYPICAL APPLICATION CIRCUIT	21
8.2. PCB LAYOUT	21
9. PACKAGE INFORMATION	22
10. ORDERING INFORMATION	26
11. TAPE AND REEL INFORMATION	27
12. REVISION HISTORY	28

1. Pin Configuration and Functions

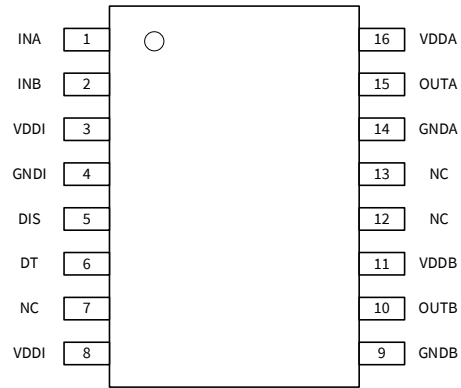


Figure 1.1 NSi6602 SOW16/SOP16 Package

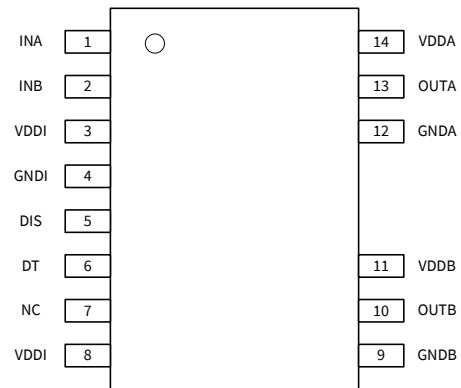


Figure 1.2 NSi6602 SOW14 Package

Table 1.1 NSi6602 Pin Configuration and Description

PIN NO.		SYMBOL	FUNCTION
SOP16	SOP14		
4	4	GND	Input-side ground reference.
1	1	INA	TTL/CMOS compatible input signal for channel A with internal pull down to GND. It is recommended to connect this pin to GND if not used.
2	2	INB	TTL/CMOS compatible input signal for channel B with internal pull down to GND. It is recommended to connect this pin to GND if not used.
3, 8	3, 8	VDDI	Input-side supply voltage. It is recommended to place a bypass capacitor from this pin to GND as close as possible.
5	5	DISABLE	Disables the isolator inputs and driver outputs if asserted high, enables if asserted low or left open. It is recommended to connect this pin to GND if not used.
6	6	DT	Programmable deadtime control. To allow the outputs overlapping by connecting DT to VDDI. Place a 1kΩ to 200kΩ resistor (R_{DT}) between DT and GND to adjust deadtime following: $t_{DT} (ns) = 10 \times R_{DT} (k\Omega)$. It is recommended to parallel a low ESR capacitor, e.g., 2.2nF or above.
9	9	GNDB	Ground for output channel B
10	10	OUTB	Output gate driver for channel B
11	11	Vddb	Supply voltage for channel B
14	12	GNDA	Ground for output channel A
15	13	OUTA	Output gate driver for channel A
16	14	VDDA	Supply voltage for channel A
7,12 ¹⁾ ,13	7	NC	Not connected

1) For SOP16(150mil) package, Pin 12 has been connected to GNDB. Suggest not to connect Pin12 with other nets.

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit
Input Side Supply Voltage	VDDI to GNDI	-0.3	6	V
Output Side Supply Voltage	VDDA to GNDA, Vddb to GNDB	-0.3	30	V
Input Signal Voltage	INA, INB, DIS, DT to GNDI	-0.3	$V_{VDDI}+0.3$	V
	INA, INB, DIS, DT to GNDI, Transient for 50ns	-5	$V_{VDDI}+0.3$	V
Output Signal Voltage	OUTA to GNDA, OUTB to GNDB	-0.3	$V_{VDDA}+0.3$ $V_{Vddb}+0.3$	V
	OUTA to GNDA, OUTB to GNDB, Transient for 200ns	-2	$V_{VDDA}+0.3$	V

Parameters	Symbol	Min	Max	Unit
			V _{VDDB} +0.3	
Channel A to Channel B Voltage	GND A to GND B in SOP16&SOW16 package		1500	V
	GND A to GND B in SOW14 package		1850	V
Junction Temperature	T _J	-40	150	°C
Storage Temperature	T _{stg}	-65	150	°C
Electrostatic discharge	HBM (all pins)	-4000	4000	V
	CDM	-1500	1500	V

3. Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit
Input Side Supply Voltage	VDDI to GNDI	3	5.5	V
Driver Side Supply Voltage	VDDA to GND A, VDD B to GND B (NSi6602A)	7	25	V
	VDDA to GND A, VDD B to GND B (NSi6602B)	9.4	25	V
	VDDA to GND A, VDD B to GND B (NSi6602C)	14.2	25	V
Input Signal Voltage	INA, INB, DIS, DT	0	V _{VDDI}	V
Junction Temperature	T _J	-40	150	°C
Ambient Temperature	T _a	-40	125	°C

4. Thermal Information

Parameters	Symbol	SOW16/SOW14	SOP16	Unit
Junction-to-ambient thermal resistance ¹⁾	R _{JA}	97.0	150.5	°C/W
Junction-to-case(top) thermal resistance ²⁾	R _{JC (top)}	23.3	21.2	°C/W
Junction-to-top characterization parameter ³⁾	Ψ _{JT}	35.8	52.3	°C/W
Junction-to-board characterization parameter ³⁾	Ψ _{JB}	39.0	55.6	°C/W

- 1) Standard JESD51-3 Low Effective Thermal Conductivity Test Board (1s) in an environment described in JESD51-2a.
- 2) Standard JESD51-3 Low Effective Thermal Conductivity Test Board (1s) by transient dual interface test method described in JESD51-14.
- 3) Obtained by Simulating in an environment described in JESD51-2a.

5. Specifications

5.1. Electrical Characteristics

VDDI=3.3V or 5V, VDDA=VDDDB=12V for NSi6602A/B, VDDA=VDDDB=15V for NSi6602C, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at Ta=25°C

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Input Side Supply						
VDDI Quiescent Current	I _{VDDIQ}		0.75	2	mA	INA=0, INB=0
VDDI Operating Current	I _{VDDI}		1.8		mA	Input frequency 500kHz, C _{OUTA/B} =15pF
VDDI UVLO Rising Threshold	V _{VDDI_ON}	2.35	2.55	2.75	V	
VDDI UVLO Falling Threshold	V _{VDDI_OFF}	2.15	2.35	2.55	V	
VDDI UVLO Hysteresis	V _{VDDI_HYS}		0.2		V	
Output Side Supply						
Output Side Supply Voltage	V _{VDDA} , V _{VDDDB}			25	V	Minimum defined by UVLO
VDDA/B Quiescent Current, per Channel	I _{VDDAQ} , I _{VDDDBQ}		1.6	2.5	mA	INA=0, INB=0, VDDx=12V for 6V,8V UVLO; VDDx=15V for 13V UVLO
VDDA/B Operation Current, per Channel	I _{VDDA} , I _{VDDDB}		3.2		mA	100pF, 500kHz, VDDx=12V for 6V,8V UVLO; VDDx=15V for 13V UVLO
VDDA/B UVLO Rising Threshold	V _{VDDA_ON} , V _{VDDDB_ON}	5.7	6.15	6.5	V	NSi6602A (6V)
VDDA/B UVLO Falling Threshold	V _{VDDA_OFF} , V _{VDDDB_OFF}	5.4	5.85	6.2	V	
VDDA/B UVLO Hysteresis	V _{VDDA_HYS} , V _{VDDDB_HYS}		0.3		V	
VDDA/B UVLO Rising Threshold	V _{VDDA_ON} , V _{VDDDB_ON}	8.1	8.5	8.9	V	NSi6602B (8V)
VDDA/B UVLO Falling Threshold	V _{VDDA_OFF} , V _{VDDDB_OFF}	7.6	8.0	8.4	V	
VDDA/B UVLO Hysteresis	V _{VDDA_HYS} , V _{VDDDB_HYS}		0.5		V	
VDDA/B UVLO Rising Threshold	V _{VDDA_ON} , V _{VDDDB_ON}	12.7	13.2	13.7	V	NSi6602C (13V)
VDDA/B UVLO Falling Threshold	V _{VDDA_OFF} , V _{VDDDB_OFF}	11.7	12.2	12.7	V	
VDDA/B UVLO Hysteresis	V _{VDDA_HYS} , V _{VDDDB_HYS}		1		V	
Input Side Characteristic						
Input Pin Pull Down Resistance, INA, INB	R _{INA_PD} , R _{INB_PD}		100		kΩ	
Input Pin Pull Down Resistance, DIS	R _{DIS_PD}		100		kΩ	
Logic High Input Threshold	V _{INA_H} , V _{INB_H} , V _{DIS_H}	1.5	1.7	2	V	

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Logic Low Input Threshold	$V_{INA_L}, V_{INB_L}, V_{DIS_L}$	0.8	1.1	1.3	V	
Input Hysteresis	$V_{INA_HYS}, V_{INB_HYS}, V_{DIS_HYS}$		0.6		V	
Output Side Characteristic						
Logic High Output Voltage	$V_{VDDA-V_{OUTA_H}}, V_{VDDB-V_{OUTB_H}}$		0.34		V	$I_{out} = 100mA$
Logic Low Output Voltage	V_{OUTA_L}, V_{OUTB_L}		55		mV	$I_{out} = -100mA$
Output Source Resistance ¹⁾	R_{OUTA_H}, R_{OUTB_H}		3.4		Ω	$I_{out} = 100mA$
Output Sink Resistance	R_{OUTA_L}, R_{OUTB_L}		0.55		Ω	$I_{out} = -100mA$
Peak Output Source Current	I_{OUTA+}, I_{OUTB+}		4		A	
Peak Output Sink Current	I_{OUTA-}, I_{OUTB-}		6		A	

- 1) The output source structure features a P-channel MOSFET and an N-channel MOSFET in parallel. The on-resistance of this N-channel MOSFET is approximately 1.1 Ω .

5.2. Switching Characteristics

VDDI=3.3V or 5V, VDDA=VDDB=12V for NSi6602A/B, VDDA=VDDB=15V for NSi6602C, Ta=-40°C to 125°C.

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Minimum Pulse Width	t_{PWmin}		10	15	ns	$C_{OUTA/B} = 0 pF$
Propagation Delay	t_{PDHL}, t_{PDLH}	10	25	35	ns	
Pulse Width Distortion $ t_{PDLH}-t_{PDHL} $	t_{PWD}			6	ns	
Channel to Channel Delay Matching	t_{DMLH}, t_{DMHL}			5	ns	
Programmed Deadtime	t_{DT}	160	200	240	ns	$t_{DT}(ns)=10 \cdot R(k\Omega)$; Test for $R = 20k\Omega, \pm 1\%$
Output Rise Time (20% to 80%)	t_R		7	16	ns	$C_{OUTA/B}=1.8nF$, verified by design
Output Fall Time (90% to 10%)	t_F		6	12	ns	$C_{OUTA/B}=1.8nF$, verified by design
Shutdown Time from Disable True	t_{DIS}			40	ns	
Recovery Time from Disable False	t_{EN}			40	ns	
VDDI Power-up Time Delay (Time from VDDI = VDDI_ON to OUTA/B = INA/B)	t_{start_VDDI}		8.5	15	us	INA or INB tied to VDDI
VDDA/B Power-up Time Delay (Time from VDDA/B = 2V to OUTA/B = INA/B)	$t_{start_VDDA}, t_{start_VDDB}$		18	30	us	INA or INB tied to VDDI $C_{OUTA/B}=1.8nF$
Common Mode Transient Immunity	CMTI	100	150		kV/us	verified by design

5.3. Typical Performance Characteristics

VDDI = 3.3 V, VDDA=VDDB=12V for NSi6602A/B, VDDA=VDDB=15V for NSi6602C, TA = 25°C. Output has no load unless otherwise noted.

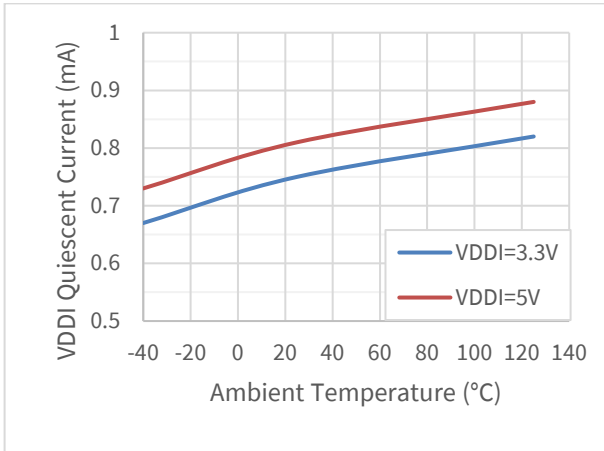


Figure 5.1 VDDI Quiescent Current vs Temperature

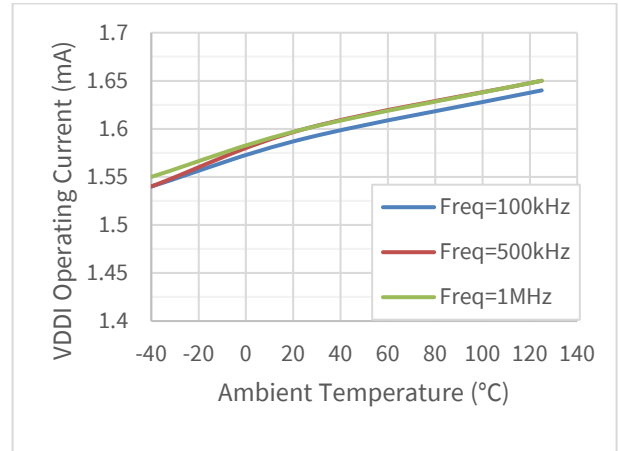


Figure 5.2 VDDI Operating Current vs Temperature

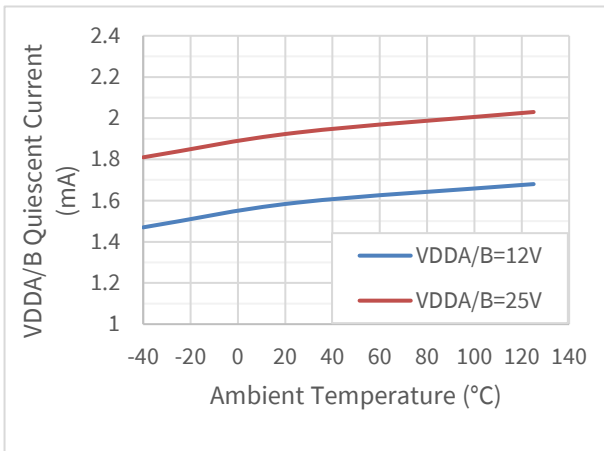


Figure 5.3 VDDA/B Quiescent Current vs Temperature

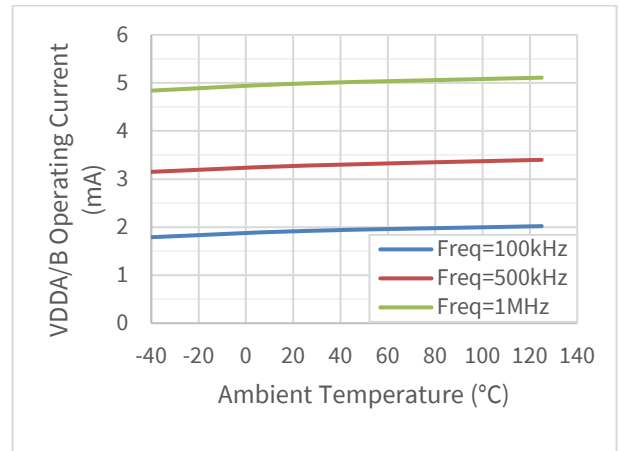


Figure 5.4 VDDA/B Operating Current vs Temperature

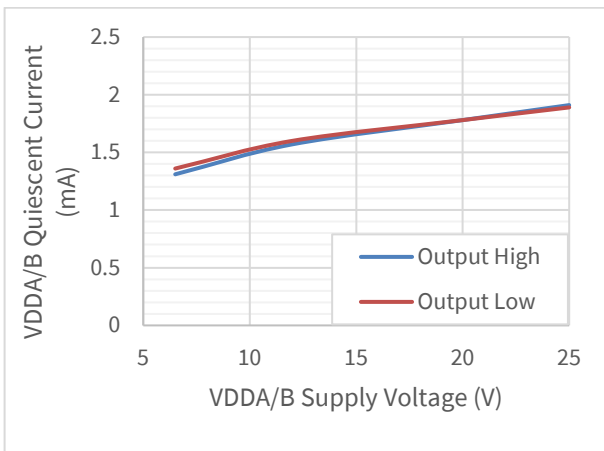


Figure 5.5 VDDA/B Quiescent Current vs Supply Voltage

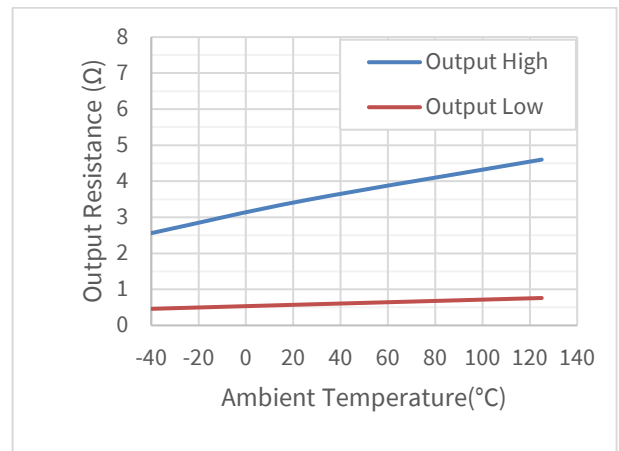


Figure 5.6 Output Resistance vs Temperature

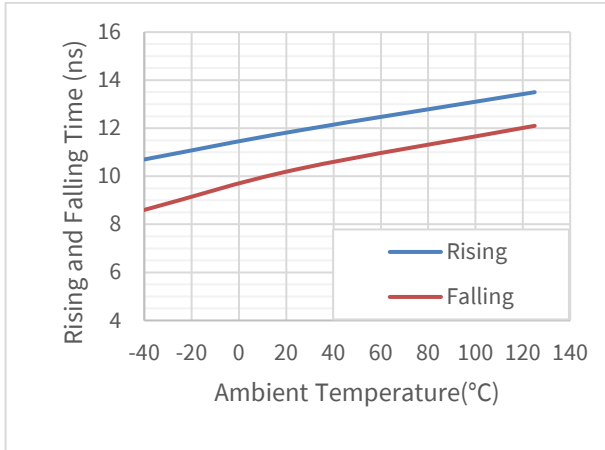


Figure 5.7 Typical Rise Time & Fall Time vs Temperature

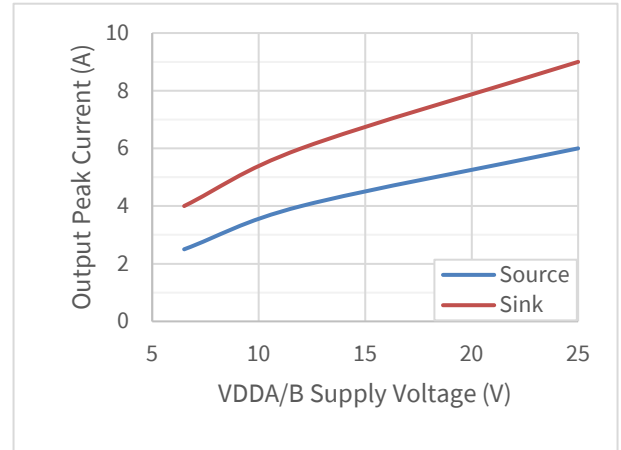


Figure 5.8 Output Peak Current vs VDDA/B Supply Voltage

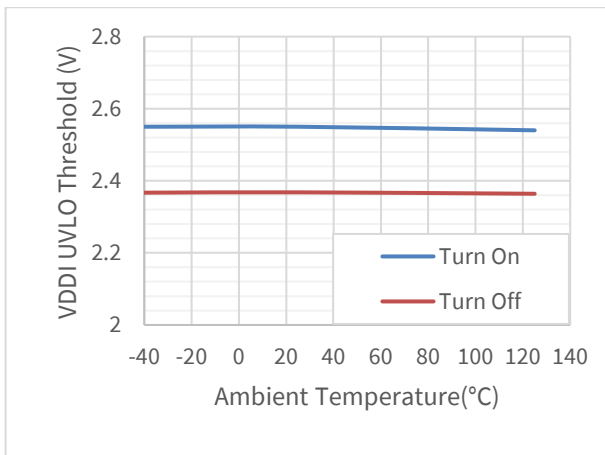


Figure 5.9 VDDI UVLO Threshold vs Temperature

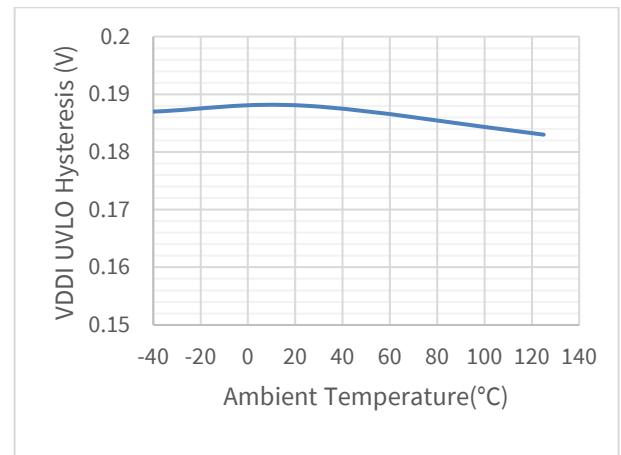


Figure 5.10 VDDI UVLO Hysteresis vs Temperature

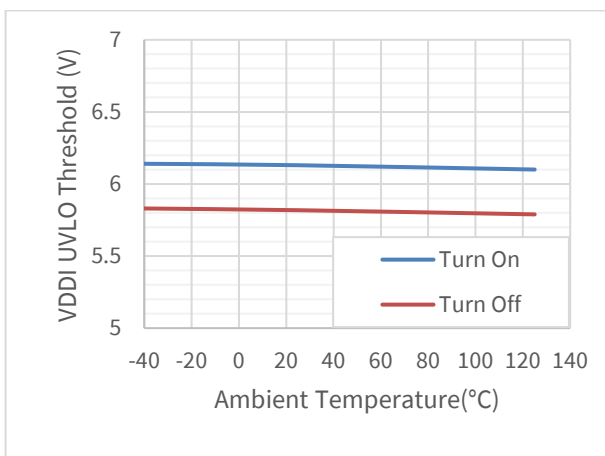


Figure 5.11 6V VDDA/B UVLO Threshold vs Temperature

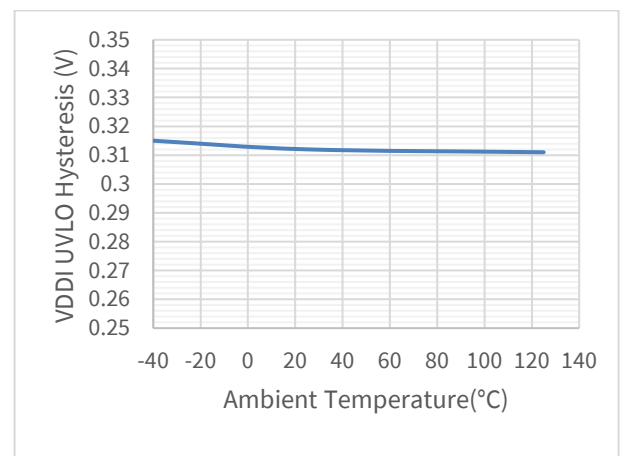


Figure 5.12 6V VDDA/B UVLO Hysteresis vs Temperature

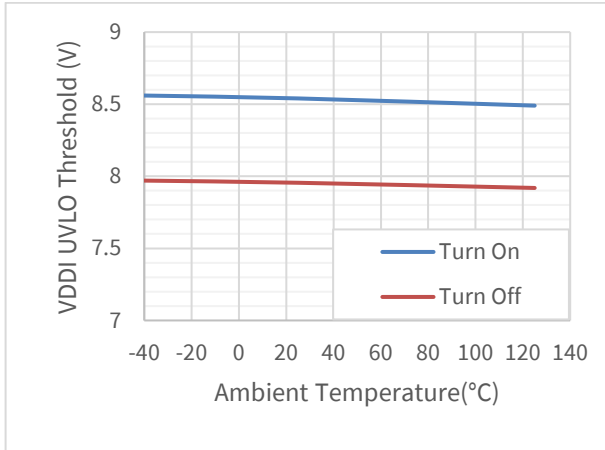


Figure 5.13 8V VDDA/B UVLO Threshold vs Temperature

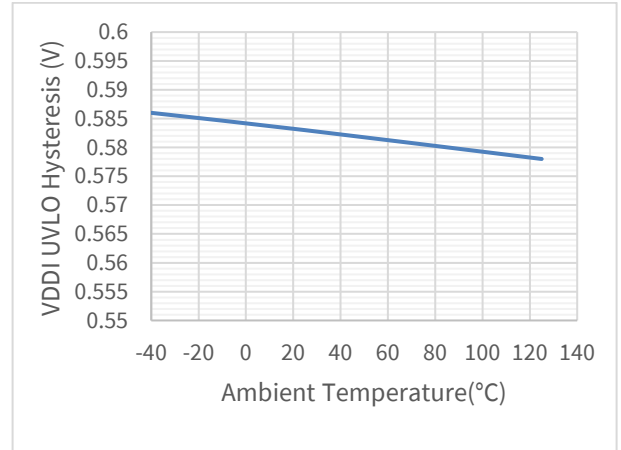


Figure 5.14 8V VDDA/B UVLO Hysteresis vs Temperature

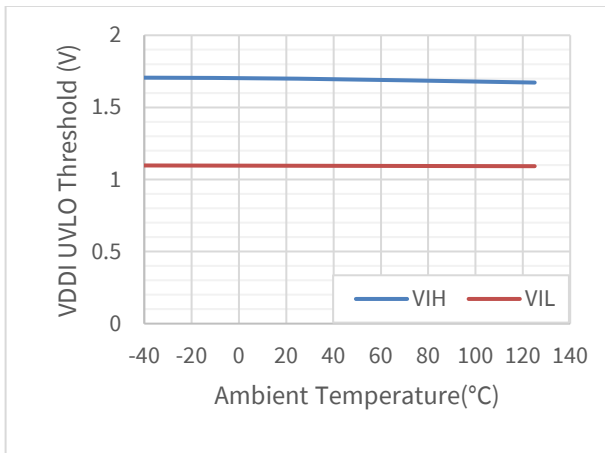


Figure 5.15 INA/INB/DIS Threshold vs Temperature

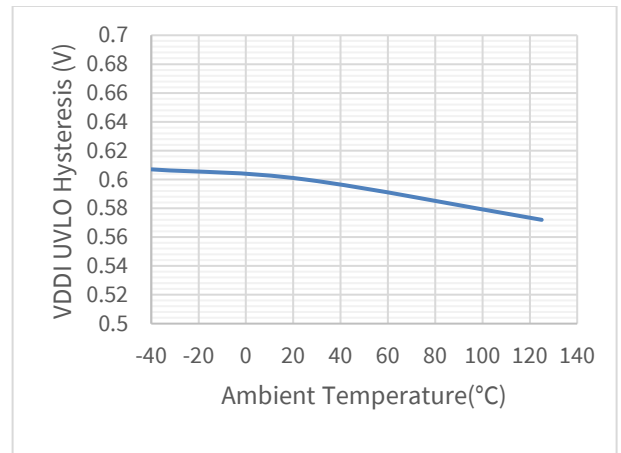


Figure 5.16 INA/INB/DIS Hysteresis vs Temperature

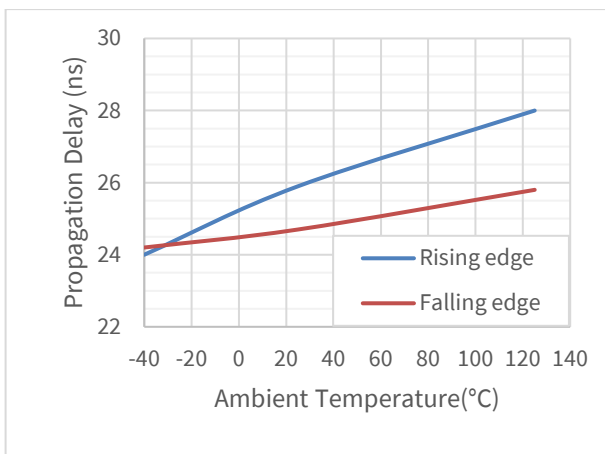


Figure 5.17 Propagation Delay vs Temperature

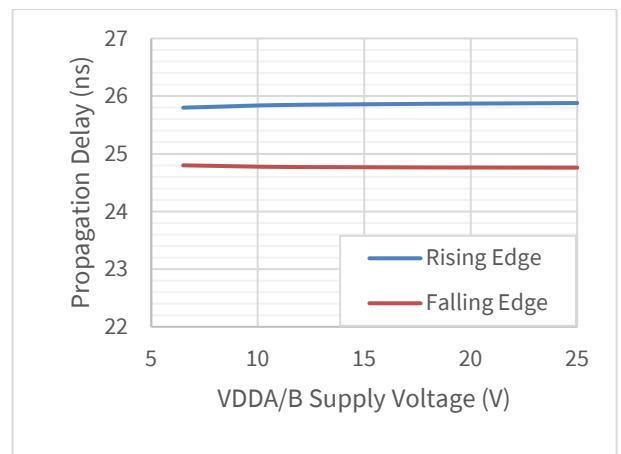


Figure 5.18 Propagation Delay vs VDDA/B

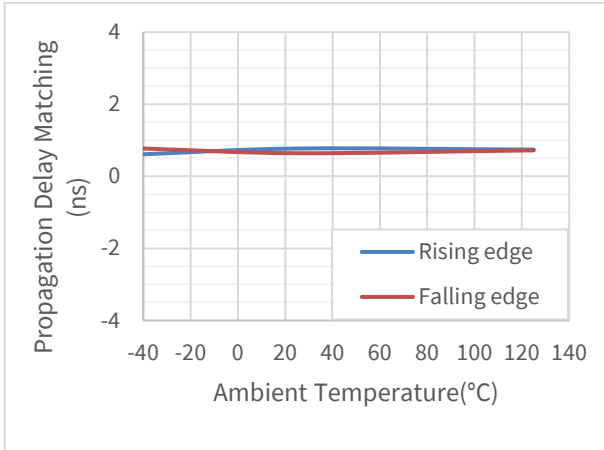


Figure 5.19 Propagation Delay Matching vs Temperature

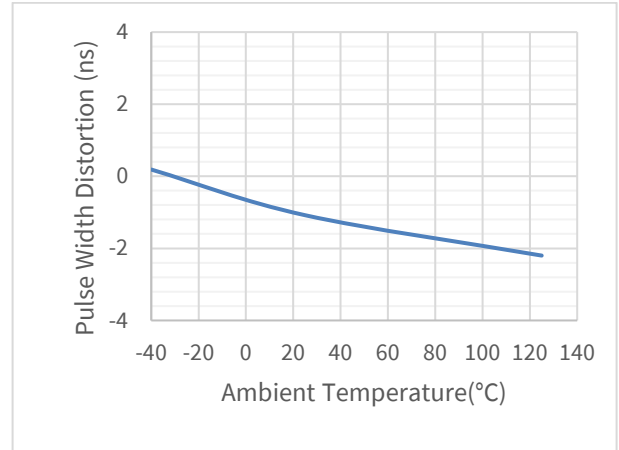


Figure 5.20 Pulse Width Distortion vs Temperature

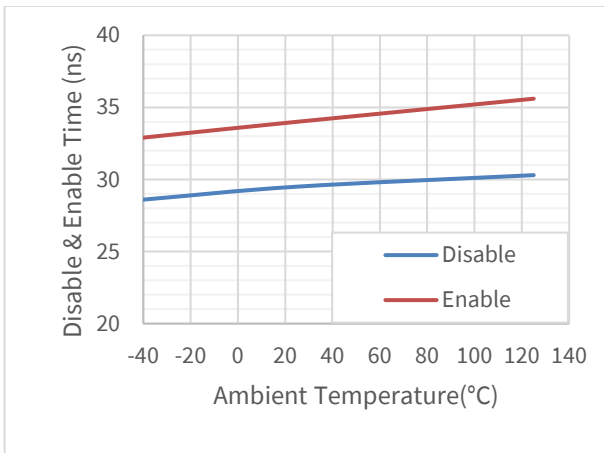


Figure 5.21 Disable & Enable Time vs Temperature

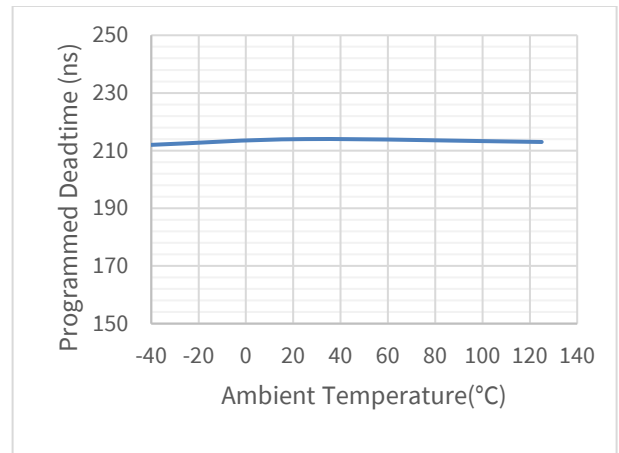


Figure 5.22 Deadtime (RDT=20kΩ) vs Temperature

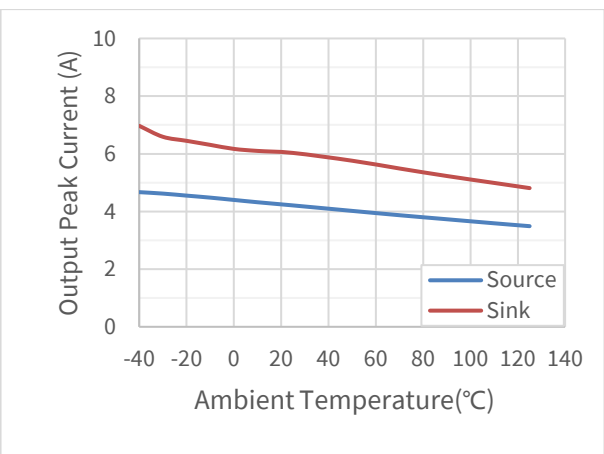


Figure 5.23 Output Peak Current vs Temperature

5.4. Parameter Measurement Information

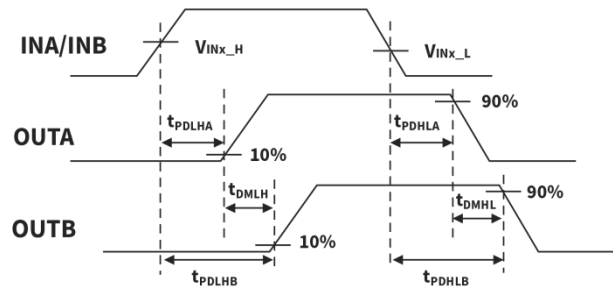


Figure 5.23 Propagation Delay and Channel to Channel Delay Match Time, connect DT to VDDI

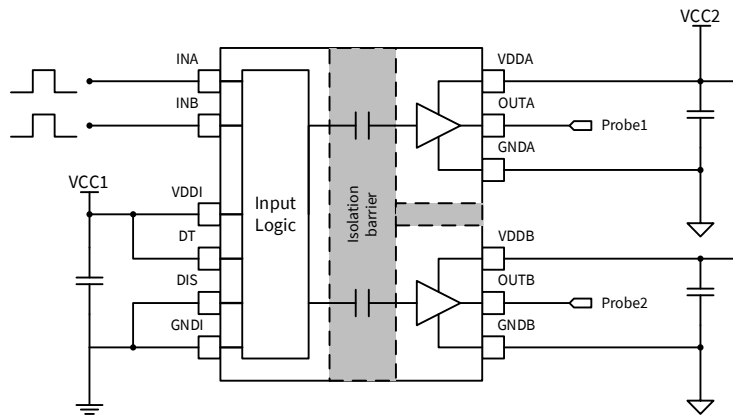


Figure 5.24 Channel to Channel Delay Match Test Circuit

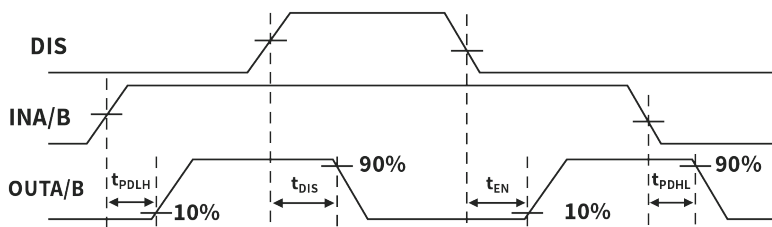


Figure 5.25 Disable Time and Enable Time

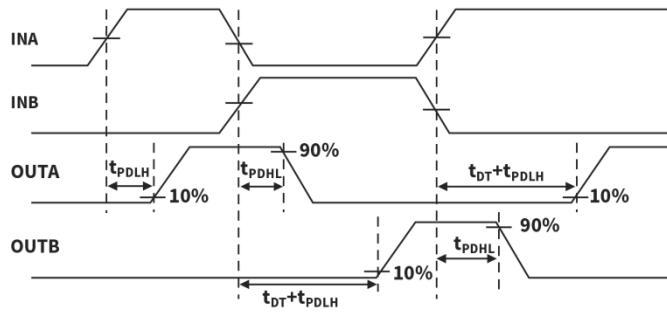


Figure 5.26 Deadtime, Determined by RDT

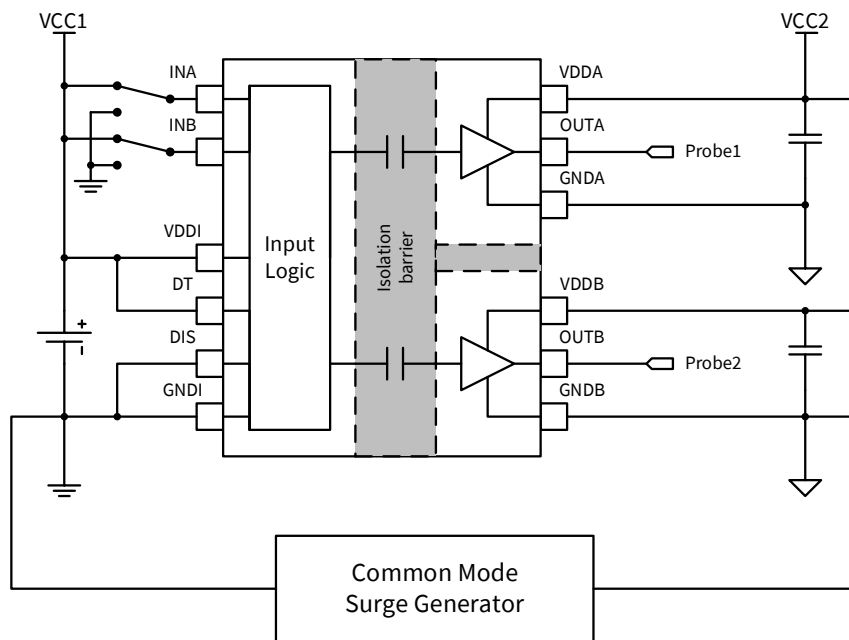


Figure 5.27 Common-Mode Transient Immunity Test Circuit

6. High Voltage Feature Description

6.1. Insulation Characteristics

Description	Test Condition	Symbol	Value		Unit
			SOW16/14	SOP16	
Min. External Air Gap (Clearance)		CLR	8	4	mm
Min. External Tracking (Creepage)		CPG	8	4	mm
Distance through the Insulation ²⁾		DTI	32		um
Comparative Tracking Index	DIN EN 60112 (VDE 0303-11)	CTI	>600		V
Material Group	IEC 60664-1		I		
Installation Classification per DIN VDE 0110					
For Rated Mains Voltage ≤ 150Vrms			I to IV	I to IV	
For Rated Mains Voltage ≤ 300Vrms			I to IV	I to III	
For Rated Mains Voltage ≤ 600Vrms			I to IV	I to II	
For Rated Mains Voltage ≤ 1000Vrms			I to III	/	
Insulation Specification per DIN VDE V 0884-11:2017-01 ¹⁾					
Climatic Category			40/125/21		
Pollution Degree	per DIN VDE 0110, Table 1		2		
Maximum Working Isolation Voltage	AC voltage	V_{IOWM}	1000	700	V_{RMS}
	DC voltage		1414	990	V_{DC}
Maximum Repetitive Isolation Voltage		V_{IORM}	1414	990	V_{peak}
Input to Output Test Voltage, Method B1	$V_{ini.b} = V_{IOTM}$, $V_{pd(m)} = V_{IORM} \times 1.5$, $t_{ini} = t_m = 1 \text{ sec}$, $q_{pd} \leq 5 \text{ pC}$, 100% production test	$V_{pd(m)}$	/	1485	V_{peak}
	$V_{ini.b} = V_{IOTM}$, $V_{pd(m)} = V_{IORM} \times 1.875$, $t_{ini} = t_m = 1 \text{ sec}$, $q_{pd} \leq 5 \text{ pC}$, 100% production test	$V_{pd(m)}$	2652	/	V_{peak}
Input to Output Test Voltage, Method A. After Environmental Tests Subgroup 1	$V_{ini.a} = V_{IOTM}$, $V_{pd(m)} = V_{IORM} \times 1.3$, $t_{ini} = 60 \text{ sec}$, $t_m = 10 \text{ sec}$, $q_{pd} \leq 5 \text{ pC}$	$V_{pd(m)}$	/	1287	V_{peak}
	$V_{ini.a} = V_{IOTM}$, $V_{pd(m)} = V_{IORM} \times 1.6$, $t_{ini} = 60 \text{ sec}$, $t_m = 10 \text{ sec}$, $q_{pd} \leq 5 \text{ pC}$	$V_{pd(m)}$	2263	/	V_{peak}
Input to Output Test Voltage, Method A. After Input and Output Safety Test Subgroup 2 and Subgroup 3	$V_{ini.a} = V_{IOTM}$, $V_{pd(m)} = V_{IORM} \times 1.2$, $t_{ini} = 60 \text{ sec}$, $t_m = 10 \text{ sec}$, $q_{pd} \leq 5 \text{ pC}$	$V_{pd(m)}$	1697	1188	V_{peak}

Description	Test Condition	Symbol	Value		Unit
Maximum Transient Isolation Voltage	t = 60 sec	V _{IOTM}	8000	4242	V _{peak}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50us waveform, V _{TEST} = 1.3 × V _{IOSM}	V _{IOSM}	/	6000	V _{peak}
	Test method per IEC62368-1, 1.2/50us waveform, V _{TEST} = 1.6 × V _{IOSM}		6250	/	V _{peak}
Isolation Resistance	V _{IO} = 500 V, T _{amb} = T _s	R _{IO}	>10 ⁹		Ω
	V _{IO} = 500 V, 100 °C ≤ T _{amb} ≤ 125 °C		>10 ¹¹		Ω
Isolation Capacitance	f = 1MHz	C _{IO}	1.2		pF
Insulation Specification per UL1577					
Withstand Isolation Voltage	V _{TEST} = 1.2 × V _{ISO} , t = 1 sec, 100% production test	V _{ISO}	5700	3000	V _{rms}

- 1) This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- 2)

6.2. Safety-Limiting Values

Reinforced isolation safety-limiting values as outlined in VDE-0884-11 of NSi6602x-xSWxR (SOW16/SOW14)

Description	Test Condition	Side	Value	Unit
Safety Supply Power	R _{θJA} = 97 °C/W ¹⁾ , T _J = 150 °C, T _A = 25 °C	Input	12	mW
		Driver A, Driver B	638	mW
		Total	1288	mW
Safety Supply Current	R _{θJA} = 97 °C/W ¹⁾ , V _{DDA/B} = 12V, T _J = 150 °C, T _A = 25 °C	Driver A, Driver B	53.1	mA
	R _{θJA} = 97 °C/W ¹⁾ , V _{DDA/B} = 25V, T _J = 150 °C, T _A = 25 °C	Driver A, Driver B	25.5	mA
Safety Temperature ²⁾			150	°C

- 1) Calculate with the junction-to-air thermal resistance, R_{θJA}, of SOW16/SOW14 package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

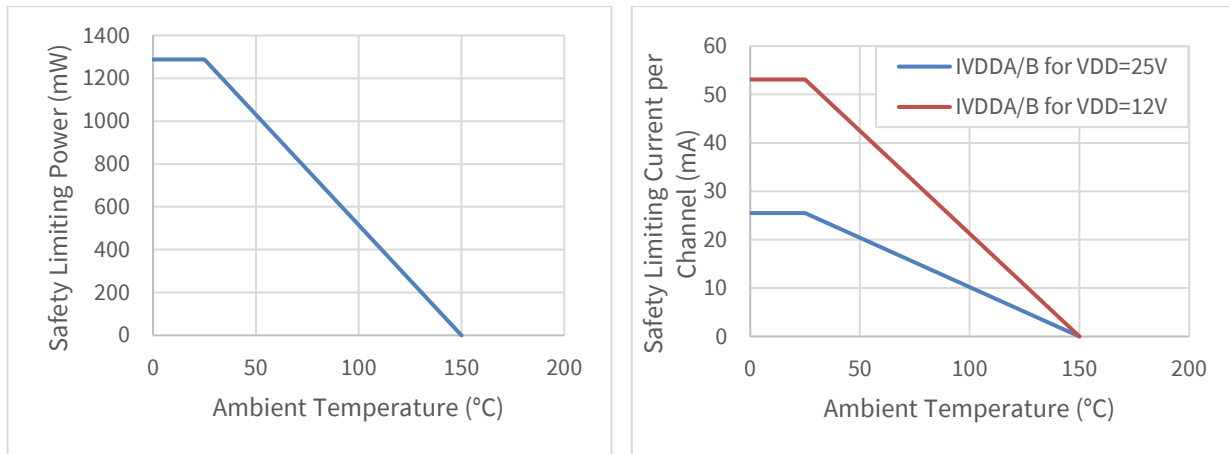


Figure 6.1 NSi6602x-Q1SWR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

Basic isolation safety-limiting values as outlined in VDE-0884-11 of NSi6602x-xSPNR (SOP16)

Description	Test Condition	Side	Value	Unit
Safety Supply Power	$R_{\theta JA} = 150.5 \text{ } ^\circ\text{C/W}^1$, $T_J = 150 \text{ } ^\circ\text{C}$, $T_A = 25 \text{ } ^\circ\text{C}$	Input	12	mW
		Driver A, Driver B	409	mW
		Total	830	mW
Safety Supply Current	$R_{\theta JA} = 150.5 \text{ } ^\circ\text{C/W}^1$, $V_{DDA/B} = 12\text{V}$, $T_J = 150 \text{ } ^\circ\text{C}$, $T_A = 25 \text{ } ^\circ\text{C}$	Driver A, Driver B	34.0	mA
	$R_{\theta JA} = 150.5 \text{ } ^\circ\text{C/W}^1$, $V_{DDA/B} = 25\text{V}$, $T_J = 150 \text{ } ^\circ\text{C}$, $T_A = 25 \text{ } ^\circ\text{C}$	Driver A, Driver B	16.3	mA
Safety Temperature ²⁾			150	$^\circ\text{C}$

- 1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOP16 package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

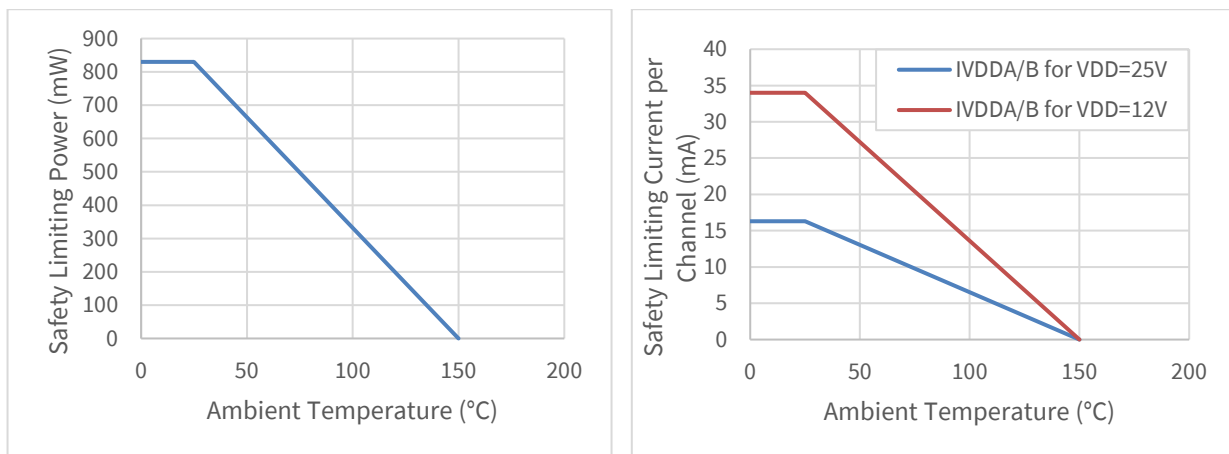


Figure 6.2 NSi6602x-Q1SWR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

6.3. Safety-Related Certifications

The NSi6602x-Q1SWxR(SOW16/SOW14) are approved or pending approval by the organizations listed in table.

<i>CUL</i>		<i>VDE</i>		<i>CQC</i>
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11: 2017-01		Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 5700Vrms Isolation voltage	Single Protection, 5700Vrms Isolation voltage	Reinforced insulation at $V_{IORM}=1414V_{PEAK}$ $V_{IOSM}=6250V_{PEAK}$ $V_{IOTM}=8000V_{PEAK}$		Reinforced insulation
E500602	E500602	Certification No. 40052820		CQC20001264939

The NSi6602x-Q1SPNR(SOP16) are approved or pending approval by the organizations listed in table.

<i>CUL</i>		<i>VDE</i>		<i>CQC</i>
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-11):2017-01		Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 3000Vrms Isolation voltage	Single Protection, 3000Vrms Isolation voltage	Basic insulation at $V_{IORM}=990V_{PEAK}$ $V_{IOSM}=6000V_{PEAK}$ $V_{IOTM}=4242V_{PEAK}$		Basic insulation
E500602	E500602	File (pending)		CQC21001289931

7. Function Description

7.1. Overview

NSi6602 is a high reliability dual channel isolated gate driver which could be designed in variety switching power and motor drive topologies. NSi6602 has some useful protections, such as under voltage lock-out (UVLO) for both input and output supply, a disable pin, dead-time control, default low output as input is floating. The functional circuit block diagram is shown as below:

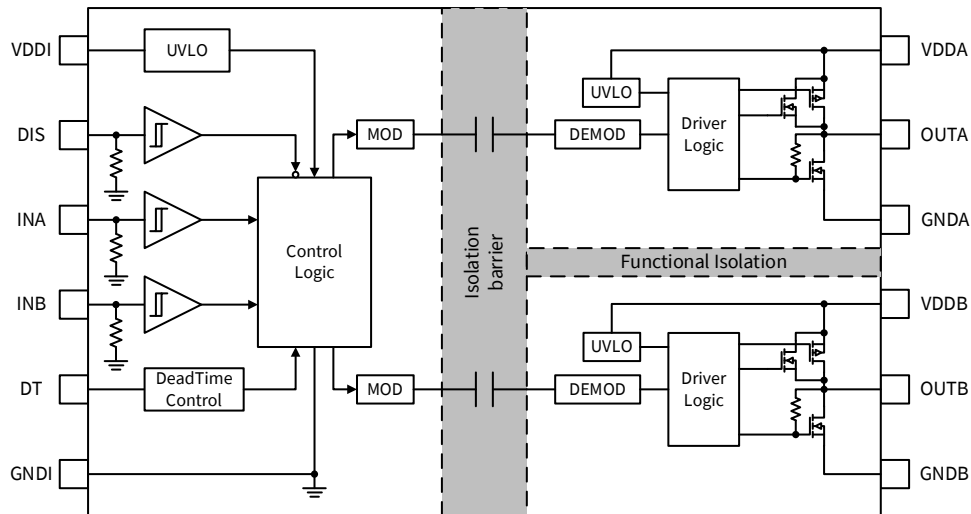


Figure 7.1 Functional Block Diagram

7.2. Under Voltage Lock Out (UVLO)

The NSi6602 has an internal under voltage lock out (UVLO) protection on both input and output supply circuit blocks. The driver output is held low by an active clamp circuit when the supply voltage of VDDI or VDDA/VDDB is lower than V_{VDD_ON} at power-up status or lower than V_{VDD_OFF} after power-up, regardless of the status of the input pins.

The VDDI and VDDA/B ULVO protections have hysteresis (V_{VDD_HYS}) to prevent chatter noise from VDD supply and allow small drops in supply power which are usually happened in startup.

7.3. Input and Output Logic Table

When the device is power up, setting the DIS pin high can shut down both outputs simultaneously. Left open or grounding the DIS pin can allow the device operating normally.

Table 7.1 Output status vs. Input and Power status

VDDI status	VDDA/B status	DIS	IN		OUT		NOTE ¹⁾
			A	B	A	B	
PU	PU	L or O	L	H	L	H	If Deadtime function is used, output transits to high after the deadtime expires.
PU	PU	L or O	H	L	H	L	
PU	PU	L or O	H	H	H	H	DT pin is pulled to VDDI.
PU	PU	L or O	H	H	L	L	DT is left open or programmed with R _{DT} .
PU	PU	L or O	L	L	L	L	
PU	PU	L or O	O	O	L	L	
PU	PU	H	X	X	L	L	
PU	PD	X	X	X	L	L	
PD	PU	X	X	X	L	L	

1) PD= Power Down; PU= Power Up; H= Logic High; L= Logic Low; O= Left Open; X= Irrelevant.

7.4. Programmable Deadtime (DT pin)

7.4.1. Pulling the DT Pin to VDDI

This allows outputs match inputs completely and no deadtime is asserted.

7.4.2. DT Pin Left Open or Connected to a Programming Resistor between DT and GND Pins

If the DT pin is left open, the deadtime duration (t_{DT}) is set to <35ns. t_{DT} can be programmed by placing a resistor, R_{DT}, between the DT pin and GND. The appropriate R_{DT} value can be determined from Equation 1, where R_{DT} is in kΩ and t_{DT} in ns:

$$t_{DT} \approx 10 \times R_{DT} \tag{1}$$

The recommended value of R_{DT} is between from 1kΩ to 200kΩ. The steady state voltage at DT pin is about 0.8 V, and the DT pin current will be less than 10uA when R_{DT} =100kΩ. It is also recommended to parallel a ceramic capacitor, for example 2.2nF, with R_{DT} to achieve better noise immunity.

The programmed deadtime is activated by the input signal’s falling edge to prevent shoot-through when the device is designed in an application of high side and low side driver. The details of input and output logic with deadtime are shown as Figure 7.2:

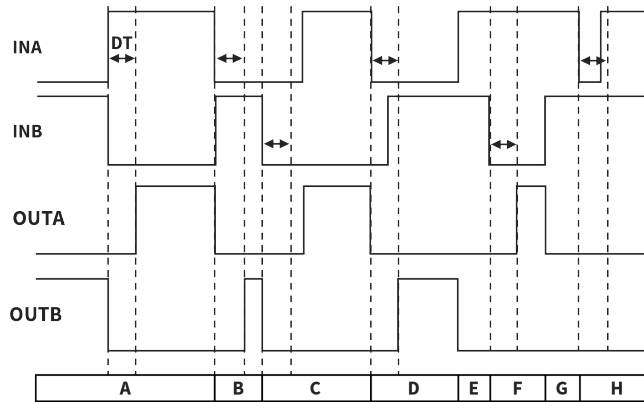


Figure 7.2 Input and Output Logic with the Programmed Deadtime

Condition	Result
A: INA goes high, and INB goes low.	OUTB goes low immediately, then OUTA goes high after the programmed deadtime which is assigned at INB goes low.
B: INA goes low, and INB goes high.	OUTA goes low immediately, then OUTB goes high after the programmed deadtime which is assigned at INA goes low.
C: INB goes low, then INA goes high after deadtime.	OUTB goes low immediately, then OUTA goes high immediately when INA goes high.
D: INA goes low, then INB goes high before deadtime.	OUTA goes low immediately, then OUTB goes high after deadtime
E: INA goes high, INB is still high.	OUTB goes low immediately and OUTA keeps low.
F: INA is still high, INB goes low.	OUTA goes high after deadtime while INB is low and OUTB keeps low.
G: INA is still high, INB goes high after deadtime	OUTA goes low immediately and OUTB keeps low.
H: INA goes low then goes high before deadtime while INB is still high.	OUTA keeps low and OUTB keeps low because deadtime control.

7.5. ESD Protection

Figure 7.3 shows the multiple diodes involved in the ESD protection part of NSi6602.

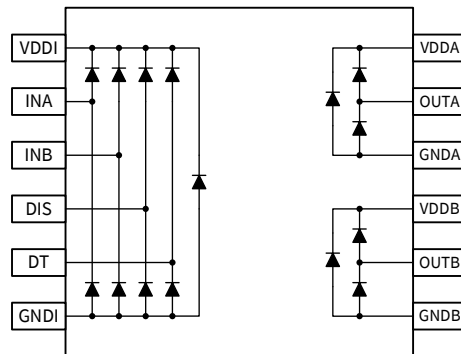


Figure 7.3 ESD Structure

8. Application Note

8.1. Typical Application Circuit

The circuit shows a typical half-bridge configuration by using the driver NSi6602 which could be used in several popular power converter topologies such as half-bridge/full bridge/LLC isolated topologies, buck-boost topologies and 3-phase motor drive applications.

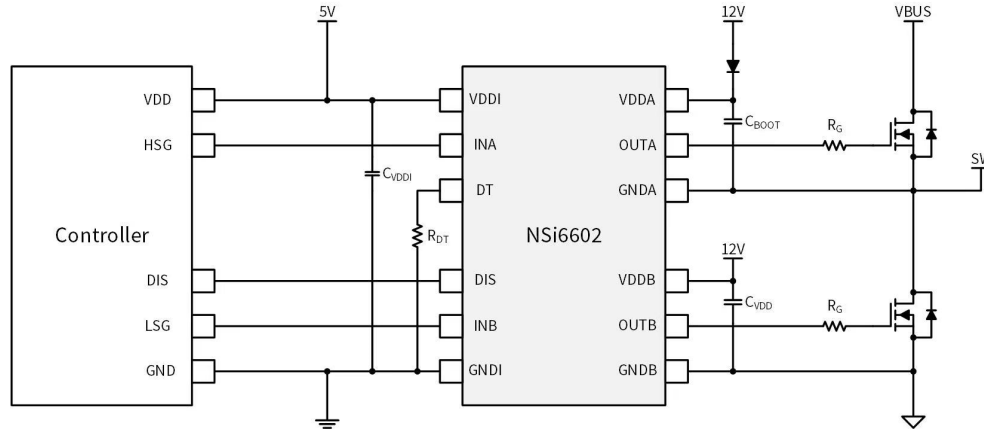


Figure 8.1 Typical Half-Bridge Application Schematic

8.2. PCB Layout

PCB layout is important to get optimal performance. Some key guidelines are given as below:

- Low-ESR and low-ESL bypass capacitors should be placed close to the device between pin VDDI to GND and pin VDDA/B to GNDA/B.
- There is high frequency switching current that charges and discharges the gate of external power transistor, leading to EMI and ring issues. The parasitic inductance of this loop should be minimized, by decreasing loop area and placing NSi6602 close to power transistor.
- Large amount of copper should be placed at VDDA/B pin and GNDA/B pin for thermal dissipation.
- To ensure isolation performance between primary and secondary side, the space under the device should keep free from any plane, trace, pad or via.

9. Package information

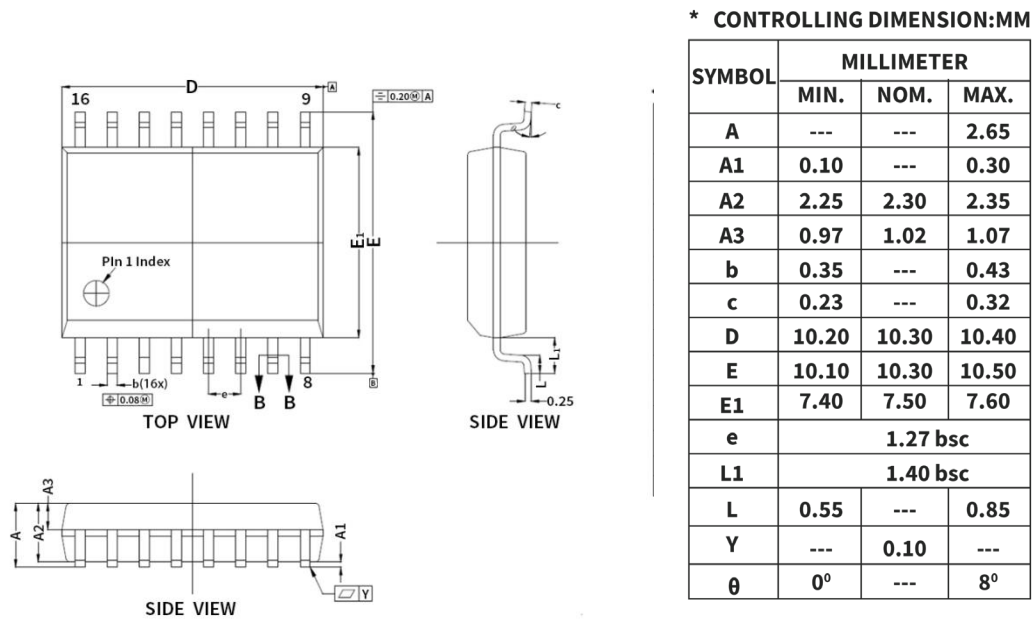


Figure 9.1 SOW16 Package Shape and Dimension

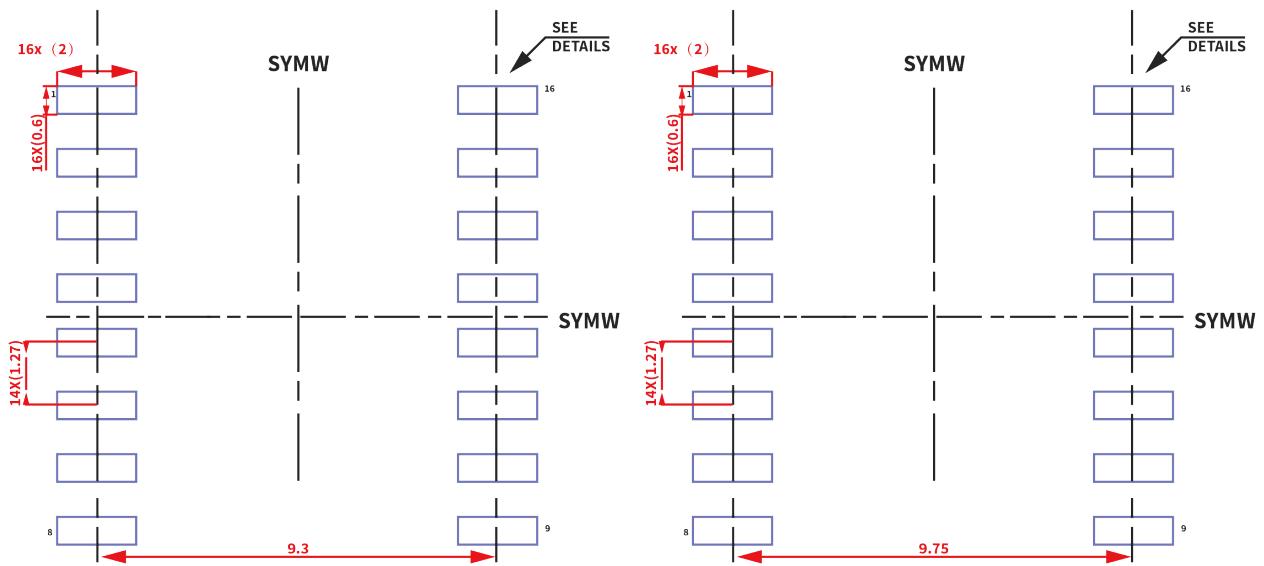


Figure 9.2 SOW16 Package Board Layout Example(mm)

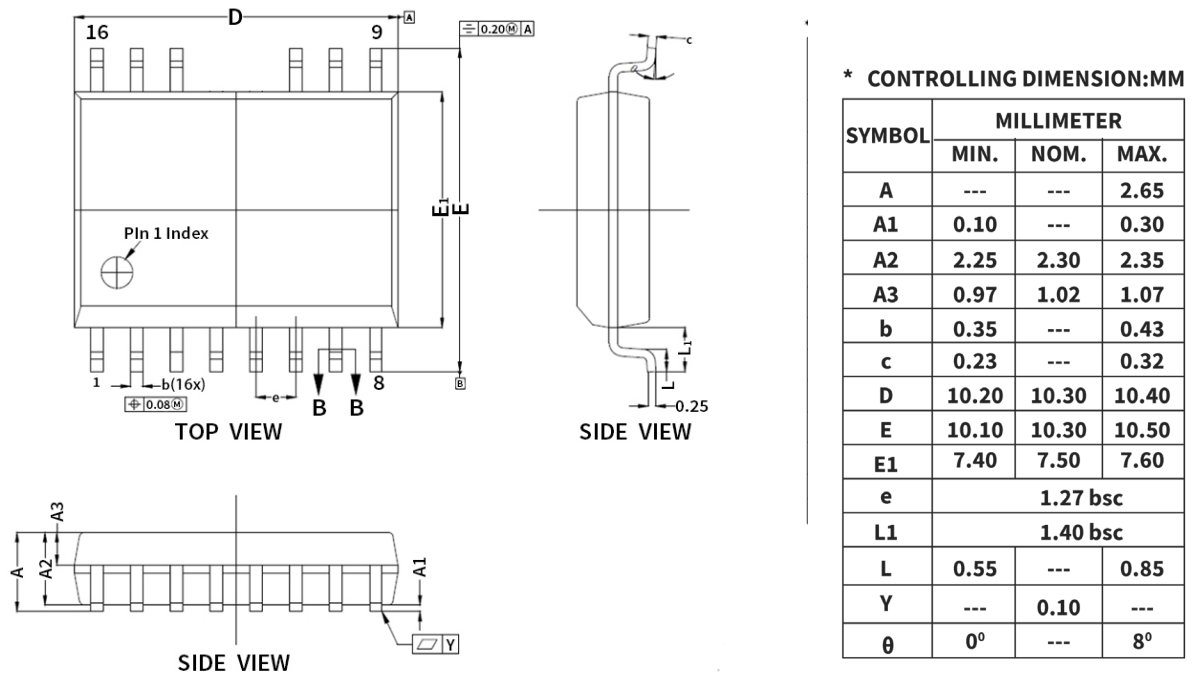


Figure 9.3 SOW14 Package Shape and Dimension

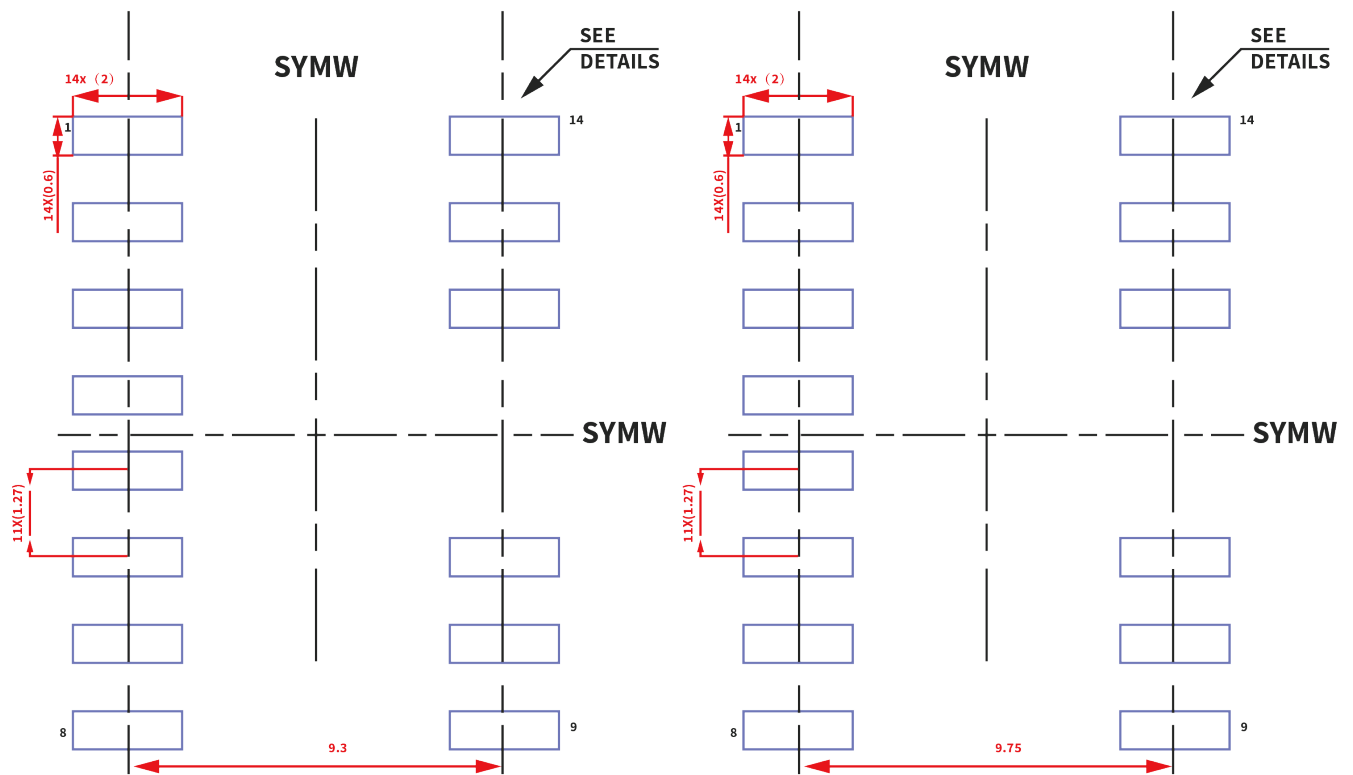


Figure 9.4 SOW14 Package Board Layout Example(mm)

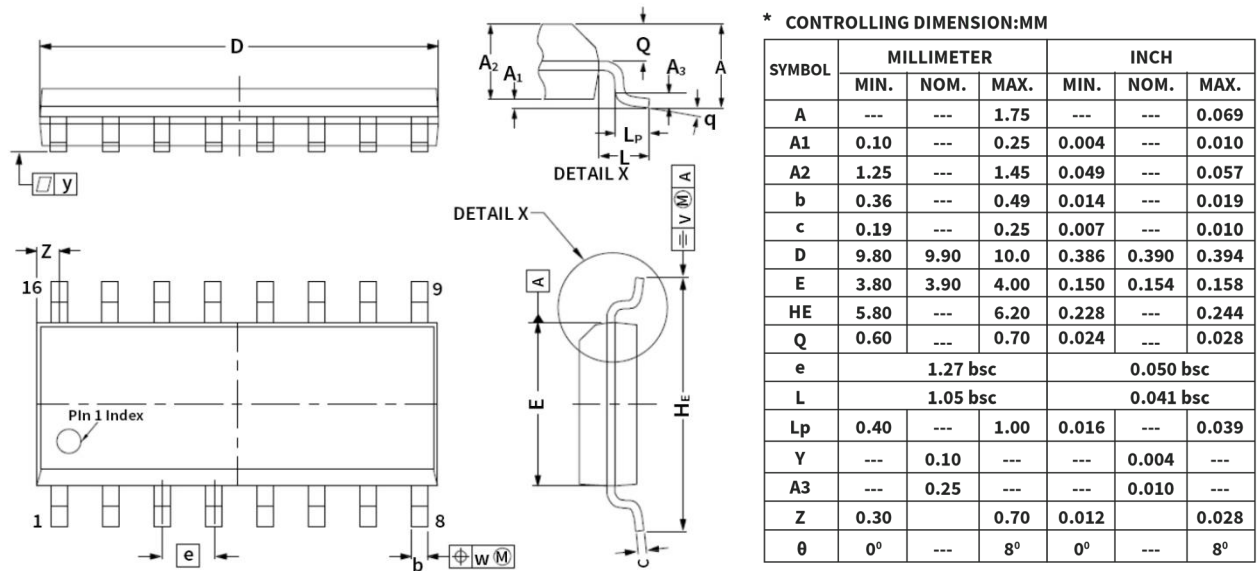


Figure 9.3 SOP16 Package Shape and Dimension

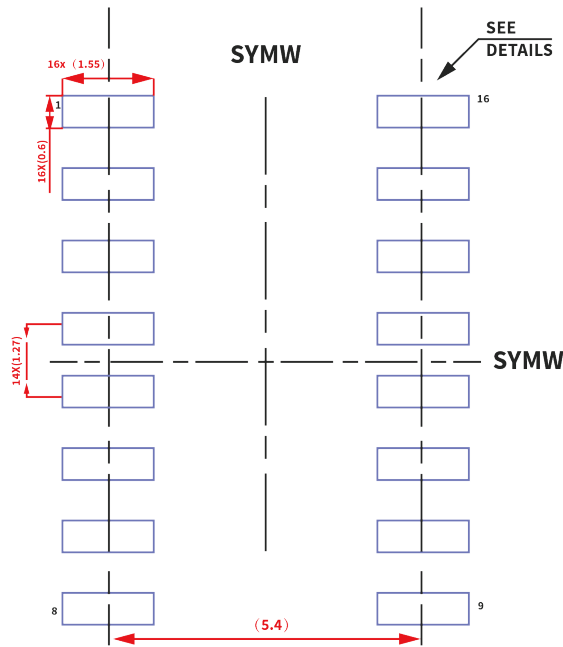


Figure 9.4 SOP16 Package Board Layout Example(mm)

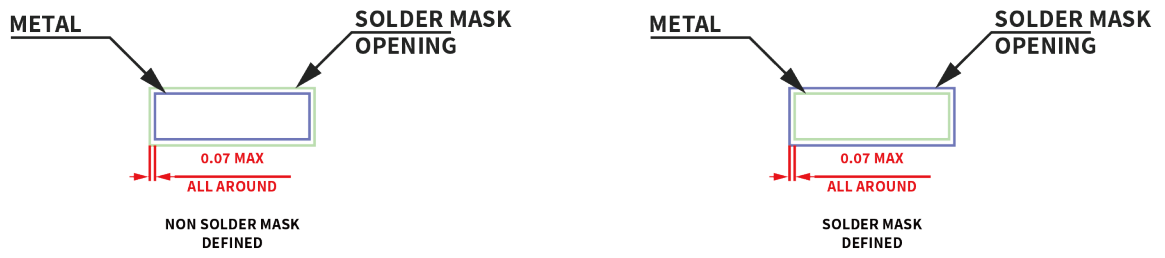


Figure 9.5 Solder Mask Details(mm)

10. Ordering Information

Part No.	Isolation Rating(kV_{RMS})	Driver-side UVLO TYP.	Temperature	Auto-motive ¹	Package Type	Package Drawing	MSL	SPQ
NSi6602A-Q1SWR	5.7	6V	-40 to 125°C	YES	SOP16(300mil)	SOW16	2	1000
NSi6602B-Q1SWR	5.7	8V	-40 to 125°C	YES	SOP16(300mil)	SOW16	2	1000
NSi6602C-Q1SWR	5.7	13V	-40 to 125°C	YES	SOP16(300mil)	SOW16	2	1000
NSi6602A-Q1SWKR	5.7	6V	-40 to 125°C	YES	SOP14(300mil)	SOW14	2	1000
NSi6602B-Q1SWKR	5.7	8V	-40 to 125°C	YES	SOP14(300mil)	SOW14	2	1000
NSi6602C-Q1SWKR	5.7	13V	-40 to 125°C	YES	SOP14(300mil)	SOW14	2	1000
NSi6602A-Q1SPNR	3.0	6V	-40 to 125°C	YES	SOP16(150mil)	SOP16	1	2500
NSi6602B-Q1SPNR	3.0	8V	-40 to 125°C	YES	SOP16(150mil)	SOP16	1	2500
NSi6602C-Q1SPNR	3.0	13V	-40 to 125°C	YES	SOP16(150mil)	SOP16	1	2500

1) All devices in auto-motive class are AEC-Q100 qualified.

11. Tape and Reel Information

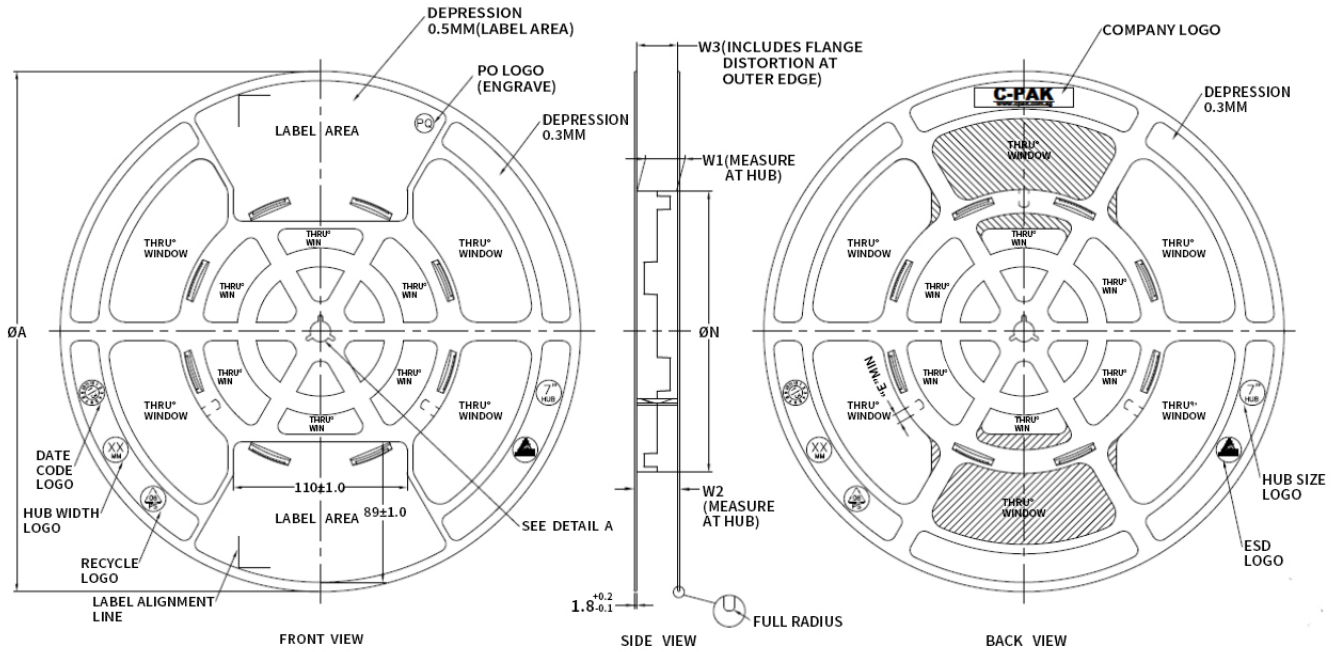
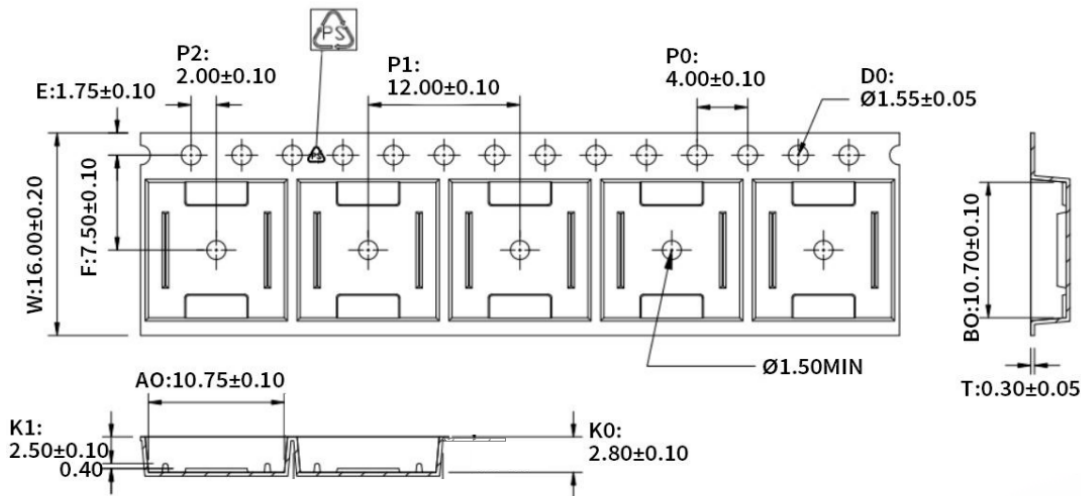


Figure 11.1 Tape Information



1. 1.10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481 requirements.
5. Thickness: 0.30±0.05mm.
6. Packing length per 22" reel: 378 Meters.(N=122)
7. Component load per 13" reel: 1000 pcs.

Figure 11.2 SOW16/SOW14 Reel Information

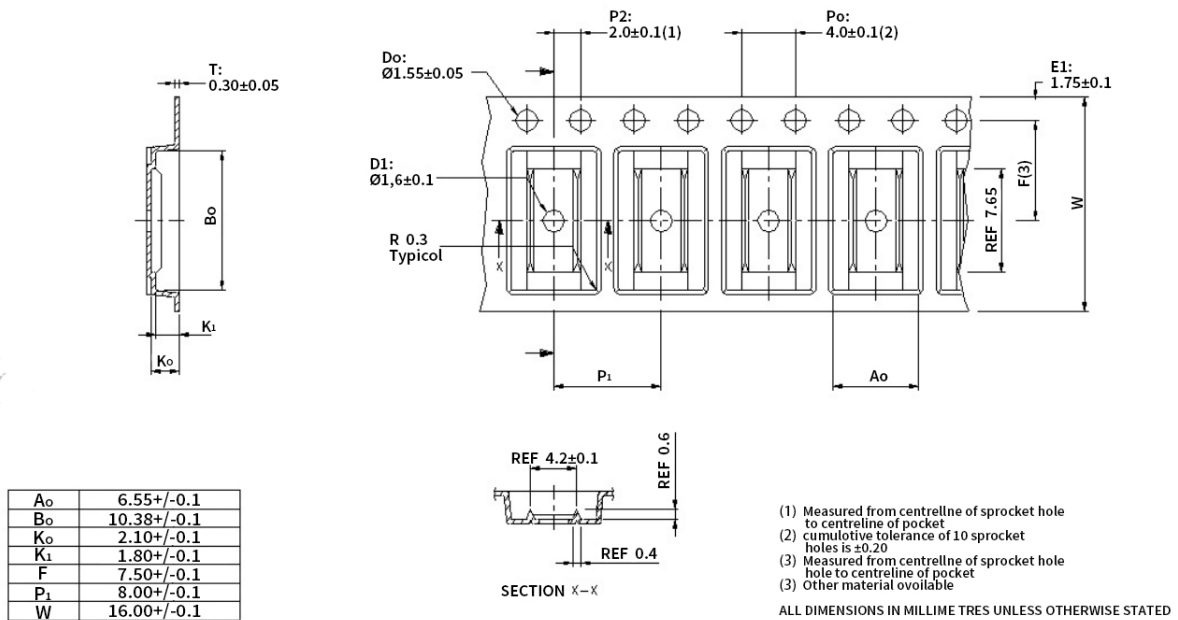


Figure 11.3 SOP16 Reel Information

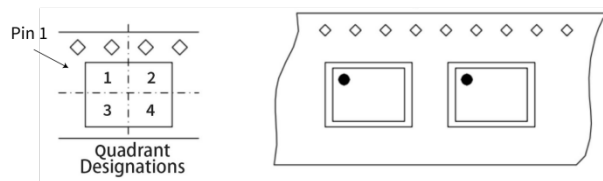


Figure 11.4 Quadrant Designation for Pin1 Orientation in Tape

12. Revision History

Revision	Description	Date
1.0	Initial release	2021/7/20
1.1	Add Figure 5.23.	2022/9/28

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