NSI6801M

Single-Channel Isolated Gate Driver

Datasheet (EN) 1.0

Product Overview

The NSI6801M is a single-channel isolated gate driver which is designed to drive power MOSFET, SiC, and IGBT transistors. It can source and sink 5A peak current and an integrated active Miller Clamp circuit with the same current rating to prevent false turn on caused by Miller current. System robustness is supported by 150kV/us minimum common-mode transient immunity (CMTI).

The driver operates with a maximum supply voltage of 32V. While the input circuit imitates the characters of LEDs, it has performance advantages compared to standard opto isolated gate drivers, including better reliability and aging performance, higher working temperature, shorter propagation delay and smaller pulse width distortion.

As a result, the NSI6801M is suitable to replace opto-isolated driver in high reliability, power density and efficiency switching power system.

Key Features

- 5.7kV$_{RMS}$ withstand isolation voltage
- Up to 32V output driver supply voltage
  -9V and 12V UVLO Options
- 5A peak current at rail-to-rail outputs
- High CMTI: ±150kV/us
- Active Miller Clamp
- 30ns maximum pulse width distortion
- Operation ambient temperature: -40°C ~125°C
- RoHS & REACH Compliance
- Lead-free component, suitable for lead-free soldering profile: 260°C ,MSL3

Safety Regulatory Approvals

- UL recognition: 5700V$_{RMS}$ SOW8 for 1 minute per UL1577
- DIN VDE V 0884-11:2017-01
- CSA component notice 5A
- CQC certification per GB4943.1-2011

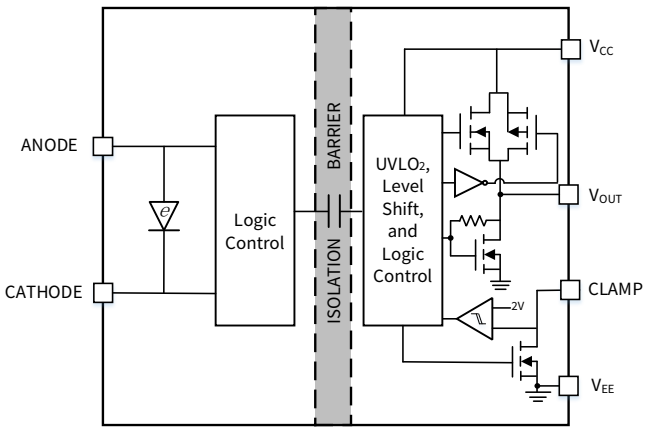
Applications

- DC-to-AC solar inverters
- Motor drives
- UPS and battery chargers
- Isolated DC/DC and AC/DC power supplies

Device Information

Part Number	*UVLO Level*	*Package*	*Body Size*
NSI6801MC-DSWVR	12V	SOW8	7.5×5.85×2.3mm
NSI6801MB-DSWVR	9V	SOW8	7.5×5.85×2.3mm

Functional Block Diagram



NSI6801M SOW8 Block Diagram

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1. Pin Configuration and Functions

Figure 1.1 NSI6801M SOW8 Top View

Table 1.1 NSI6801M Pin Configuration and Description

SYMBOL	***PIN NO.*** *NSI6801M*	***FUNCTION***
ANODE	1	Anode of LED emulator
NC	2	No Connection
CATHODE	3	Cathode of LED emulator
NRC	4	Internally connected, not recommended connecting in circuit
V_{EE}	5	Negative output supply rail
CLAMP	6	Internal Miller-Clamp pin
V_{OUT}	7	Gate-drive output
V_{CC}	8	Positive output supply rail

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit
Average Input Current	I_{F_AVG}		25	mA
Peak Transient Input Current	I_{F_PEAK}		0.2	A
Reverse Input Voltage	V_{R_MAX}		6.5	V
Driver Side Supply Voltage	V_{CC}-V_{EE}, V_{CLAMP}- V_{EE}	-0.3	35	V
Output Signal Voltage	V_{OUT}	V_{EE}-0.3	V_{CC}+0.3	V
Operating Junction Temperature	T_J	-40	150	°C
Storage Temperature	T_{stg}	-65	150	°C

3. ESD Ratings

Ratings		Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002-RevD ● All pins	±2000	V
	Charged device model (CDM), per AEC-Q100-011-RevB ● All pins	±1000	V

4. Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit
Input Current (ON)	$I_{F(ON)}$	7	16	mA
Input Voltage (OFF)	$V_{F(off)}$	-5.5	0.9	V
Driver Side Supply Voltage (NSI6801MC)	V_{CC}-V_{EE}	14	32	V
Driver Side Supply Voltage (NSI6801MB)	V_{CC}-V_{EE}	10	32	V
Ambient Temperature	T_A	-40	125	°C

5. Thermal Information

Parameters	Symbol	SOW8	Unit
Junction–to-ambient thermal resistance(1)	$R_{\theta JA}$	110	°C/W
Junction–to-top characterization parameter(2)	Ψ_{JT}	18	°C/W

1) Tested using High Effective Thermal Conductivity Test Board (2s2p) described in JESD51-7

2) Tested following the environment described in JESD51-7

6. Specifications

6.1. DC Electrical Characteristics

(Unless otherwise noted, Typical values are at V_{CC} =15V, V_{EE}=GND, T_A=25°C. All min and max specifications are at T_A=-40°C to 125°C, V_{CC}=15V to 30V, V_{EE}=GND, $I_{F(ON)}$=7 mA to 16 mA, $V_{F(off)}$= –5.5V to 0.8V)

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Condition*
Driver Side Supply						
High Level Supply Current	I_{CCH}		1.7	3	mA	I_F=10mA, I_{OUT}=0mA
Low Level Supply Current	I_{CCL}		1.6	3	mA	V_F=0V, I_{OUT}=0mA
Driver Side Supply UVLO Threshold (NSI6801MC, 12V UVLO Level)						
VCC UVLO Rising Threshold	V_{CC_ON}		12.2	13	V	I_F=10mA
VCC UVLO Falling Threshold	V_{CC_OFF}	10.3	11.2		V	
VCC UVLO Hysteresis	V_{CC_HYS}		1		V	
Driver Side Supply UVLO Threshold (NSI6801MB, 9V UVLO Level)						
VCC2 UVLO Rising Threshold	V_{CC_ON}		9.2	10	V	I_F=10mA
VCC2 UVLO Falling Threshold	V_{CC_OFF}	8	8.5		V	
VCC2 UVLO Hysteresis	V_{CC_HYS}		0.7		V	
Input Pin Characteristic						
Input Forward Threshold Current Low to High	I_{FLH}	1.5	2.7	4	mA	V_{OUT}>5V, Cg=1nF
Threshold Input Voltage High to Low	V_{FHL}	0.9			V	V_{OUT}<5V, Cg=1nF
Input Forward Voltage	V_F	1.8	2.1	2.4	V	I_F=10mA
Temp Coefficient of Input Forward Voltage	$\Delta V_F/\Delta T$		0.34		mV/°C	I_F=10mA
Input Reverse Breakdown Voltage	V_R	6.5			V	I_R=10μA
Input Capacitance	C_{IN}		17		pF	f=1MHz
Output Pin Characteristic						
High Level Output Voltage	V_{OH}	V_{CC}-0.3	V_{CC}-0.15		V	I_{OUT}=-50mA, I_F=10mA
			V_{CC}			I_{OUT}=0mA, I_F=10mA
Low Level Output Voltage	V_{OL}		30	65	mV	I_{OUT}=50mA, V_F=0V
High Level Peak Output Current	I_{OH}		5		A	V_{CC}=15V, pulse width<10μs
Low Level Peak Output Current	I_{OL}		5		A	V_{CC}=15V, pulse width<10μs
Active Miller Clamp (NSi6801M)						
Clamp Low Level Voltage	V_{LL_CLAMP}		11.2	24	mV	I_{CLAMP}=20mA,V_F=0V
Clamp Threshold Voltage	V_{CLAMP_TH}		2.1	2.3	V	Referred to V_{EE2}

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Low Level Clamp Current (Peak)	I_{LL_CLAMP}		5		A	V_F=0V, V_{CLAMP}=15V pulse
Clamp Delay Falling	T_{CD}		46		ns	
Short Circuit Clamping						
Clamping Voltage (OUT) (V_{OUT}-V_{CC})	V_{CLP_OUT}		1	1.5	V	I_{OUT}=500mA with t_{pulse}=10μs
Clamping Voltage (CLAMP) (V_{CLAMP}-V_{CC})	V_{CLP_CLAMP}		1.2	1.5	V	I_{OUT}=500mA with t_{pulse}=10μs
Active Pulldown						
Active Pulldown Voltage on CLAMP (V_{CLAMP} to V_{EE})	V_{ACTPD}		2.5		V	I_{CLAMP}=500mA , V_{CC} open

6.2. Switching Electrical Characteristics

(Unless otherwise noted, Typical values are at V_{CC} =15V, V_{EE}=GND, T_A=25°C. All min and max specifications are at T_A=-40°C to 125°C, V_{CC}=15V to 30V, V_{EE}=GND, $I_{F(ON)}$=7 mA to 16 mA, $V_{F(off)}$= −5.5V to 0.8V)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Minimum Pulse Width	t_{PWmin}		30	60	ns	
Propagation Delay	t_{pLH}	50	90	110	ns	C_{LOAD}=1nF, f=20kHz (50% Duty Cycle)
Propagation Delay	t_{pHL}	50	75	110	ns	
Pulse Width Distortion $\lvert t_{PLH}-t_{PHL}\rvert$	t_{PWD}		15	50	ns	
Output Rise Time (20% to 80%)	t_R		9	20	ns	C_{LOAD}=1nF
Output Fall Time (80% to 20%)	t_F		8	18	ns	C_{LOAD}=1nF
Common Mode Transient Immunity	CMTI	150			kV/us	Verified by design

6.3. Typical Performance characteristics

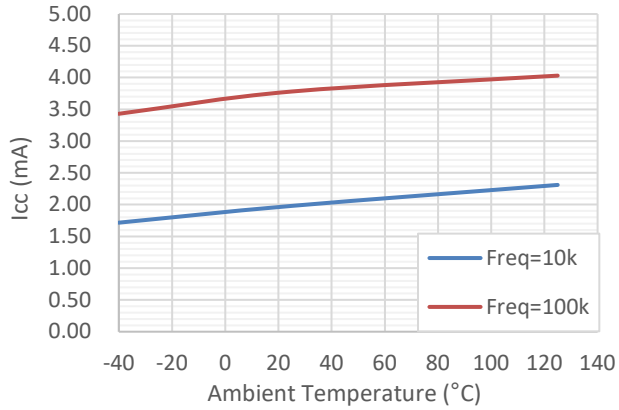


Figure 6.1 V_{CC} Operating Current versus Temperature

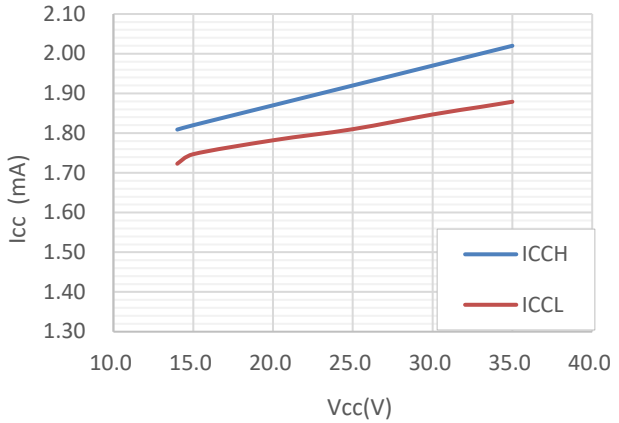


Figure 6.2 V_{CC} Quiescent Current versus Supply Voltage

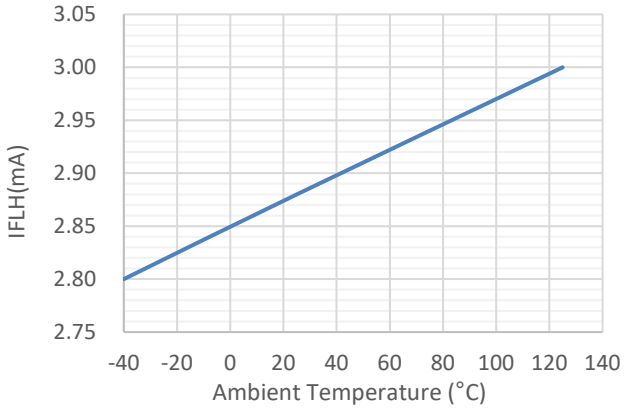


Figure 6.3 Forward Threshold Current versus Temperature

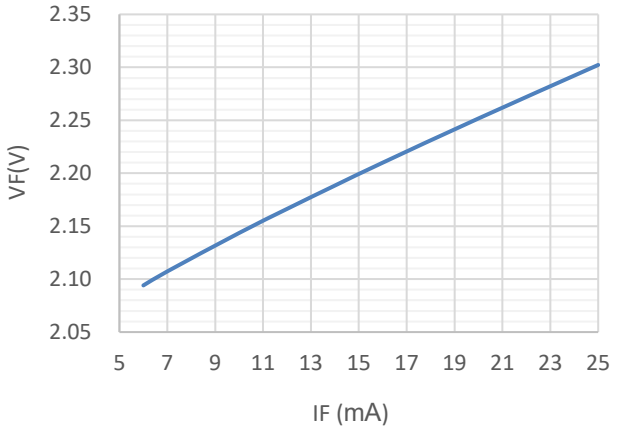


Figure 6.4 Forward Current versus Forward Voltage Drop

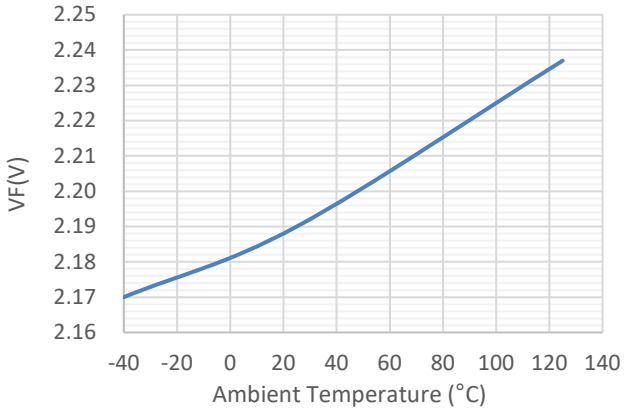


Figure 6.5 Forward voltage drop versus Temperature (I_F=10mA)

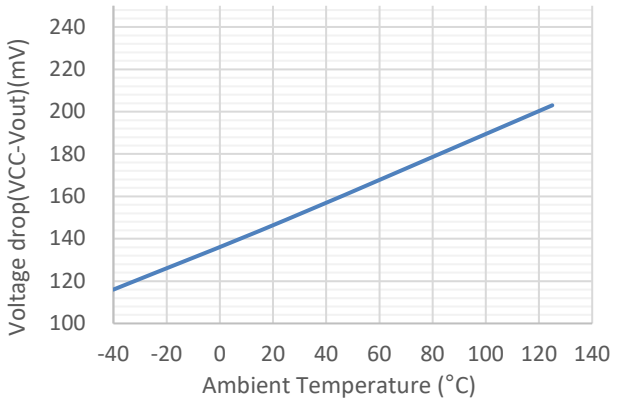


Figure 6.6 V_{OH} (50mA Load) versus Temperature

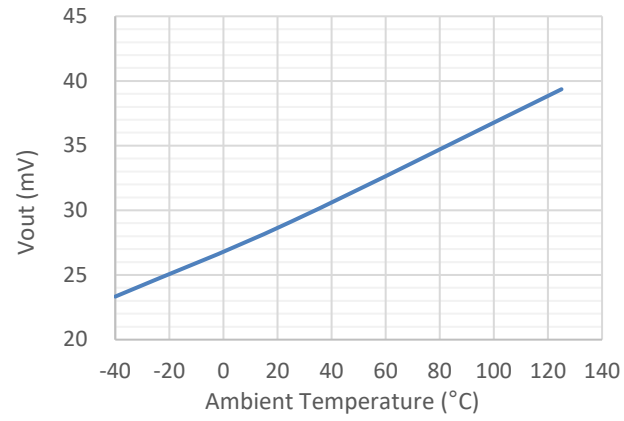


Figure 6.7 V_{OL} (50mA Load) versus Temperature

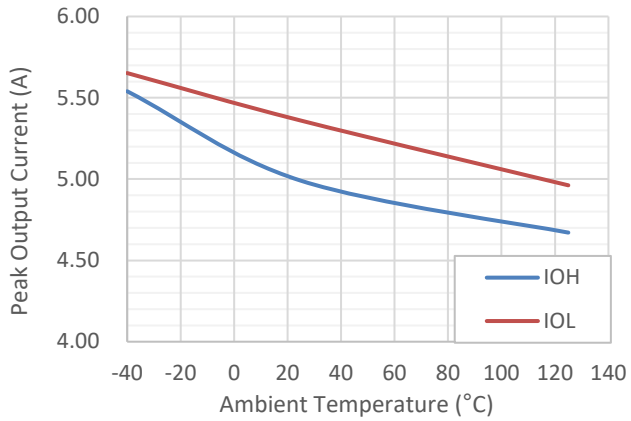


Figure 6.8 Output drive currents versus Temperature

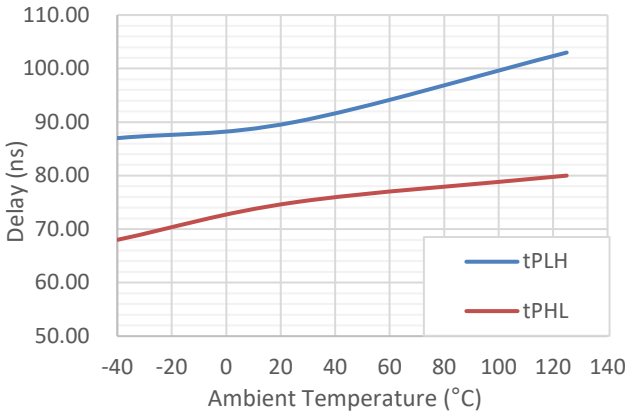


Figure 6.9 Propagation delay versus Temperature (I_F=10mA)

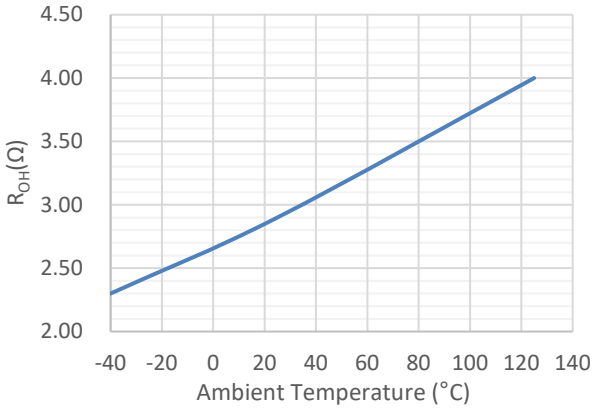


Figure 6.10 R_{OH} versus Temperature

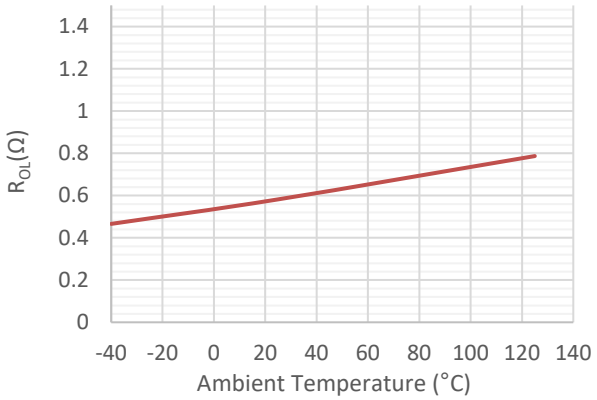


Figure 6.11 R_{OL} versus Supply voltage

6.4. Parameter Measurement Information

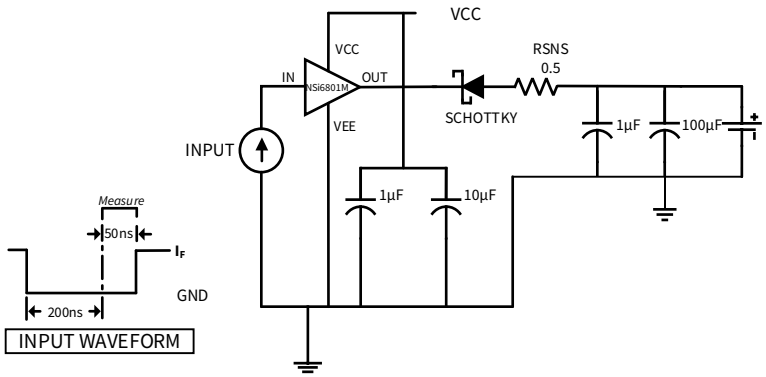


Figure 6.12 I_{OL} Sink Current Test Circuit

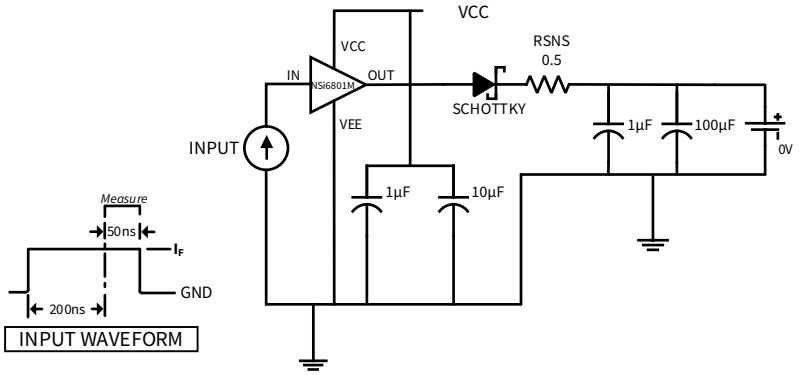


Figure 6.13 I_{OH} Source Current Test Circuit

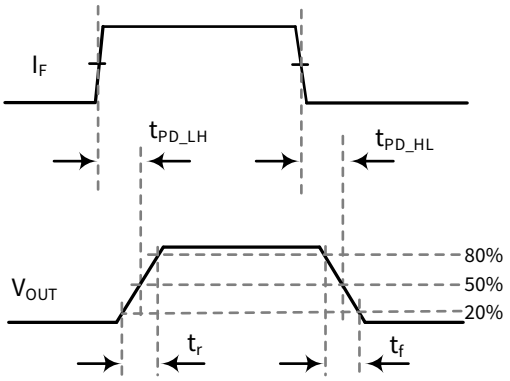


Figure 6.14 I_F to V_{OUT} Propagation Delay, Rise Time and Fall Time

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

Parameters	*Symbol*	*Value* *SOW8*	*Unit*	*Comments*
Minimum External Air Gap (Clearance)	CLR	8	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	CPG	8	mm	Shortest terminal-to-terminal distance across the package surface
Distance Through Insulation	DTI	20	um	Minimum internal gap
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	
Material Group		I		IEC 60664-1

7.2. Insulation Specification for SOW8 Package

Description	*Test Condition*	*Symbol*	*Value*	*Unit*
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 600V_{RMS}		I to III	
	For Rated Mains Voltage ≤ 1000V_{RMS}		I to II	
Climatic Category			40/125/21	
Pollution Degree			2	
DIN EN IEC 60747-17(VDE 0884-17)				
Maximum Working Isolation Voltage	AC voltage	V_{IOWM}	1500	V_{RMS}
	DC voltage		2121	V_{DC}
Maximum Repetitive Peak Isolation Voltage		V_{IORM}	2121	V_{PEAK}
Apparent Charge	Method B1,$V_{pd(m)}$=V_{IORM}×1.875, 100% production test, t_{ini}=t_m=1s	q_{pd}	<5	pC
	Method A , After Environmental Tests Subgroup 1,$V_{pd(m)}$=V_{IORM}×1.6, t_{ini}=60s, t_m=10s			pC
	Method A , After Input and Output Safety Test Subgroup 2 and Subgroup 3,$V_{pd(m)}$=V_{IORM}×1.2, t_{ini}=60s, t_m=10s, partial discharge <5pC			pC
Maximum Transient Isolation Voltage	t = 60s	V_{IOTM}	8000	V_{PEAK}
Maximum Impulse Voltage	Tested in air, 1.2/50us waveform per IEC62368-1	V_{IMP}	6000	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC62368-1,1.2/50us waveform, VIOSM⩾VIMP × 1.3	V_{IOSM}	10000	V_{PEAK}
Isolation Resistance	V_{IO}=500V at T_A=T_S=25°C	R_{IO}	>10^{12}	Ω
	V_{IO}=500V at T_A=T_S=150°C		>10^9	Ω
	V_{IO}=500V at 100°C≤T_A≤125°C		>10^{11}	Ω
Isolation Capacitance	f = 1MHz	C_{IO}	1	pF
UL1577				
Insulation voltage per UL	V_{TEST} = V_{ISO}, t = 60s (qualification),V_{TEST} = 1.2×V_{ISO},t = 1s(100% production test)	V_{ISO}	5700	V_{PEAK}

7.3. Safety-Limiting Values for SOW8 Package

Description	Test Condition	Symbol	Value		Unit
Maximum Safety Temperature		T_S	150		°C
Maximum Safety Power Dissipation	$R_{\theta JA}$=120°C/W, T_J=150°C, T_A=25°C	P_S	Total	1.04	W
			Input Side	0.05	
			Output Side	0.99	
Maximum Safety Current	$R_{\theta JA}$=120°C/W, V_{CC2}=15V, T_J=150°C, T_A=25°C	I_S	Output Side	66	mA
	$R_{\theta JA}$=120°C/W, V_{CC2}=30V, T_J=150°C, T_A=25°C		Output Side	33	

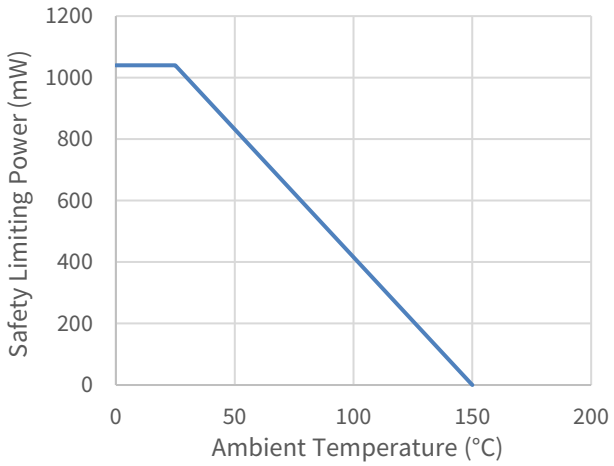


Figure 7.1 Thermal Derating Curve for Limiting Power per DIN VDE V 0884-17 for SOW8 Package

7.4. Regulatory Information for SOW8 Package

UL		*VDE*	*CQC*
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-17):2017-01	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 5700V_{RMS} Isolation Voltage	Single Protection, 5700V_{RMS} Isolation voltage	Reinforced Insulation V_{IORM}=2121V_{PEAK}, V_{IOTM}=8000V_{PEAK}, V_{IOSM}=10000V_{PEAK}	Reinforced Insulation
File (pending)	File (pending)	File (pending)	File (pending)

8. Function Description

8.1. Functional Block Diagram

The NSI6801M is a single-channel isolated gate driver which is pin-compatible for popular opto-coupled gate driver. The integrated galvanic isolation between control input logic and driving output stage grants additional safety. The device can source 5A and sink 5A peak current, which can drive IGBTs, power MOSFETs and SiC MOSFETs in many applications such as motor control systems, solar inverters and power supplies. Active pull-down and short circuit clamping features are implemented to protect power transistor.

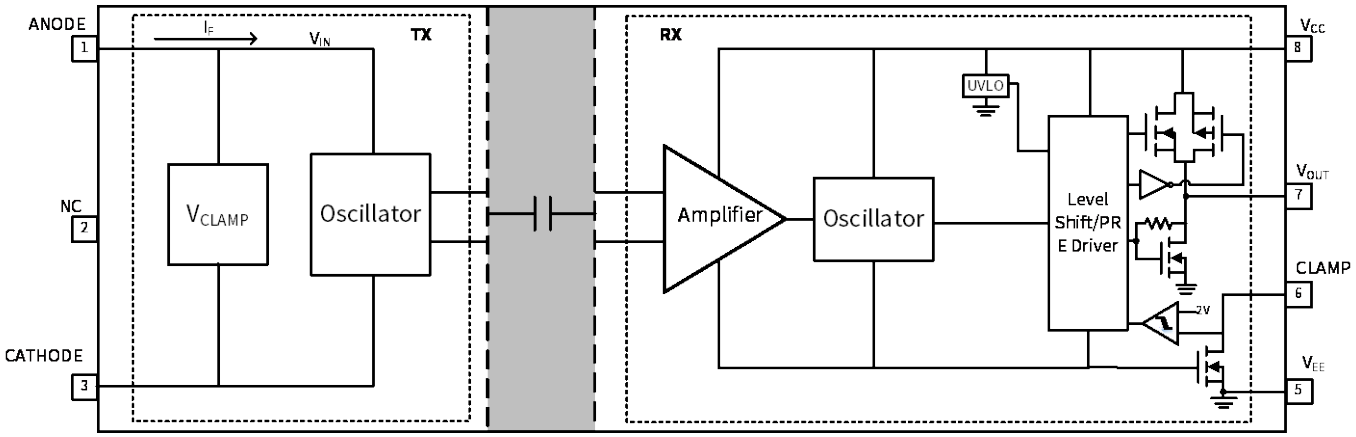


Figure 8.1 NSI6801M Functional Block Diagram

8.2. Truth Tables

Table 8.1 Driver Function Table (1)

e-diode	*V_{CC} status*	*Outputs*
X	Powered Down	L
$I_F>I_{FLH}$	Powered Up	H
$I_F<I_{FLH}$	Powered Up	L

(1) H= Logic High; L= Logic Low; X= Irrelevant

8.3. Output Stage

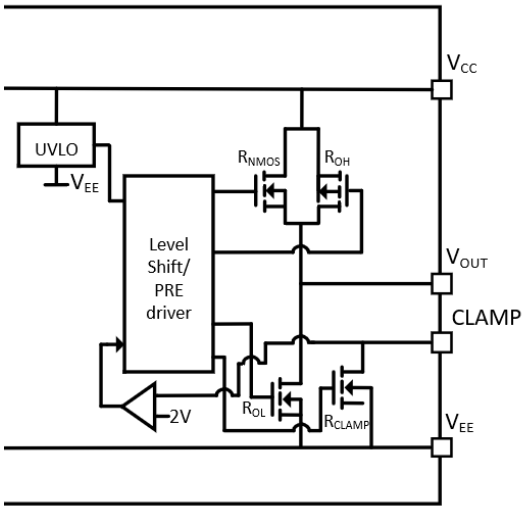


Figure 8.2 NSI6801M Output Stage

In miller-clamp output configuration as shown in Figure 8.2, the pull down structure works as two parallel N-channel MOSFETs

structure when the CLAMP and OUT pins connect to the gate of the IGBT or MOSFET.

Table 8.2 NSI6801M Output Stage On-Resistance

R_{NMOS}	R_{OH}	R_{OL}	R_{CLAMP}	Unit
0.8	3	0.6	0.6	Ω

The NSI6801M has P-channel and N-channel MOSFET in parallel to pull up the OUT pin when turning on external power transistor. During DC measurement, only the P-channel MOSFET is conducting. The measurement result R_{OH} represents the on-resistance of P-channel MOSFET.

The voltage and current of external power transistor drain to source or collector to emitter change during turn on. At that time, the NSI6801M N-channel MOSFET turns on to pull up OUT more quickly. It results external power transistor faster turn on time, lower turn on power loss, also leads to smaller temperature increase of NSI6801M. The equivalent pull-up resistance of NSI6801M is the parallel combination ROH || RNMOS. The result is quite small, indicating the strong driving capability of NSI6801M.

The pull-down structure of NSI6801M is simply composed of an N-channel MOSFET with on-resistance of R_{OL}. The result is quite small, indicating the strong driving capability of NSI6801M.

8.4. V_{CC} and Under Voltage Lock Out (UVLO)

The lower limit of driver side supply voltage (V_{CC}) is determined by the internal UVLO protection feature of the device. V_{CC} voltage should not fall below the UVLO threshold for normal operation, or else the gate-driver outputs can become clamped low.

A local bypass capacitor should be placed between the V_{CC} and V_{EE} pins, with a value of 220-nF to 10-µF for device biasing. An additional 100nF capacitor in parallel with the device biasing capacitor is recommended for high frequency filtering. Both capacitors should be positioned as close to the device as possible. Low-ESR, ceramic surface-mount capacitors are recommended.

8.5. Active Pull-Down

The Active Pull-Down feature ensures a safe IGBT or MOSFET off-state if V_{CC} is not connected to the power supply. When V_{CC} is floating, the driver output is held low and clamping V_{OUT} pin to approximately 2.5V higher than V_{EE}.

8.6. Short Circuit Clamping

During short circuit the gate voltage of IGBT or MOSFET tends to rise because of the feedback via the Miller capacitance. The diode between V_{OUT} and V_{CC} pins inside the driver limits this voltage to a value slightly higher than the supply voltage. A maximum current of 500 mA may be fed back to the supply through this path for 10 µs. If higher currents are expected or tighter clamping is desired external Schottky diodes may be added.

8.7. Active Miller Clamp

The active miller clamp function helps to prevent the false turn-on of the power switches caused by the miller current in applications such as half bridge configuration. Where switched off IGBT turns to dynamically turn-on during turn on period of the opposite IGBT. It usually happens when a unipolar power supply is used. To avoid such false turn-on of switches a miller clamp allows sinking the miller current across a low impedance path in this dv/dt situation. During turn-off the gate voltage is monitored and the power-switch gate voltage is clamped to less than 2V referred to VEE. The clamp is designed for a miller current in the same range as the nominal output current.

9. Application Note

9.1. Typical Application

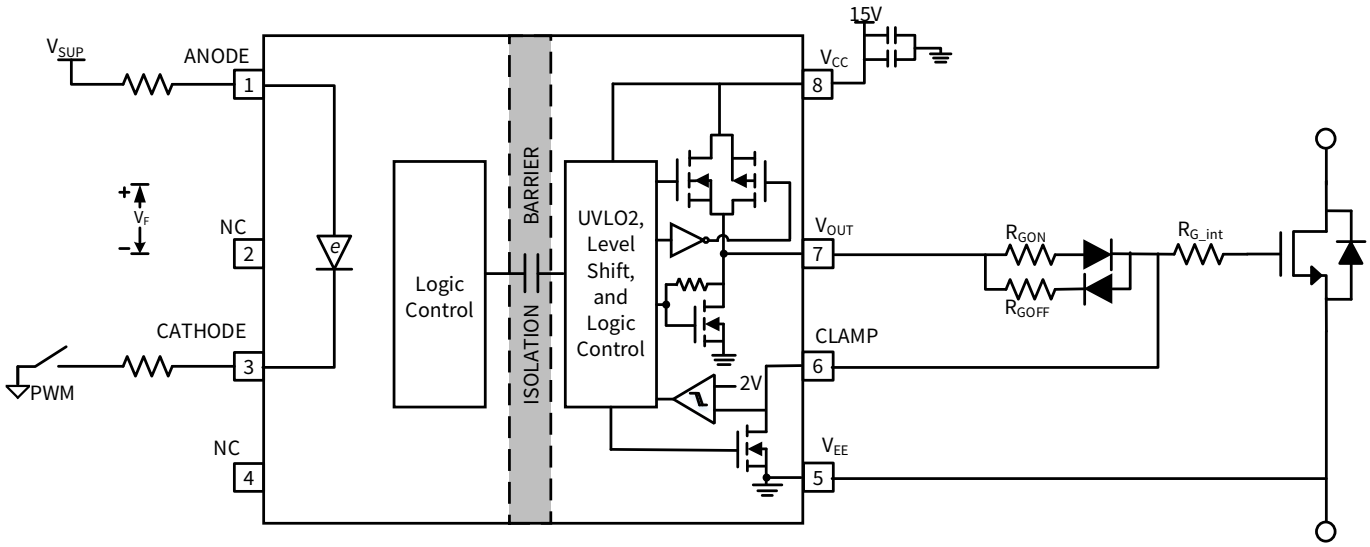


Figure 9.1 NSI6801M typical application circuit with NMOS driving input stage

Bypassing capacitors connecting between V_{CC} and V_{EE} are needed to achieve reliable performance. To filter noise, 0.1μF/50V ceramic capacitor is recommended to place as close as possible to NSI6801M. To support high peak currents when turning on external power transistor, additional 10μF/50V ceramic capacitor is recommended. If the V_{CC} power supply is located long distance from the IC, bigger capacitance is needed.

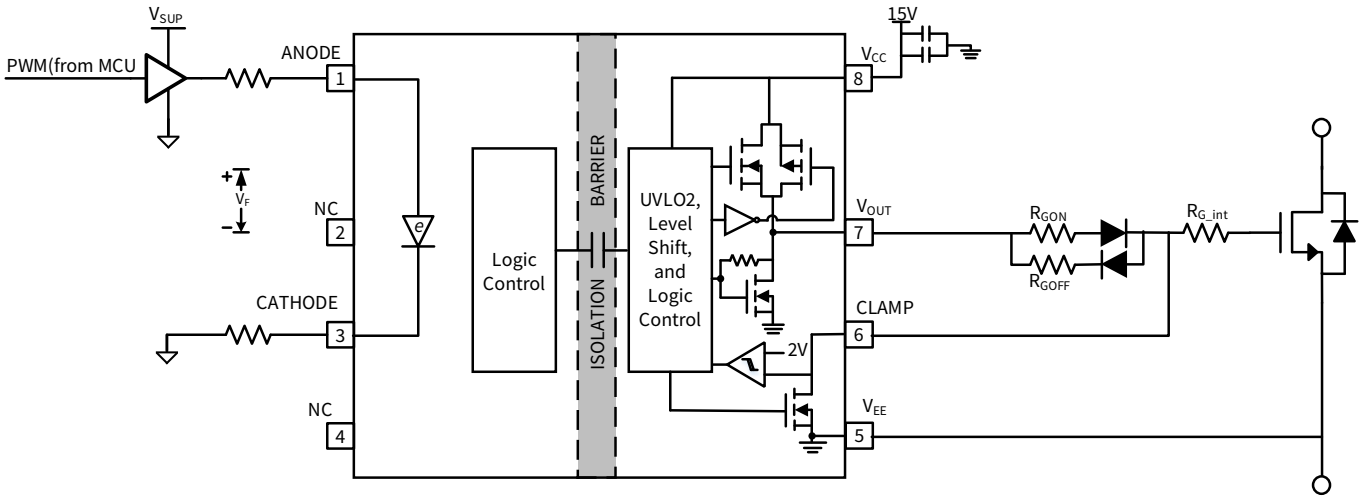


Figure 9.2 NSI6801M typical application circuit with one buffer driving input stage

NSI6801M requires 7mA to 16mA bias current that flows into the e-diode for normal operation. The PWM from MCU is not suitable to provide such current directly and external circuit is needed. In Figure 9.1, one NMOS is used with split input resistors. Another input drive method is using one buffer, as shown in Figure 9.2. The details to calculate input drive parameters are in Chapter 9.3.

9.2. Interlock Protection

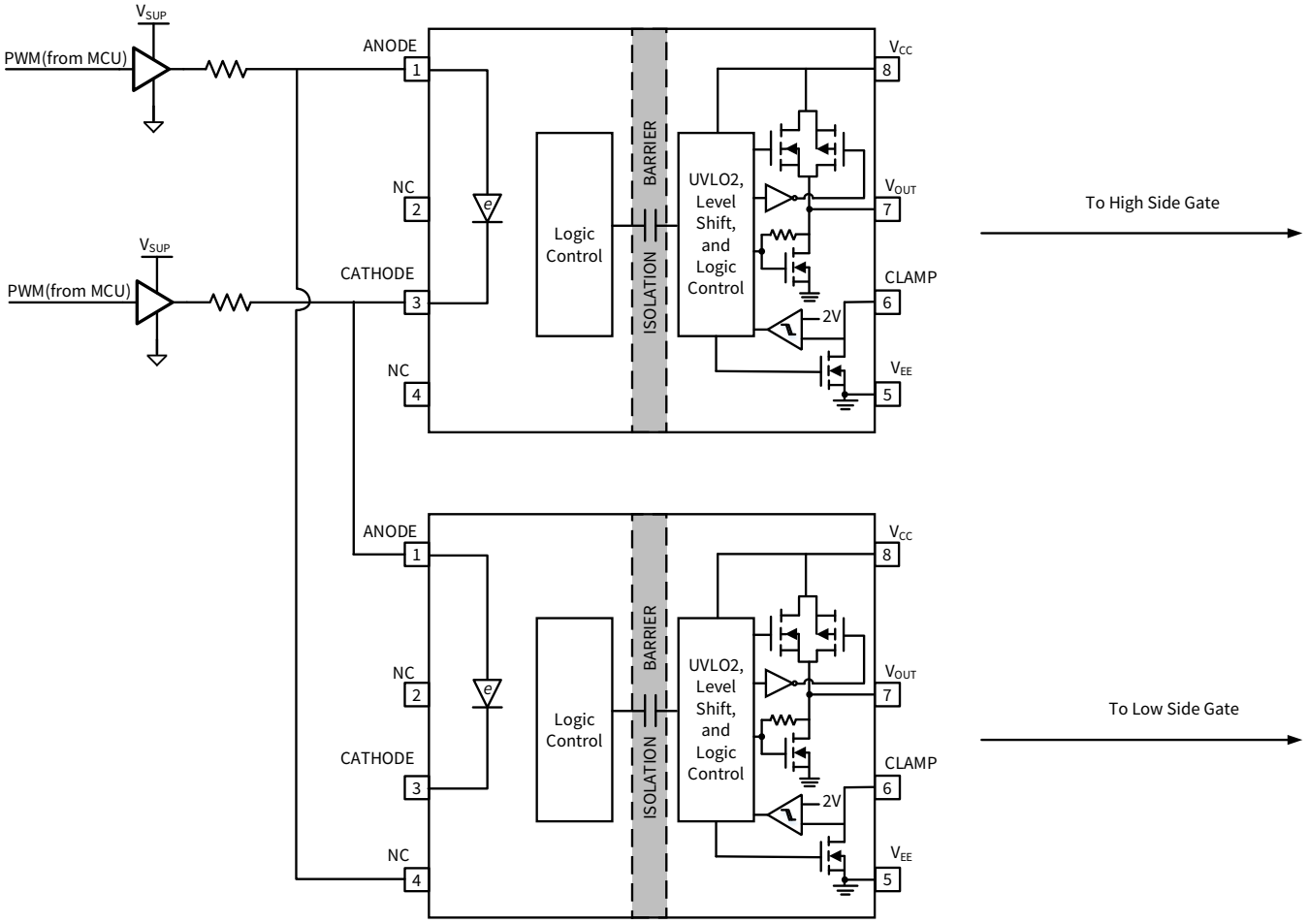


Figure 9.3 Interlock Protection using NSI6801M

For applications to drive power transistors in half bridge configuration, two NSI6801M can be used. Interlock protection is possible as shown in Figure 9.3. If the controller has some mistake, leading to negative dead time, the output PWM of NSI6801M is adjusted to avoid power transistor shoot through. The input side reverse breakdown voltage of NSI6801M is greater than 6.5V, which supports interlock protection of 3.3V or 5V PWM signal source.

9.3. Selecting Input Resistor

The recommended forward current range for NSI6801 is 7mA to 16mA. The value of input resistor, buffer supply voltage and buffer internal resistance influence the forward current, as shown in Equation (1). In Figure 9.1, R_{IN1} is the on-resistance of the external NMOS. In Figure 9.2, R_{IN2} is the buffer output impedance in output "High" state. In Figure 9.3, R_{IN3} is the summary of buffer output impedance in "High" and "Low" state.

$$R_{EXT} = \frac{V_{SUP}-V_F}{I_F} - R_{INx} \quad (1)$$

The parameter variation needs to be taken into consideration when selecting input resistor. Table 9.1 lists parameter variation in this example. Manufacturer's tolerance for R_{EXT} is 2%.

Table 9.1 External parameters range when calculating input resistor

Parameters	*Min*	*Typ*	*Max*
NSI6801 forward current I_F	7mA	10mA	16mA
NSI6801 forward voltage V_F	1.8V	2.1V	2.4V
Buffer supply voltage V_{SUP}	5V*95%	5V	5V*105%

R_{IN1}	0.25Ω	/	1Ω
R_{IN2}	12Ω	18Ω	23Ω
R_{IN3}	9Ω	14Ω	18Ω

R_{EXT} caculated based on these parameters above is as follows:

$$R_{EXT\_min} = \left(\frac{V_{SUP\_max}-V_{F\_min}}{I_{F\_max}} - R_{INx\_min}\right)/(1-2\%) \quad (2)$$

$$R_{EXT\_typ} = \frac{V_{SUP\_typ}-V_{F\_typ}}{I_{F\_typ}} - R_{INx\_typ} \quad (3)$$

$$R_{EXT\_max} = \left(\frac{V_{SUP\_min}-V_{F\_max}}{I_{F\_min}} - R_{INx\_max}\right)/(1+2\%) \quad (4)$$

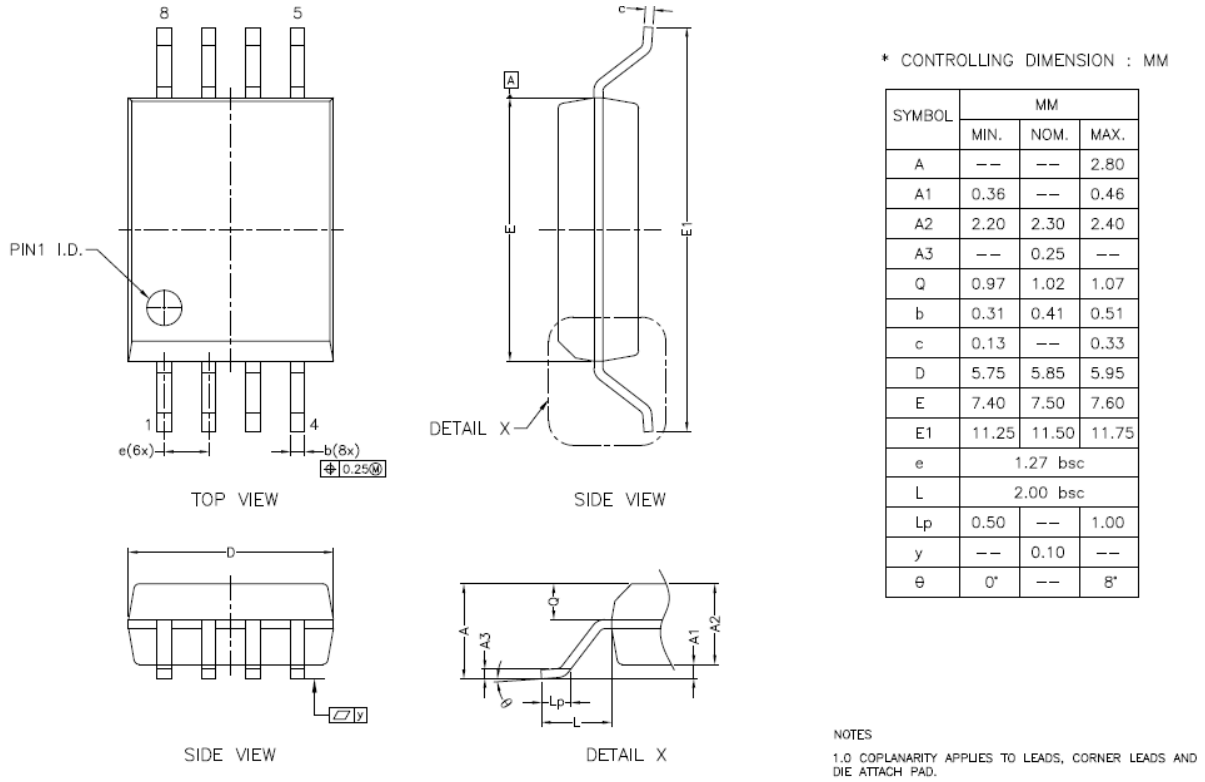
Where R_{INx}=R_{IN1} or R_{IN2} or R_{IN3} is determined by topology.

9.4. PCB Layout

Carful PCB layout is essential for optimal performance. Some key guidelines are:

- The bypass capacitors should be placed close to NSI6801M, between V_{CC} to V_{EE}.
- There is high switching current that charges and discharges the gate of external power transistor, leading to EMI and ring issues. The parasitic inductance of this loop should be minimized, by decreasing loop area and place NSI6801M close to power transistor.
- Place large amount of copper connecting to V_{EE} pin and V_{CC} pin for thermal dissipation, with priority on V_{EE} pin. If the system has multi V_{EE} or V_{CC} layers, use multiple vias of adequate size for connection.
- To ensure isolation performance between primary and secondary side, the space under the chip should keep free from planes, traces, pads or via.

10. Package Information



SYMBOL	MM		
	MIN.	NOM.	MAX.
A	--	--	2.80
A1	0.36	--	0.46
A2	2.20	2.30	2.40
A3	--	0.25	--
Q	0.97	1.02	1.07
b	0.31	0.41	0.51
c	0.13	--	0.33
D	5.75	5.85	5.95
E	7.40	7.50	7.60
E1	11.25	11.50	11.75
e	1.27 bsc		
L	2.00 bsc		
Lp	0.50	--	1.00
y	--	0.10	--
θ	0°	--	8°

NOTES
1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

Figure 10.1 SOW8 Package Shape and Dimension in millimeters

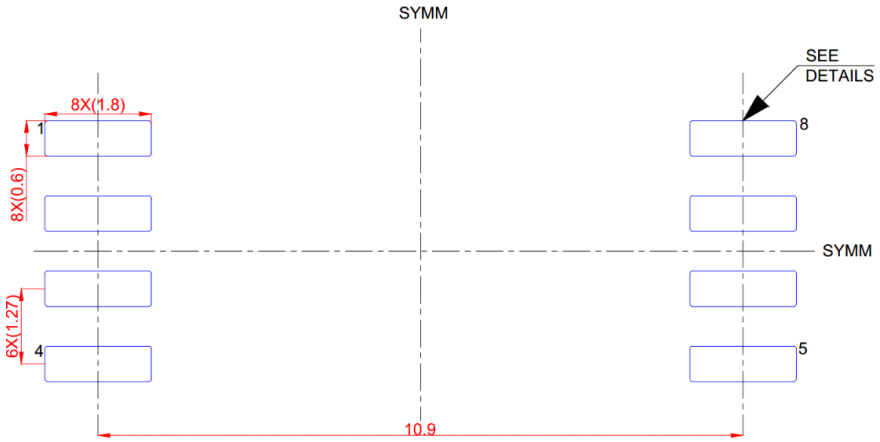


Figure 10.2 Land Pattern Example of SOW8_300mil

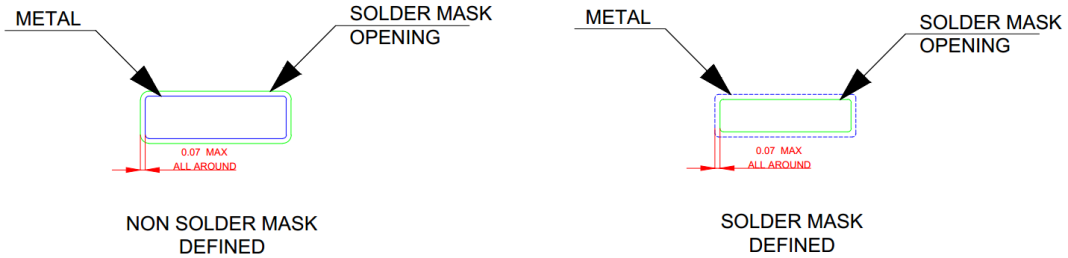
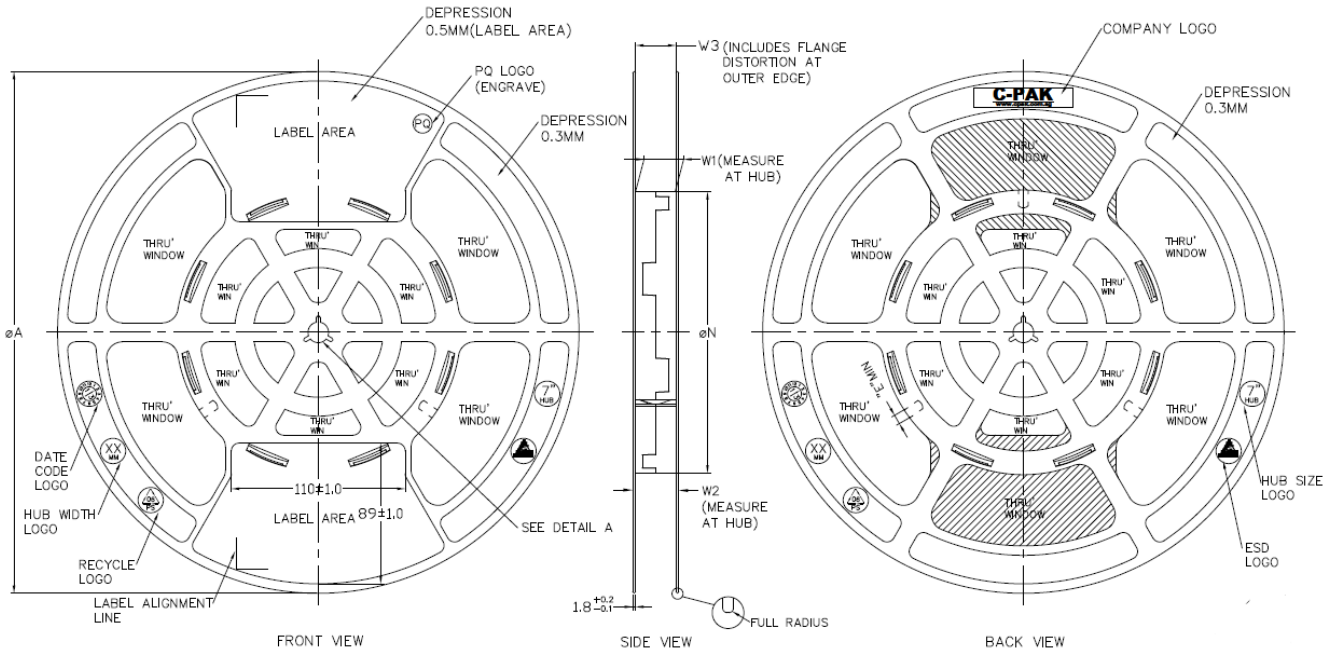


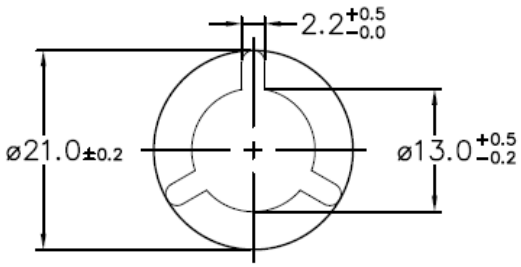
Figure 10.3 Solder Mask Detail of SOW8_300mil

11. Ordering Information

Part Number	*Isolation Rating (kV)*	*UVLO Level*	*Temperature*	*MSL*	*Package Drawing*	*SPQ*	*Category*
NSI6801MB-DSWVR	5.7	9V	-40 to 125°C	3	SOW8	1000	Industrial
NSI6801MC-DSWVR	5.7	12V	-40 to 125°C	3	SOW8	1000	Industrial

12. Tape and Reel Information



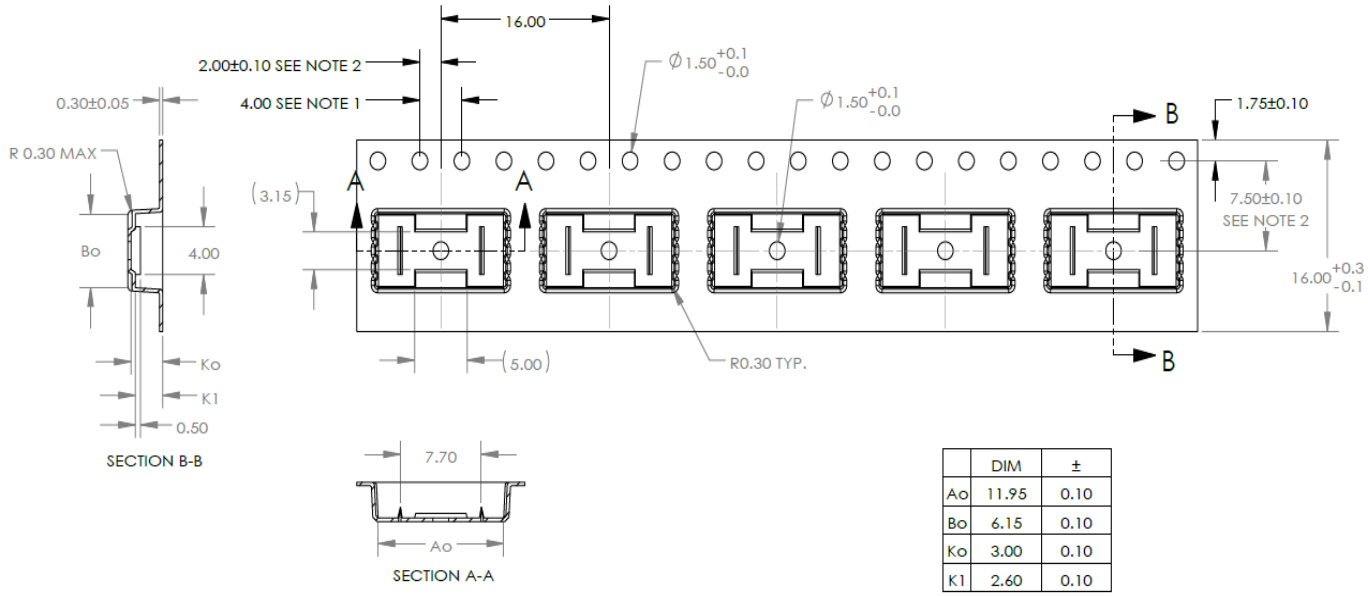


ARBOR HOLE
DETAIL A
SCALE : 3:1

PRODUCT SPECIFICATION						
TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4	18.4		5.5
16MM	330	178	16.4	22.4		5.5
24MM	330	178	24.4	30.4		5.5
32MM	330	178	32.4	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES

Figure 12.1 Tape Information



	DIM	±
Ao	11.95	0.10
Bo	6.15	0.10
Ko	3.00	0.10
K1	2.60	0.10

NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE.
3. Ao AND Bo ARE MEASURED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.

S

Figure 12.2 Reel Information of SOW8

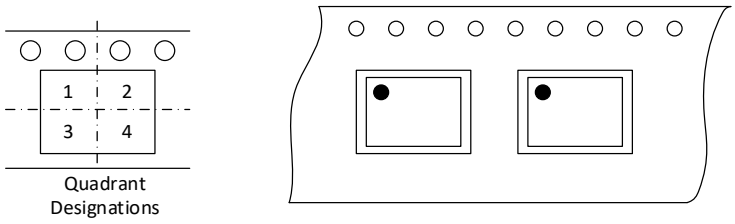


Figure 12.3 Quadrant Designation for Pin1 Orientation in Tape

13. Revision History

Revision	Description	Date
1.0	Initial version	2024/1/10

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