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1. Pin Configuration and Functions

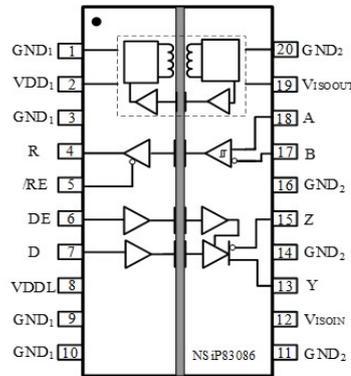


Figure 1.1 NSiP83086(V)-DSWTR Package

Table1.1 NSiP83086(V)-DSWTR Pin Configuration and Description

PIN NO.	SYMBOL	FUNCTION
1	GND ₁	Ground 1, the ground reference for Isolator Side 1
2	VDD ₁	Power Supply for Isolator Side 1, It is recommended this pin have a 0.1μF + 10 μF capacitor to GND ₁ (Pin1, Pin3)
3	GND ₁	Ground 1, the ground reference for Isolator Side 1
4	R	Receiver output
5	/RE	Receiver enable input, this is an active low input
6	DE	Driver enable input, this is an active high input
7	D	Driver transmit data input
8	VDDL	I/O Power Supply input, Side1 I/O logic level
9	GND ₁	Ground 1, the ground reference for Isolator Side 1
10	GND ₁	Ground 1, the ground reference for Isolator Side 1
11	GND ₂	Ground 2, the ground reference for Isolator Side 2
12	VISOIN	Isolated power supply input. This pin must be connected externally to VISOOUT. It is recommended this pin have a 0.1 μF capacitor to GND ₂ (Pin11). Connect this pin to VISOOUT through a ferrite bead and short trace length for operation.
13	Y	Non-inverting Driver Output. When the driver is disabled, or when VDDL is powered down, Pin Y is put into a high impedance state to avoid overloading the bus.
14	GND ₂	Ground 2, the ground reference for Isolator Side 2
15	Z	Inverting Driver Output. When the driver is disabled, or when VDD is powered down, Pin Z is put into a high impedance state to avoid overloading the bus.
16	GND ₂	Ground 2, the ground reference for Isolator Side 2
17	B	Inverting Receiver Input

18	A	Non-inverting Receiver Input
19	V _{ISOOUT}	Isolated Power Supply Output. This pin must be connected externally to V _{ISOIN} . It is recommended this pin have a 0.1 μF and 10μF capacitor to GND ₂ (Pin20). Connect this pin through a ferrite bead and short trace length to V _{ISOIN} for operation.
20	GND ₂	Ground 2, the ground reference for Isolator Side 2

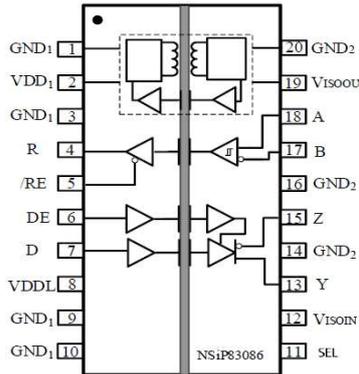


Figure 1.2 NSiP83086C-DSWTR Package

Table1.2NSiP83086C-DSWTR Pin Configuration and Description

PIN NO.	SYMBOL	FUNCTION
1	GND ₁	Ground 1, the ground reference for Isolator Side 1
2	VDD ₁	Power Supply for Isolator Side 1, It is recommended this pin have a 0.1μF + 10 μF capacitor to GND ₁ (Pin1, Pin3)
3	GND ₁	Ground 1, the ground reference for Isolator Side 1
4	R	Receiver output
5	/RE	Receiver enable input, this is an active low input
6	DE	Driver enable input, this is an active high input
7	D	Driver transmit data input
8	VDDL	I/O Power Supply input, Side1 I/O logic level
9	GND ₁	Ground 1, the ground reference for Isolator Side 1
10	GND ₁	Ground 1, the ground reference for Isolator Side 1
11	SEL	VISO output voltage select, V _{ISOOUT} =5V when SEL is floating or connect to V _{ISOIN} , V _{ISOOUT} =3.3V when SEL short to GND ₂
12	V _{ISOIN}	Isolated power supply Input. This pin must be connected externally to V _{ISOOUT} . It is recommended this pin have a 0.1 μF capacitor to GND ₂ . Connect this pin to V _{ISOOUT} through a ferrite bead and short trace length for operation.
13	Y	Non-inverting Driver Output. When the driver is disabled, or when VDDL is powered down, Pin Y is put into a high impedance state to avoid overloading the bus.
14	GND ₂	Ground 2, the ground reference for Isolator Side 2

15	Z	Inverting Driver Output. When the driver is disabled, or when VDD is powered down, Pin Z is put into a high impedance state to avoid overloading the bus.
16	GND ₂	Ground 2, the ground reference for Isolator Side 2
17	B	Inverting Receiver Input
18	A	Non-inverting Receiver Input
19	V _{ISOOUT}	Isolated Power Supply Output. This pin must be connected externally to V _{ISOIN} . It is recommended this pin have a 0.1 μF and 10μF capacitor to GND ₂ (Pin20). Connect this pin through a ferrite bead and short trace length to V _{ISOIN} for operation.
20	GND ₂	Ground 2, the ground reference for Isolator Side 2

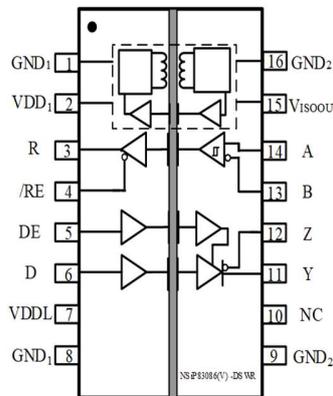


Figure 1.3 NSiP83086(V)-DSWR Package

Table1.3NSiP83086(V)-DSWR Pin Configuration and Description

PIN NO.	SYMBOL	FUNCTION
1	GND ₁	Ground 1, the ground reference for Isolator Side 1
2	VDD ₁	Power Supply for Isolator Side 1. It is recommended this pin have a 0.1 μF + 10 μF capacitor to GND ₁ (Pin1)
3	R	Receiver output
4	/RE	Receiver enable input, this is an active low input
5	DE	Driver enable input, this is an active high input
6	D	Driver transmit data input
7	VDDL	I/O Power Supply input, Side1 I/O logic level
8	GND ₁	Ground 1, the ground reference for Isolator Side 1
9	GND ₂	Ground 2, the ground reference for Isolator Side 2
10	NC	Not Connected
11	Y	Non-inverting Driver Output. When the driver is disabled, or when VDD is powered down, Pin Y is put into a high impedance state to avoid overloading the bus.
12	Z	Inverting Driver Output. When the driver is disabled, or when VDD is powered down, Pin Z is put

		into a high impedance state to avoid overloading the bus.
13	B	Inverting Receiver Input
14	A	Non-inverting Receiver Input
15	V _{ISOOUT}	Isolated Power Supply Output. It is recommended this pin have a 0.1 μ F and 10 μ F capacitor to GND ₂ (Pin16).
16	GND ₂	Ground 2, the ground reference for Isolator Side 2.

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD, VDDL	-0.5		6	V	
Maximum Input Voltage	/RE, DE, D	-0.4		VDDL+0.4	V	
Driver Output/Receiver Input Voltage	V _A , V _B , V _Y , V _Z	-7		12	V	
R output current	I _O	-15		15	mA	
Operating Temperature	T _{OPR}	-40		105	°C	
Junction Temperature	T _J	-40		150	°C	
Storage Temperature	T _{STG}	-40		150	°C	
Electrostatic discharge	HBM			±8000	V	
	CDM			±2000	V	

3. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
NSiP83086 Power Supply Voltage	VDD	4.5	5	5.5	V
NSiP83086C and NSiP83086V Power Supply Voltage	VDD	3	3.3/5	5.5	V
Operating Temperature	Topr	-40		105	°C
Side1 High Level Input Voltage	V _{IH}	0.7*VDDL		VDDL	V
Side1 Low Level Input Voltage	V _{IL}	0		0.3*VDDL	V
Data rate	DR			16	Mbps

4. Thermal Information

Parameters	Symbol	SOW20	SOW16	Unit
IC Junction-to-Air Thermal Resistance	θ _{JA}	51.8	51.5	°C/W
Junction-to-top characterization parameter	ψ _{JT}	2.6	2.6	°C/W
Junction-to-board characterization parameter	ψ _{JB}	20.1	17.8	°C/W

5. Specifications

5.1. DC Electrical Characteristics

(VDD=4.5V~5.5V, VDDL=1.8~5.5V, Ta=-40°C to 105°C. Unless otherwise noted, Typical values are at VDD=VDDL=5V, V_{ISOOUT}=5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power supply voltage NSiP83086	VDD ₁	4.5		5.5	V	
	VDDL	1.8		5.5	V	
Power supply voltage NSiP83086C/NSiP83086V	VDD ₁	3		5.5	V	
	VDDL	1.8		5.5	V	
Supply current V _{ISOOUT} = 5V	IDD (500kbps)		72	90	mA	R _L =120 Ω
			118	150	mA	R _L =54 Ω
	IDD (16Mbps)		100	130	mA	R _L =120 Ω
			130	160	mA	R _L =54 Ω
IDD _L			5	mA		
Supply current 3V ≤ VDD ≤ 3.6 V V _{ISOOUT} = 3.3V	IDD (500kbps)		49	72	mA	R _L =120 Ω
			78	103	mA	R _L =54 Ω
	IDD (16Mbps)		58	83	mA	R _L =120 Ω
			75	101	mA	R _L =54 Ω
IDD _L			5	mA		
Supply current 4.5V ≤ VDD ≤ 5.5 V V _{ISOOUT} = 3.3V	IDD (500kbps)		40	61	mA	R _L =120 Ω
			61	84	mA	R _L =54 Ω
	IDD (16Mbps)		45	69	mA	R _L =120 Ω
			60	83	mA	R _L =54 Ω
IDD _L			5	mA		
Isolated supply voltage	V _{ISOOUT}		5		V	NSiP83086
	V _{ISOOUT}		3.3/5		V	NSiP83086C
	V _{ISOOUT}		3.3		V	NSiP83086V
Thermal-Shutdown Threshold	T _{TS}		165		°C	
Thermal-Shutdown Hysteresis	T _{TSH}		15		°C	
Common Mode Transient Immunity	CMTI	100	150		kV/us	Figure 5.14

Side1						
Input High Voltage	V_{IH}	0.7*VDDL			V	DE, D, /RE
Input Low Voltage	V_{IL}			0.3*VDDL	V	DE, D, /RE
Input Current	I_I	-20		20	uA	D, DE, /RE
Output Voltage High	V_{OH}	0.8*VDDL			V	IOH = -4mA
Output Voltage Low	V_{OL}			0.2*VDDL	V	IOL = 4mA
Output Short-Circuit Current	I_{OSR}			150	mA	$0 \leq V_R \leq VDDL$
Three-State Output Current	I_{OZR}			15	uA	$0 \leq V_R \leq VDDL$, /RE = high
Input Capacitance	C_{IN}		2		pF	DE, D, /RE
Driver						
Differential Output Voltage	$ V_{OD} $			5.5	V	No Load, $V_{ISOOUT}=5V$
		2.7		5.5	V	Figure 5.9 , $R_L=120\Omega$, $V_{ISOOUT}=5V$
		2.1		5.5	V	Figure 5.9 , $R_L=54\Omega$, $V_{ISOOUT}=5V$
				3.3		No Load, $V_{ISOOUT}=3.3V$
		1.8				Figure 5.9 , $R_L=120\Omega$, $V_{ISOOUT}=3.3V$
		1.5				Figure 5.9 , $R_L=54\Omega$, $V_{ISOOUT}=3.3V$
Change in magnitude of the differential output voltage	$\Delta V_{OD} $			0.2	V	Figure 5.9 , $R_L=120\Omega$ or $R_L=54\Omega$
Common-Mode Output Voltage	$ V_{OC} $			3	V	Figure 5.9 , $R_L=120\Omega$ or $R_L=54\Omega$
Change in Magnitude of Common-Mode Voltage	$\Delta V_{OC} $			0.2	V	Figure 5.9 , $R_L=120\Omega$ or $R_L=54\Omega$
Driver Short-Circuit Output Current	I_{OSD}			200	mA	$0 \leq V_{Test} \leq 12V$
		-200			mA	$-7V \leq V_{Test} \leq 0V$
Output Leakage Current (Y and Z) Full-Duplex	I_o			200	uA	DE=0V, $V_{Test}=12V$
		-200			uA	DE=0V, $V_{Test}=-7V$
Receiver						
Input Current (A and B)	I_A, I_B			200	uA	DE=0V, $V_{ISOIN}=0V$, $V_{Test}=12V$
		-200			uA	DE=0V, $V_{ISOIN}=0V$, $V_{Test}=-7V$
Receiver Differential Threshold Voltage	V_{TH}	-200	-125	-10	mV	$V_{CM}=0V$
Receiver Input Hysteresis	ΔV_{TH}		15		mV	$V_{CM}=0V$
Receiver Input Resistance	R_{IN}	96			k Ω	$-7V \leq V_{CM} \leq 12V$, DE=0V

5.2. Switching Electrical Characteristics

(VDD=3V~5.5V, VDDL=1.8~5.5V, Ta=-40°C to 105°C. Unless otherwise noted, Typical values are at VDD=VDDL = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Driver						
Maximum Data Rate	f _{MAX}			16	Mbps	
Driver Propagation Delay	t _{PLH}		22	60	ns	Figure 5.10 , R _L =54Ω, C _L =50pF
	t _{PHL}		21	60	ns	Figure 5.10 , R _L =54Ω, C _L =50pF
Driver Pulse Width Distortion, t _{PHL} - t _{PLH}	t _{skew}		1	8	ns	Figure 5.10 , R _L =54Ω, C _L =50pF
Driver Output Falling Time or Rising time	t _F			15	ns	Figure 5.10 , R _L =54Ω, C _L =50pF
	t _R			15	ns	Figure 5.10 , R _L =54Ω, C _L =50pF
Driver Enable to Output High	t _{ZH}		22.8	50	ns	Figure 5.11 , R _L =120Ω, C _L =50pF
Driver Enable to Output Low	t _{ZL}		19.1	50	ns	Figure 5.11 , R _L =120Ω, C _L =50pF
Driver Disable to Output High	t _{HZ}		28	50	ns	Figure 5.11 , R _L =120Ω, C _L =50pF
Driver Disable to Output Low	t _{LZ}		27.1	50	ns	Figure 5.11 , R _L =120Ω, C _L =50pF
Receiver						
Maximum Data Rate	f _{MAX}	16			Mbps	
Receiver Propagation Delay	t _{PLH}		65.8	140	ns	Figure 5.12 , C _L =15pF
	t _{PHL}		71.4	140	ns	Figure 5.12 , C _L =15pF
Receiver Pulse Width Distortion, t _{PHL} - t _{PLH}	t _{skew}		5.6	12	ns	Figure 5.12 , C _L =15pF
Receiver Output Falling Time or Rising time	t _F			15	ns	Figure 5.12 , C _L =15pF
	t _R			15	ns	Figure 5.12 , C _L =15pF
Receiver Enable to Output High	t _{ZH}		6	15	ns	Figure 5.13 , R _L =1kΩ, C _L =15pF
Receiver Enable to Output Low	t _{ZL}		6	15	ns	Figure 5.13 , R _L =1kΩ, C _L =15pF

Receiver Disable to Output High	t_{HZ}		8	15	ns	Figure 5.13, $R_L=1k\Omega, C_L=15pF$
Receiver Disable to Output Low	t_{LZ}		8	15	ns	Figure 5.13, $R_L=1k\Omega,$ $C_L=15pF$

5.3. Typical Performance Characteristics

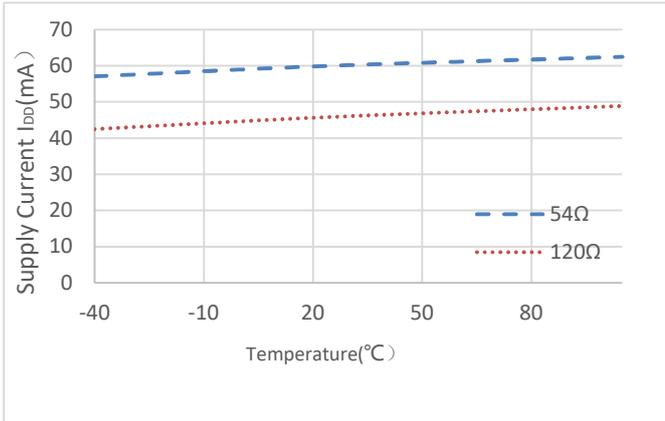


Figure 5.1 supply current vs Temperature
(Data Rate=16MHz, DE=VDDL, /RE=GND, VDD=5V, $V_{ISOOOUT}=3.3V$)

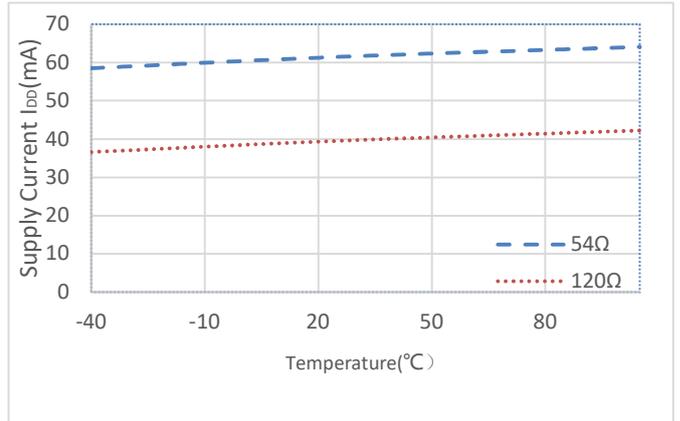


Figure 5.2 supply current vs Temperature
(Data Rate=500KHz, DE=VDDL, /RE=GND, VDD=5V, $V_{ISOOOUT}=3.3V$)

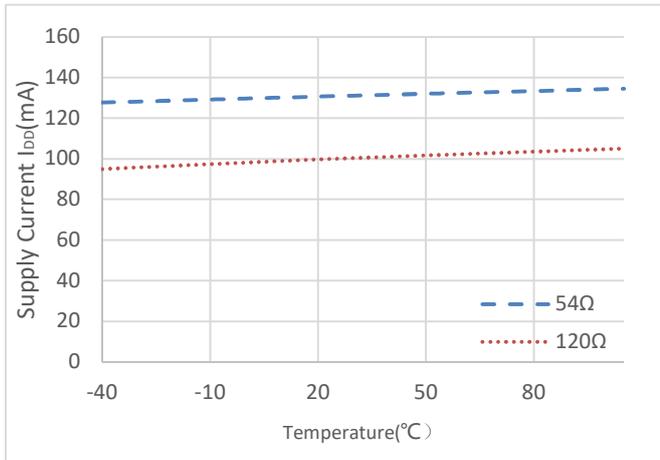


Figure 5.3 supply current vs Temperature
(Data Rate=16MHz, DE=VDDL, /RE=GND, VDD=5V, $V_{ISOOOUT}=5V$)

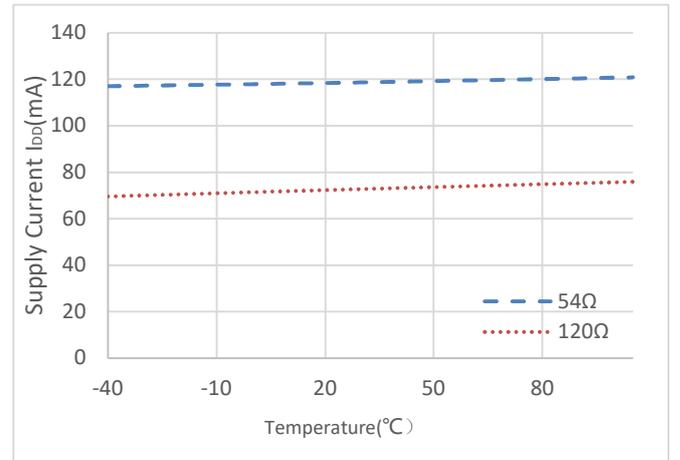


Figure 5.4 supply current vs Temperature
(Data Rate=500KHz, DE=VDDL, /RE=GND, VDD=5V, $V_{ISOOOUT}=5V$)

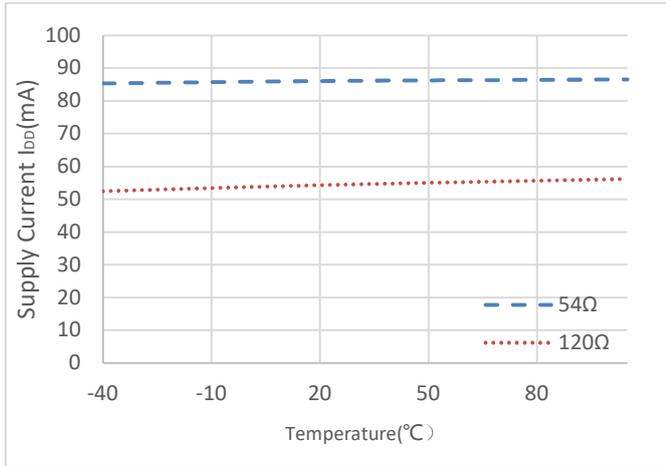


Figure 5.5 supply current vs Temperature
(Data Rate=16MHz,DE=VDDL,/RE=GND,VDD=3.3V,V_{ISOOUT}=3.3V)

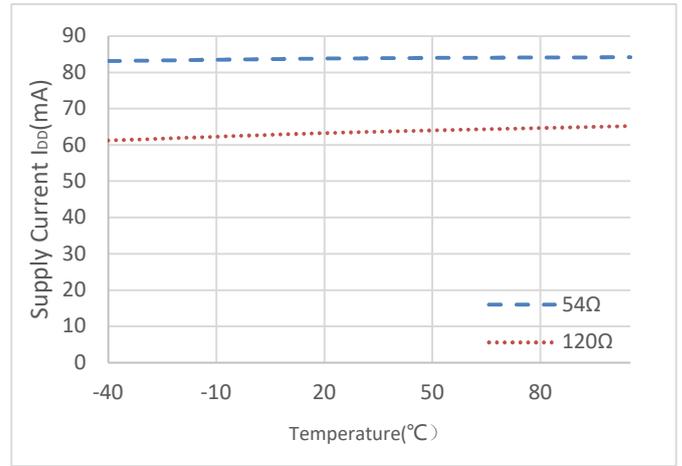


Figure 5.6 supply current vs Temperature
(Data Rate=500KHz,DE=VDDL,/RE=GND,VDD=3.3V,V_{ISOOUT}=3.3V)

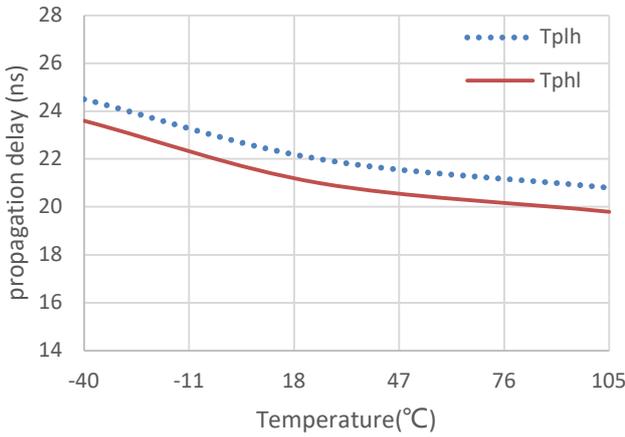


Figure 5.7 Driver Propagation Delay vs Temperature

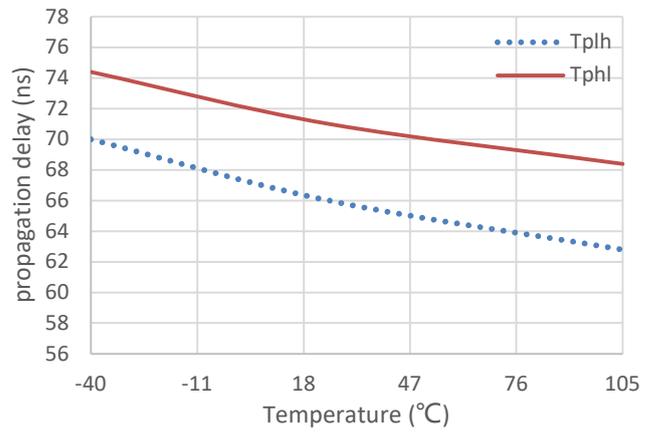


Figure 5.8 Receiver Propagation Delay vs Temperature

5.4. Parameter Measurement Information

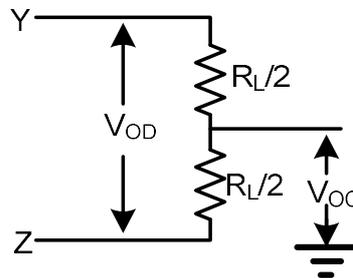


Figure 5.9 Driver DC Test Load

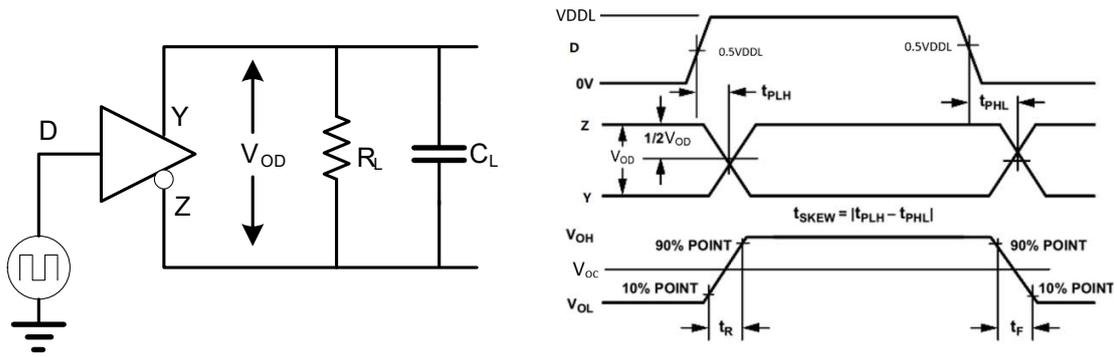


Figure 5.10 Driver Timing Test Circuit and waveform

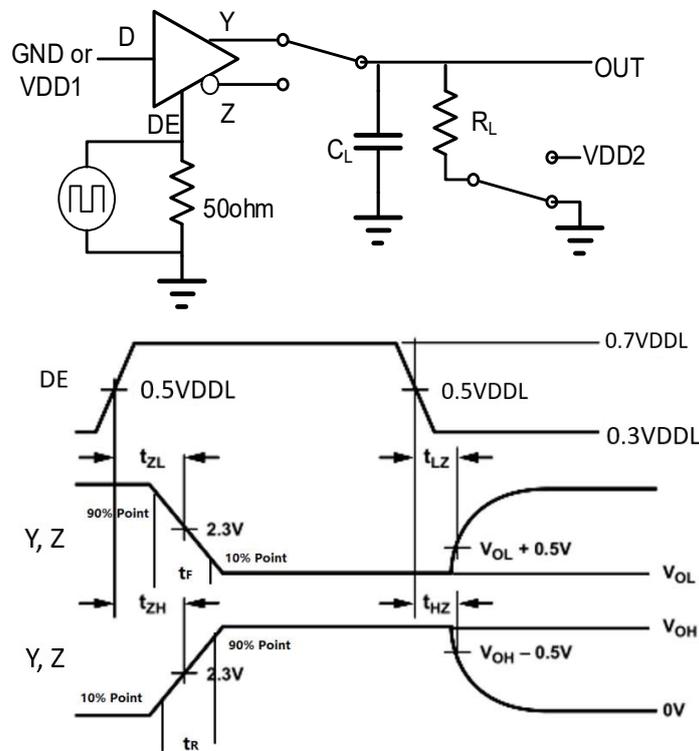


Figure 5.11 Driver Enable Disable Timing Test Circuit and waveform

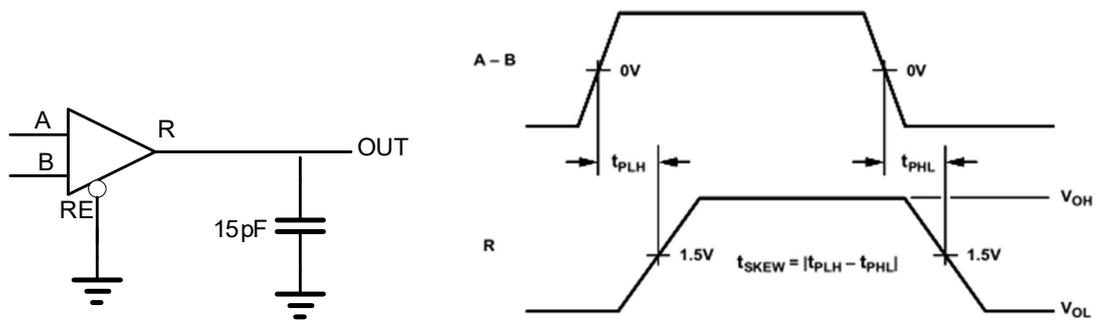


Figure 5.12 Receiver Propagation Delay Test Circuit and waveform

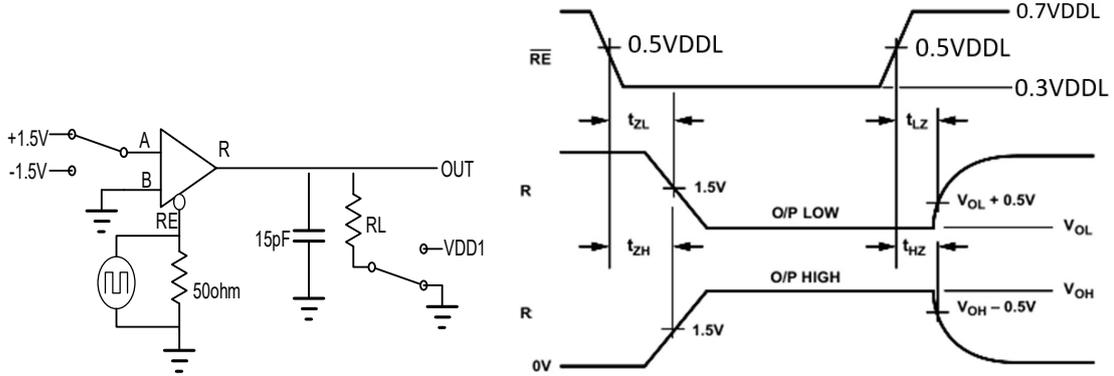


Figure 5.13 Receiver Enable Disable Timing Test Circuit and waveform

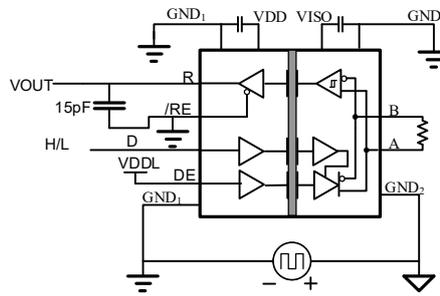


Figure 5.14 Common-Mode Transient Immunity Test Circuit

6. High Voltage Feature Description

6.1. Insulation and Safety Related Specifications

Parameters	Symbol	Value	Unit	Comments
Minimum External Air Gap (Clearance)	CLR	8.0	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	CPG	8.0	mm	Shortest terminal-to-terminal distance across the package surface
Distance through the insulation	DTI	16	um	Minimum internal gap (internal clearance – capacitive signal isolation)
		100	um	Minimum internal gap (internal clearance – transformer power isolation)
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		

6.2. DIN VDE V 0884-11 (VDE V 0884-11) :2017-01 INSULATION CHARACTERISTICS

Description	Test Condition	Symbol	Value	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150Vrms			I to IV	
For Rated Mains Voltage ≤ 300Vrms			I to IV	
For Rated Mains Voltage ≤ 600Vrms			I to III	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum repetitive peak isolation voltage		V_{IORM}	1166	V_{PEAK}
Maximum working isolation voltage	AC voltage(TDDB) test	V_{IOWM}	824	V_{RMS}
	DC Voltage	V_{IOWM}	1166	V_{DC}
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.5 = V_{pd(m)}$, 100%production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1749	V_{PEAK}
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1399	V_{PEAK}
After Input and /or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1399	V_{PEAK}
Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$; $t = 60$ s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$; $t = 1$ s (100% production)	V_{IOTM}	7000	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC60065,1.2/50us waveform, $V_{TEST} = 1.3 \times V_{ISOM}$	V_{IOSM}	5384	V_{PEAK}
Isolation resistance	$V_{IO} = 500V$	R_{IO}	$>10^{12}$	Ω
Isolation capacitance	$f = 1MHz$	C_{IO}	0.6	pF
Safety Power Dissipation for SOW20 Package	$\theta_{JA} = 68.5^{\circ}C/W$, $V_i = 5.5$ V, $T_J =$ $125^{\circ}C$, $T_A = 25^{\circ}C$	P_s	1459	mW
Safety input, output, or supply current for SOW20 Package	$\theta_{JA} = 68.5^{\circ}C/W$, $V_i = 5.5$ V, $T_J =$ $125^{\circ}C$, $T_A = 25^{\circ}C$	I_s	265	mA

Safety Power Dissipation for SOW16 Package	$\theta_{JA} = 61^{\circ}\text{C}/\text{W}$, $V_I = 5.5\text{ V}$, $T_J = 125^{\circ}\text{C}$, $T_A = 25^{\circ}\text{C}$	P_S	1639	mW
Safety input, output, or supply current for SOW16 Package	$\theta_{JA} = 61^{\circ}\text{C}/\text{W}$, $V_I = 5.5\text{ V}$, $T_J = 125^{\circ}\text{C}$, $T_A = 25^{\circ}\text{C}$	I_S	298	mA
Safety Temperature		T_S	125	$^{\circ}\text{C}$

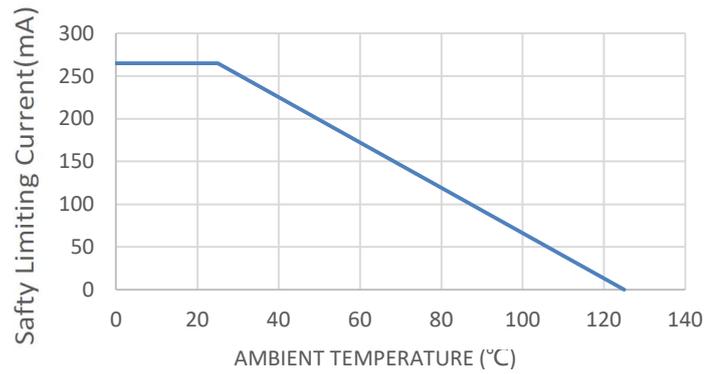


Figure 6.1 NSiP83086 Thermal Derating Curve for SOW20 package, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

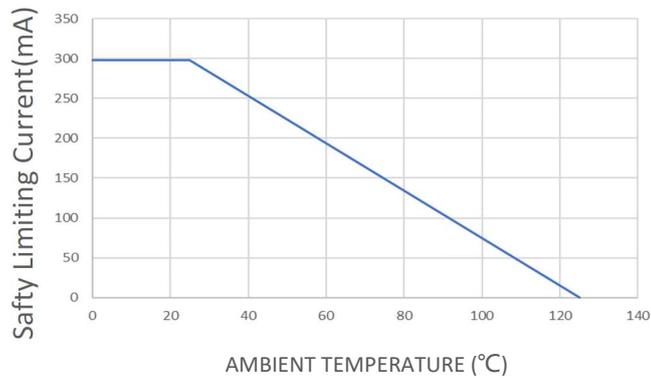


Figure 6.2 NSiP83086 Thermal Derating Curve for SOW16 package, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

6.3. Regulatory Information

The NSiP83086 are approved or pending approval by the organizations listed in table.

CUL		VDE		CQC	
UL 1577 Component Recognition Program ¹	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-11):2017-01 ²		Certified by CQC11-471543-2012	GB4943.1-2022
Single Protection, 5000V _{RMS} Isolation voltage	Single Protection, 5000V _{RMS} Isolation voltage	Basic Insulation 1166V _{peak} , V _{IOSM} =5384V _{PEAK}		Basic insulation	
File (pending)	File (pending)	File (pending)		File (pending)	

7. Function Description

NSiP83086 is a high reliability isolated full duplex RS-485 transceiver. Data isolation is achieved using Novosense integrated capacitive isolation that allows data transmission between the logic side and the Bus side. The 83086 series are safety certified by UL1577 supporting 5kV_{RMS} insulation withstand voltage.

7.1. True Fail-Safe Receiver Inputs

The devices feature fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted. The receiver threshold is fixed between -10mV and -200mV, which meets EIA/TIA-485 standard. If the differential input voltage ($V_A - V_B$) is greater than or equal to -10mV, receiver output R is logic high. In the case of a terminated bus with all transmitters disabled, the differential input voltage is pulled to zero by the termination resistors. Due to the receiver threshold, the receiver output R is logic high.

7.2. Truth Tables

Table 7.1 Driver Function Table¹

<i>VDD₁</i> status	Input (D)	Enable Input (DE)	Outputs	
			Y	Z
PU	H	H	H	L
PU	L	H	L	H
PU	X	L	Z	Z
PU	X	OPEN	Z	Z
PU	OPEN	H	H	L
PD	X	X	Z	Z

Table 7.2 Receiver Function Table¹

<i>VDD</i> status	Differential Input (VA-VB)	Enable Input (/RE)	Output (R)
PU	≥-10mV	L/Open	H
PU	≤-200mV	L/Open	L
PU	Open/Short	L/Open	H
PU	X	H	Z
PU	Idle	L	H
PD	X	X	Z

¹ PD= Powered down; PU= Powered up; H= Logic High; L= Logic Low; X= Irrelevant; Z= High Impedance;

7.3. EMI Considerations

NSiP83086 use a small on-chip transformer to provide power for RS485 Transceiver. The on-chip transformer operates at high frequency, which may degrade EMI performance, to achieve better EMI performance, special considerations must be taken during PCB layout. Please refer to the application note if needed.

7.4. Output Short and Over Temperature Protection

The NSiP83086 series are protected against output short for V_{ISOOUT}. When short on V_{ISOOUT} occurs, the device will be in Hiccup mode and the power transferred will be limit, which will limit the temperature of the device to protect the device.

The NSiP83086 series also protected against over temperature. When the chip is over 165°C, it will be shut down until the temperature of below 145°C.

8. Application Note

8.1. 256 Transceivers on the Bus

The devices have a 1/8-unit-load receiver input impedance (96kΩ) that allows up to 256 transceivers on the bus. Connect any combination of these devices, and/or other RS-485 devices, for a maximum of 32 unit-loads to the line.

8.2. ESD Protection

ESD protection structures are enhanced on all pins to protect against electrostatic discharge encountered during handling and assembly. The Bus pins have extra protection against static electricity to bus side (V_{ISOOUT} side).

ESD protection can be tested in various ways. Below is the ESD spec of the devices.

Bus pins:

- ±8kV w.r.t to GND2 using the Contact Discharge method specified in IEC 61000-4-2

Other pins except bus pins:

- ±7kV w.r.t to GND2 using the Contact Discharge method specified in IEC 61000-4-2

8.3. Layout Considerations

The NSiP83086 requires a 10μF+0.1μF bypass capacitor between VDD₁ and GND₁, 10uF+0.1uF bypass capacitor between V_{ISOOUT} and GND₂. The capacitor should be placed as close as possible to the package. To eliminate line reflections, each cable end (A-B, Y-Z) is terminated with a resistor, whose value matches the characteristic impedance of the cable(54 Ω/120 Ω). It's good practice to place the bus connectors and termination resistor as close as possible to the A and B, Y and Z pins.

8.4. Typical Application

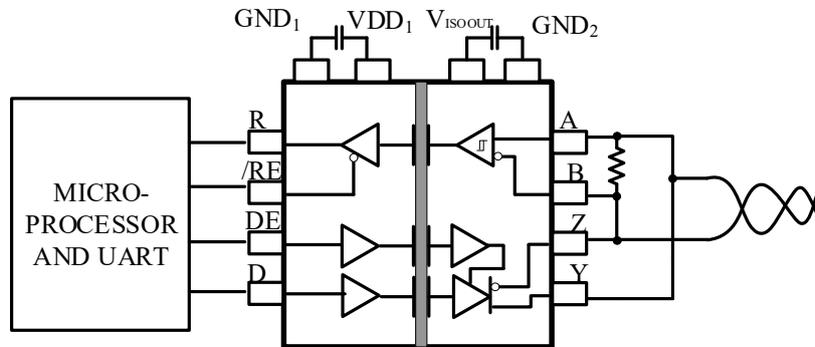


Figure 8.1 NSiP83086 in Half-Duplex RS-485 Mode

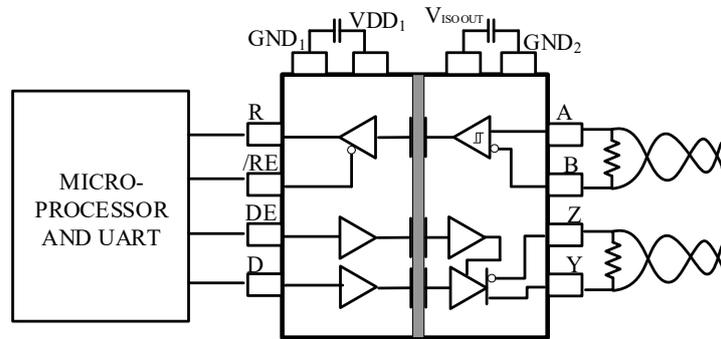


Figure 8.2 NSiP83086 typical application circuit

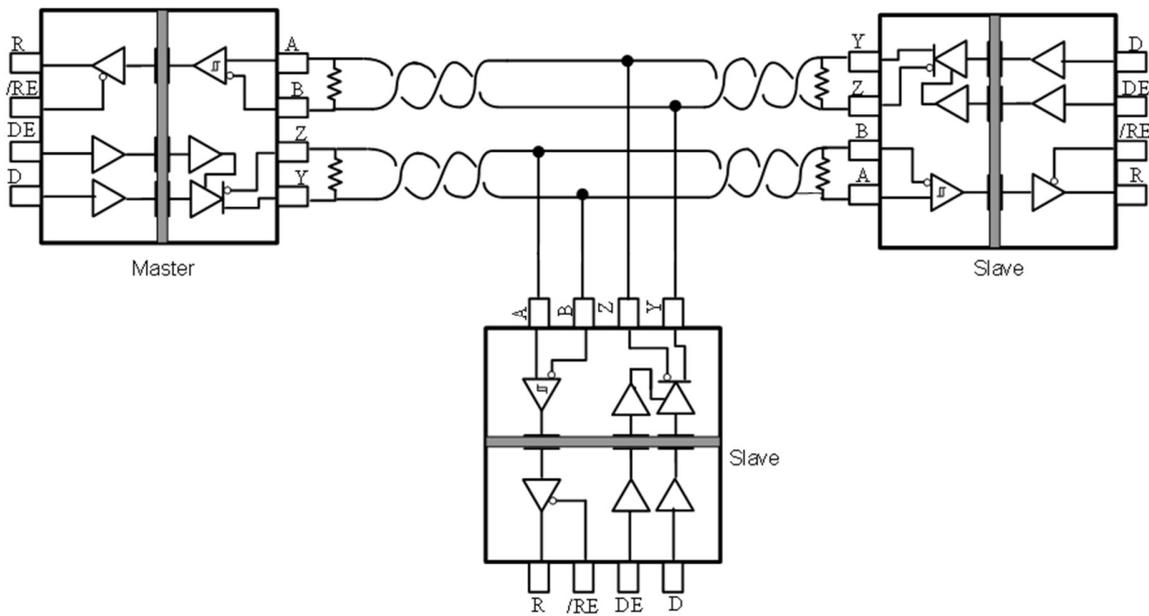


Figure 8.3 Typical isolated Full-Duplex RS-485 application

9. Package Information

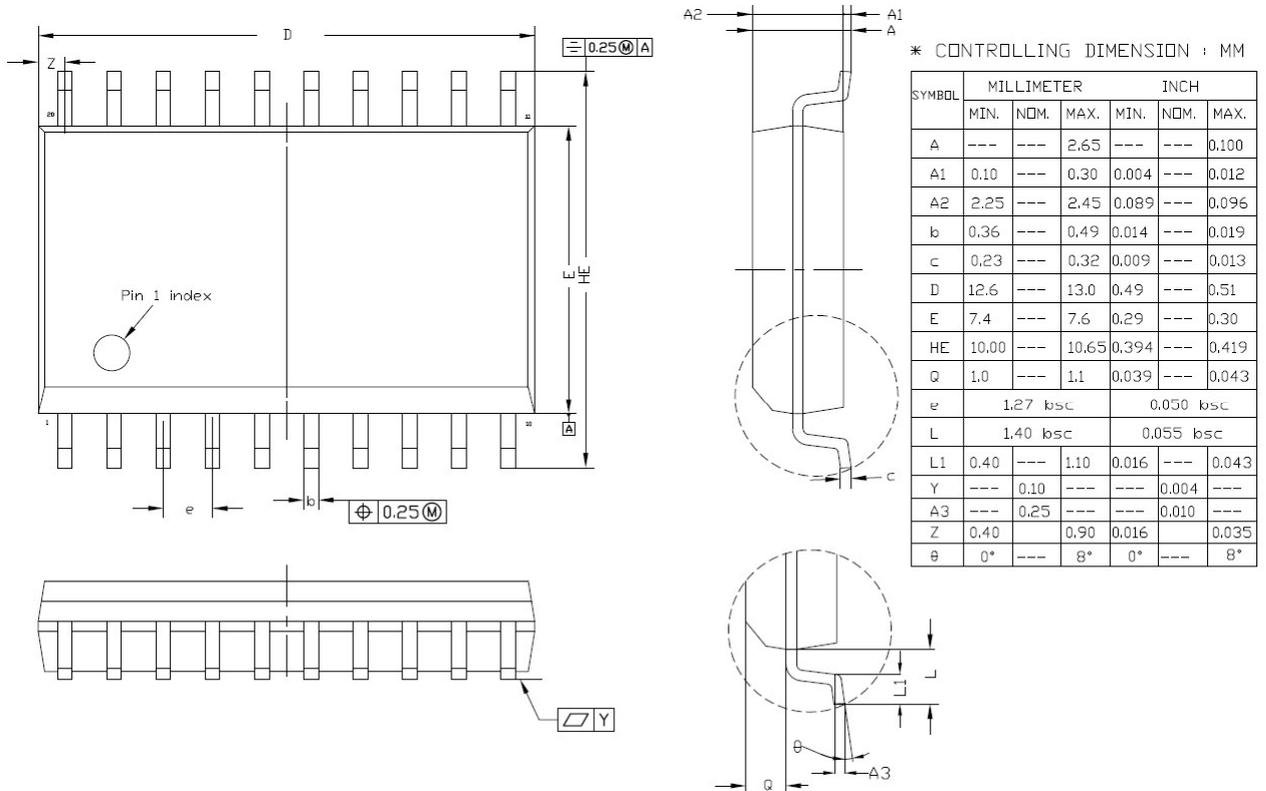


Figure 9.1 SOW20 Package Shape and Dimension in millimeters and inches

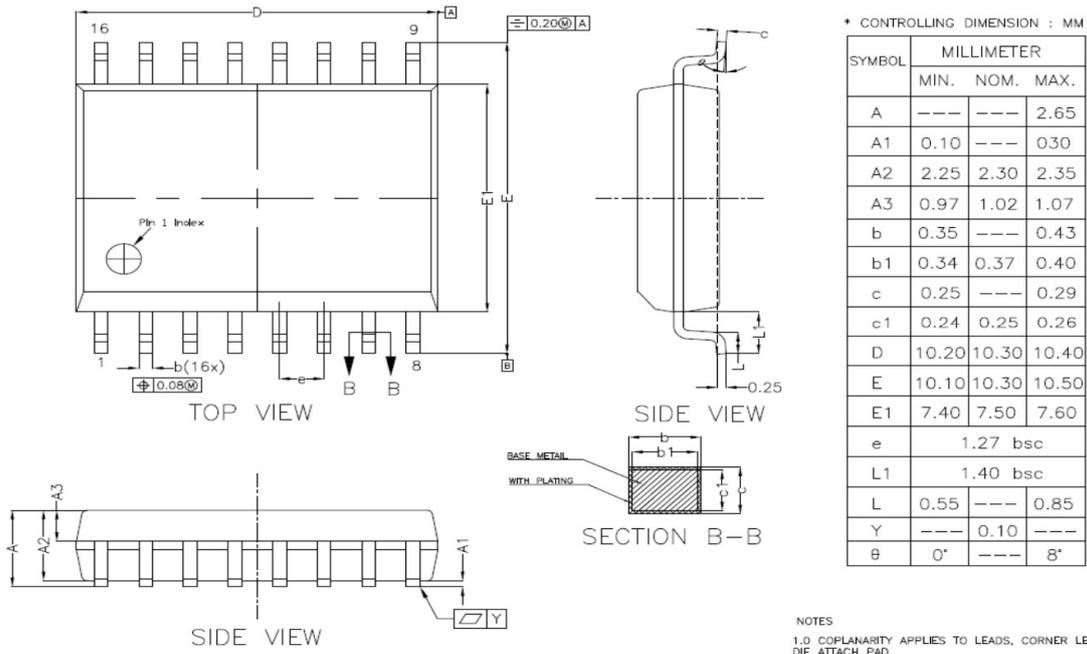


Figure 9.2 SOW16 Package Shape and Dimension in millimeters

10. Ordering Information

Part Number	Isolation Rating (kV _{RMS})	V _{ISOOUT}	Duplex	Max Data Rate (Mbps)	MSL	Temperature	No. of Nodes	Package Type	Package Drawing	SPQ
NSiP83086-DSWTR	5	5V	Full	16	3	-40 to 105°C	256	SOP20(300mil)	SOW20	1000
NSiP83086C-DSWTR	5	5/3.3V	Full	16	3	-40 to 105°C	256	SOP20(300mil)	SOW20	1000
NSiP83086V-DSWTR	5	3.3V	Full	16	3	-40 to 105°C	256	SOP20(300mil)	SOW20	1000
NSiP83086-DSWR	5	5V	Full	16	3	-40 to 105°C	256	SOP16(300mil)	SOW16	1000
NSiP83086V-DSWR	5	3.3V	Full	16	3	-40 to 105°C	256	SOP16(300mil)	SOW16	1000
NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.										

11. Documentation Support

Part Number	Product Folder	Datasheet	Application Note
NSiP83086	tbd	tbd	tbd

12. Tape And Reel Information

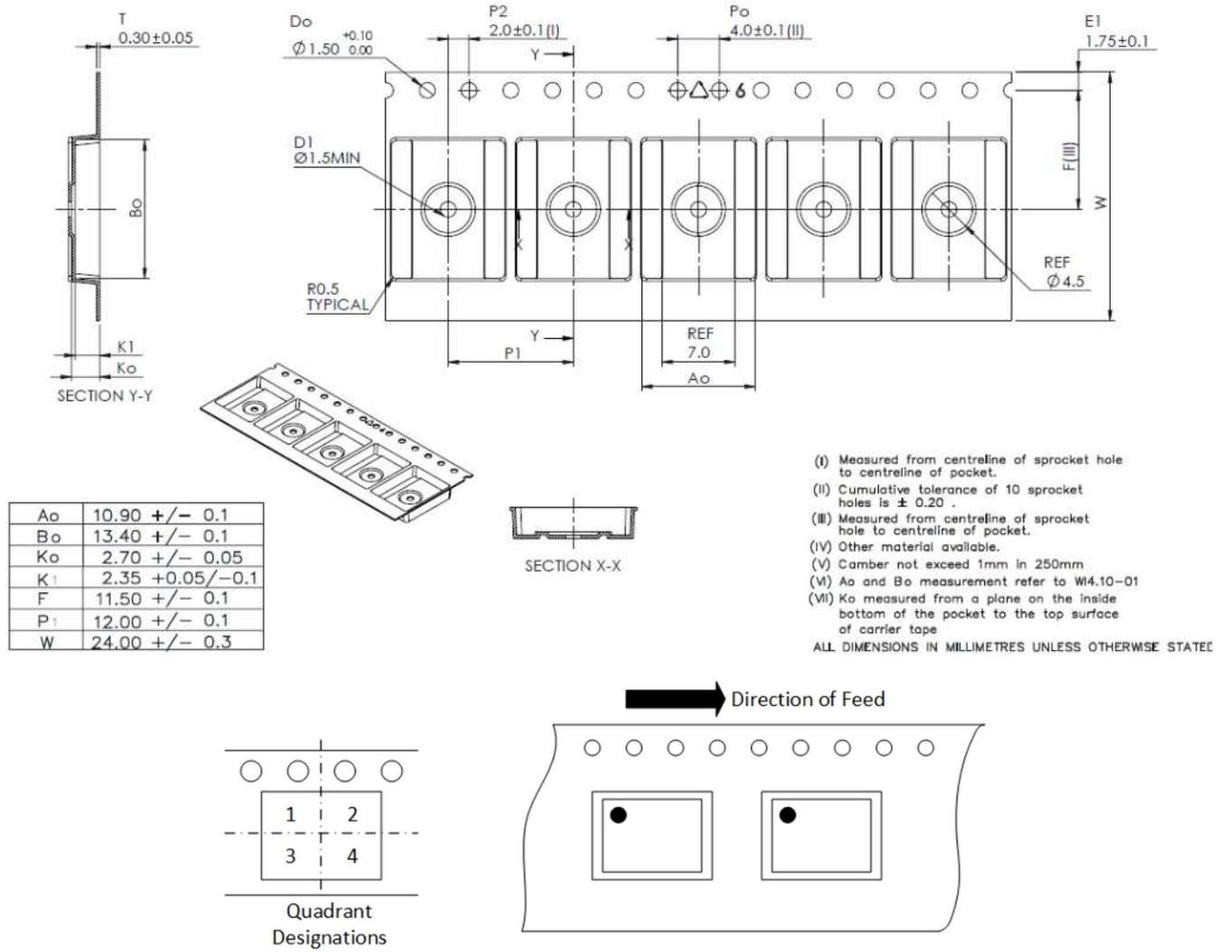
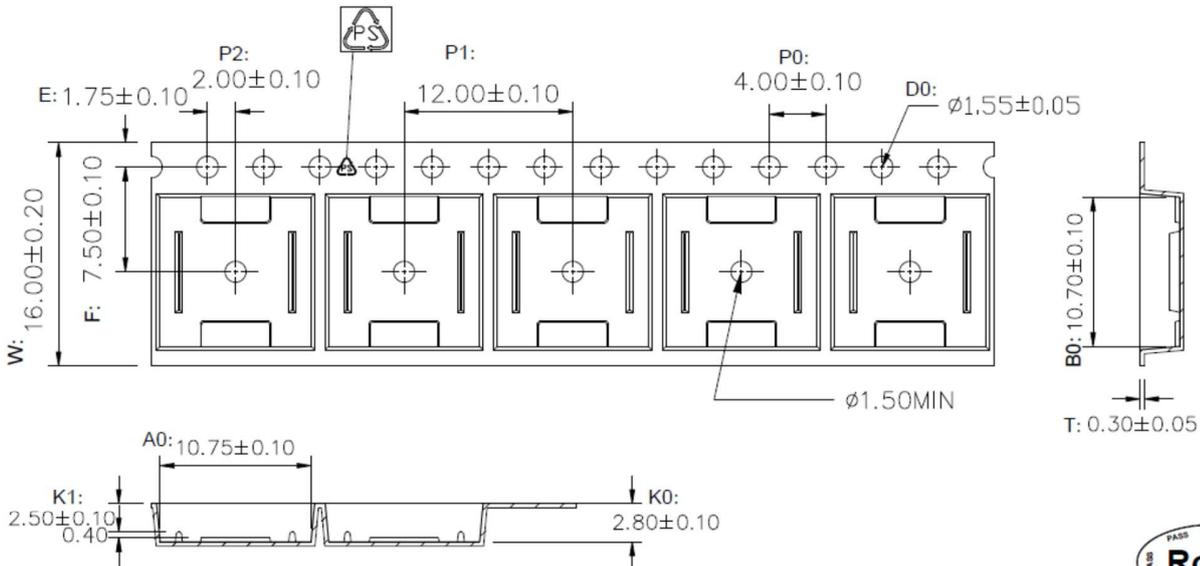


Figure 12.1 Tape and Reel Information of SOW20



1. 10 sprocket hole pitch cumulative tolerance ± 0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy .
4. All dimensions meet EIA-481 requirements.
5. Thickness : $0.30 \pm 0.05 \text{ mm}$.
6. Packing length per 22" reel : 378 Meters.(復巻 N=122)
7. Component load per 13" reel : 1000 pcs.
8. Surface resistivity : $10^5 \sim 10^{10} \Omega/\square$

W	16.00±0.20
A0	10.75±0.10
B0	10.70±0.10
K0	2.80±0.10
K1	2.50±0.10

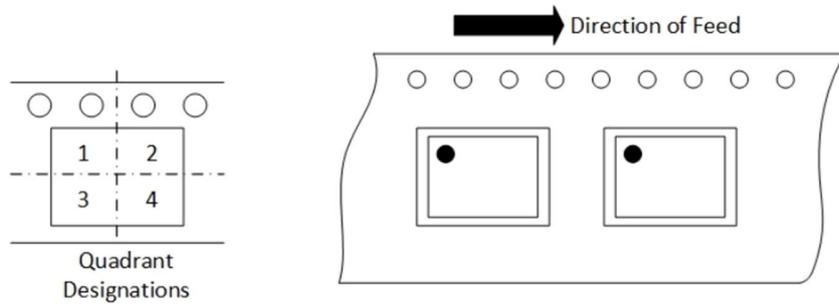


Figure 12.2 Tape and Reel Information of SOW16

13. Revision History

Revision	Description	Date
1.0	Initial Version	2022/11/30
1.1	Update Supply Current when $V_{ISOOUT} = 3.3V$ and Corrected Some Mistakes	2023/5/29

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