

NSS35200MR6T1G

35 V, 5 A, Low $V_{CE(sat)}$ PNP Transistor

ON Semiconductor's e²PowerEdge family of low $V_{CE(sat)}$ transistors are miniature surface mount devices featuring ultra low saturation voltage ($V_{CE(sat)}$) and high current gain capability. These are designed for use in low voltage, high speed switching applications where affordable efficient energy control is important.

Typical application are DC-DC converters and power management in portable and battery powered products such as cellular and cordless phones, PDAs, computers, printers, digital cameras and MP3 players. Other applications are low voltage motor controls in mass storage products such as disc drives and tape drives. In the automotive industry they can be used in air bag deployment and in the instrument cluster. The high current gain allows e²PowerEdge devices to be driven directly from PMU's control outputs, and the Linear Gain (Beta) makes them ideal components in analog amplifiers.

Features

- S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant*

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	V_{CEO}	-35	Vdc
Collector-Base Voltage	V_{CBO}	-55	Vdc
Emitter-Base Voltage	V_{EBO}	-5.0	Vdc
Collector Current - Continuous	I_C	-2.0	Adc
Collector Current - Peak	I_{CM}	-5.0	A
Electrostatic Discharge	ESD	HBM Class 3 MM Class C	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



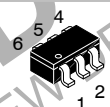
ON Semiconductor®

<http://onsemi.com>

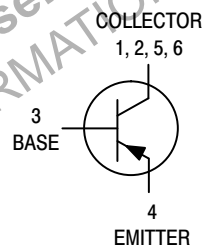
35 VOLTS

5.0 AMPS

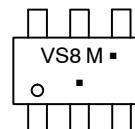
PNP LOW $V_{CE(sat)}$ TRANSISTOR
EQUIVALENT $R_{DS(on)}$ 100 m Ω



TSOP-6
CASE 318G
STYLE 6



MARKING DIAGRAM



VS8 = Device Code
M = Date Code*
▪ = Pb-Free Package

(*Note: Microdot may be in either location)
*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
NSS35200MR6T1G	TSOP-6 (Pb-Free)	3,000 / Tape & Reel
SNSS35200MR6T1G	TSOP-6 (Pb-Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NSS35200MR6T1G

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D (Note 1)	625 5.0	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$ (Note 1)	200	$^\circ\text{C/W}$
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D (Note 2)	1.0 8.0	W mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$ (Note 2)	120	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Lead #1	$R_{\theta JL}$	80	$^\circ\text{C/W}$
Total Device Dissipation (Single Pulse < 10 sec.)	$P_{D\text{single}}$ (Notes 2 & 3)	1.75	W
Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

1. FR-4 @ Minimum Pad.
2. FR-4 @ 1.0 X 1.0 inch Pad.
3. Refer to Figure 8.

DISCONTINUED
THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN
PLEASE CONTACT YOUR onsemi
REPRESENTATIVE FOR INFORMATION

NSS35200MR6T1G

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
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OFF CHARACTERISTICS

Collector – Emitter Breakdown Voltage (I _C = -10 mAdc, I _B = 0)	V _{(BR)CEO}	-35	-45	–	Vdc
Collector – Base Breakdown Voltage (I _C = -0.1 mAdc, I _E = 0)	V _{(BR)CBO}	-55	-65	–	Vdc
Emitter – Base Breakdown Voltage (I _E = -0.1 mAdc, I _C = 0)	V _{(BR)EBO}	-5.0	-7.0	–	Vdc
Collector Cutoff Current (V _{CB} = -35 Vdc, I _E = 0)	I _{CBO}	–	-0.03	-0.1	μAdc
Collector – Emitter Cutoff Current (V _{CES} = -35 Vdc)	I _{CES}	–	-0.03	-0.1	μAdc
Emitter Cutoff Current (V _{EB} = -4.0 Vdc)	I _{EBO}	–	-0.01	-0.1	μAdc

ON CHARACTERISTICS

DC Current Gain (Note 4) (I _C = -1.0 A, V _{CE} = -1.5 V) (I _C = -1.5 A, V _{CE} = -1.5 V) (I _C = -2.0 A, V _{CE} = -3.0 V)	h _{FE}	100 100 100	200 200 200	– 400 –	
Collector – Emitter Saturation Voltage (Note 4) (I _C = -0.8 A, I _B = -0.008 A) (I _C = -1.2 A, I _B = -0.012 A) (I _C = -2.0 A, I _B = -0.02 A)	V _{CE(sat)}	– – –	-0.125 -0.175 -0.260	-0.15 -0.20 -0.31	V
Base – Emitter Saturation Voltage (Note 4) (I _C = -1.2 A, I _B = -0.012 A)	V _{BE(sat)}		-0.68	-0.85	V
Base – Emitter Turn-on Voltage (Note 4) (I _C = -2.0 A, V _{CE} = -3.0 V)	V _{BE(on)}	–	-0.81	-0.875	V
Cutoff Frequency (I _C = -100 mA, V _{CE} = -5.0 V, f = 100 MHz)	f _T	100	–	–	MHz
Input Capacitance (V _{EB} = -0.5 V, f = 1.0 MHz)	C _{ibo}	–	600	650	pF
Output Capacitance (V _{CB} = -3.0 V, f = 1.0 MHz)	C _{obo}	–	85	100	pF
Turn-on Time (V _{CC} = -10 V, I _{B1} = -100 mA, I _C = -1 A, R _L = 3 Ω)	t _{on}	–	35	–	nS
Turn-off Time (V _{CC} = -10 V, I _{B1} = I _{B2} = -100 mA, I _C = 1 A, R _L = 3 Ω)	t _{off}	–	225	–	nS

4. Pulsed Condition: Pulse Width = 300 μsec, Duty Cycle ≤ 2%.

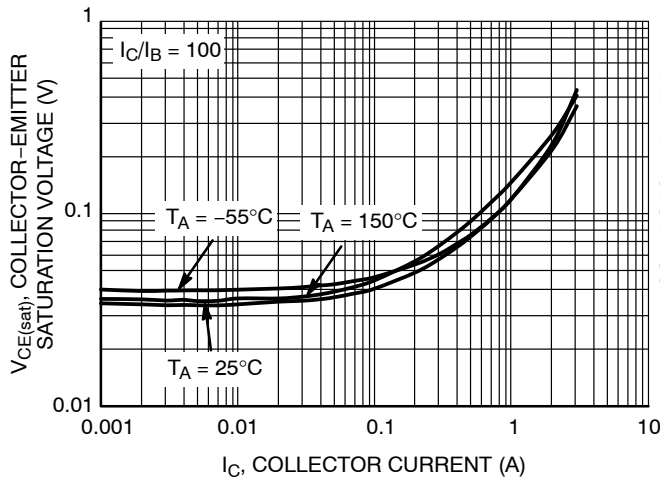


Figure 1. Collector Emitter Saturation Voltage versus Collector Current

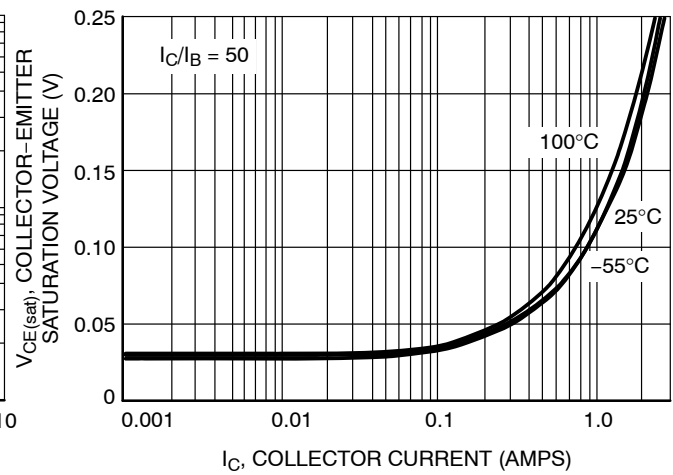


Figure 2. Collector Emitter Saturation Voltage versus Collector Current

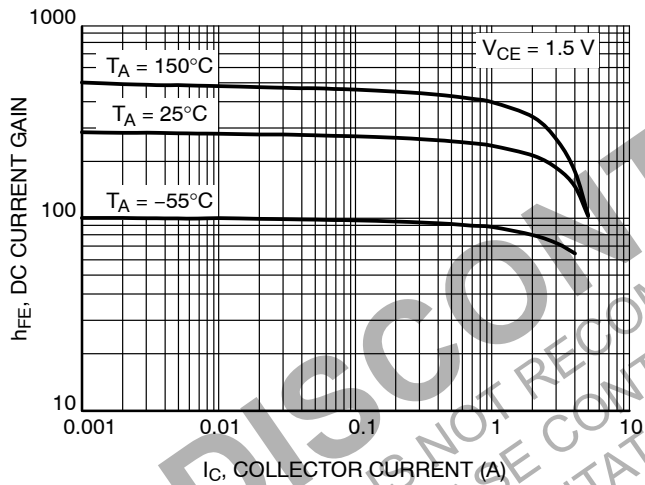


Figure 3. DC Current Gain versus Collector Current

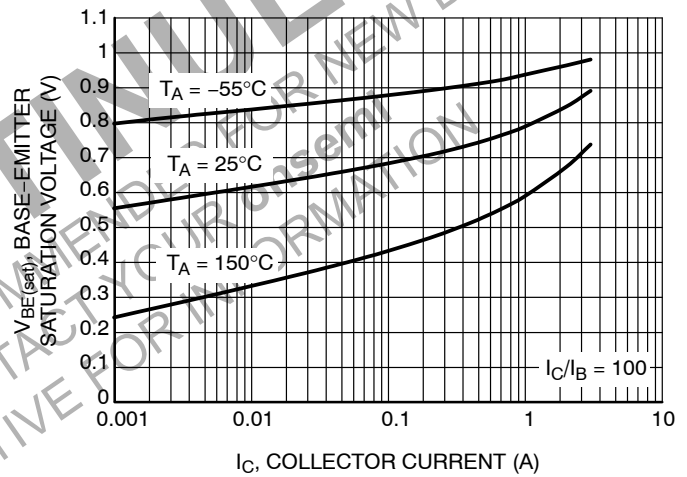


Figure 4. Base Emitter Saturation Voltage versus Collector Current

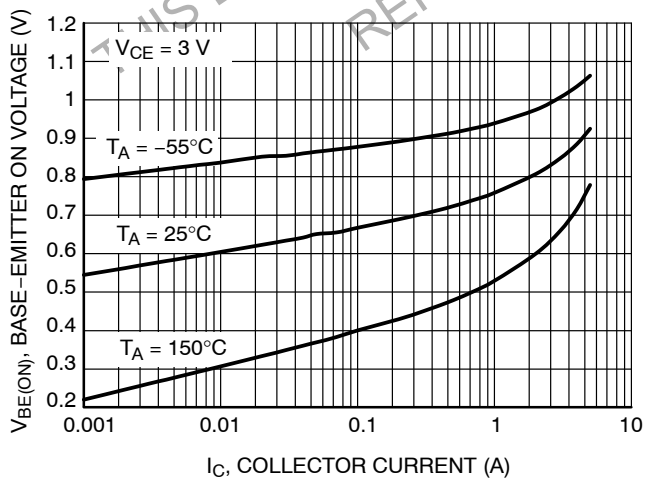


Figure 5. Base Emitter Turn-On Voltage versus Collector Current

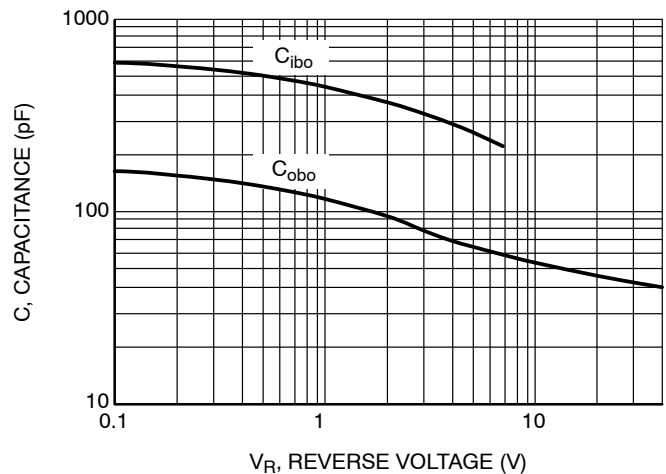


Figure 6. Capacitance

NSS35200MR6T1G

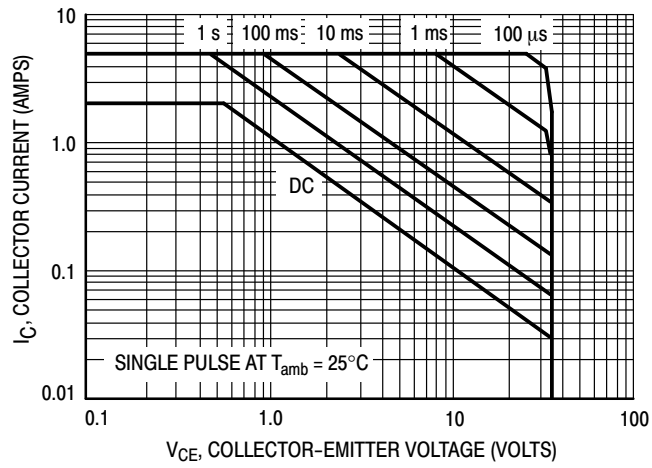


Figure 7. Safe Operating Area

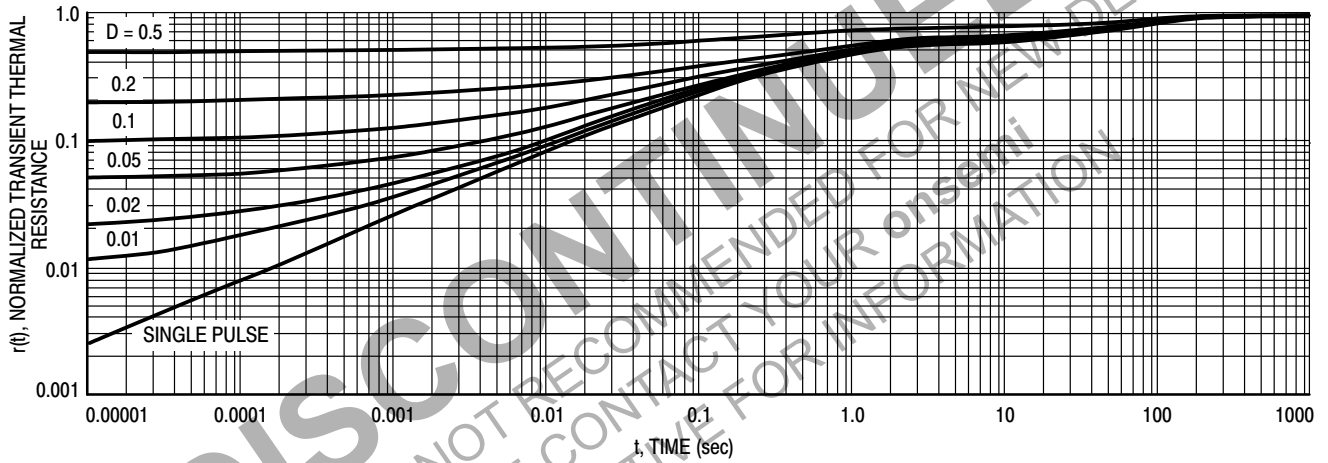
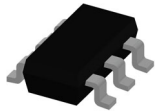
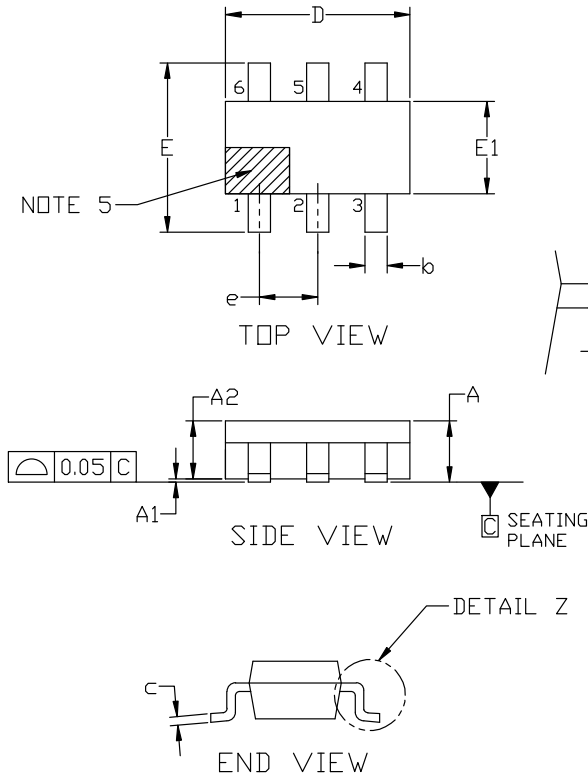


Figure 8. Normalized Thermal Response

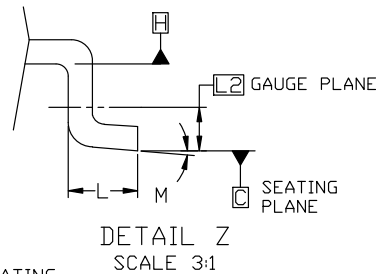

TSOP-6 3.00x1.50x0.90, 0.95P
CASE 318G
ISSUE W

DATE 26 FEB 2024

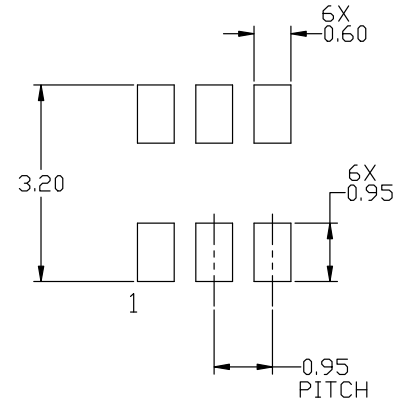


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN 1 INDICATOR MUST BE LOCATED IN THE INDICATED ZONE



MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
A2	0.80	0.90	1.00
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	---	10°


RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

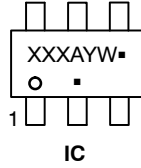
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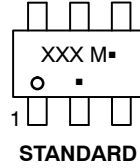
TSOP-6 3.00x1.50x0.90, 0.95P
CASE 318G
ISSUE W

DATE 26 FEB 2024

GENERIC
MARKING DIAGRAM*



IC



STANDARD

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
■ = Pb-Free Package

XXX = Specific Device Code
M = Date Code
■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1: PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN	STYLE 2: PIN 1. EMITTER 2 2. BASE 1 3. COLLECTOR 1 4. EMITTER 1 5. BASE 2 6. COLLECTOR 2	STYLE 3: PIN 1. ENABLE 2. N/C 3. R BOOST 4. Vz 5. V in 6. V out	STYLE 4: PIN 1. N/C 2. V in 3. NOT USED 4. GROUND 5. ENABLE 6. LOAD	STYLE 5: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2	STYLE 6: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR
STYLE 7: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. N/C 5. COLLECTOR 6. EMITTER	STYLE 8: PIN 1. Vbus 2. D(in) 3. D(in)+ 4. D(out)+ 5. D(out) 6. GND	STYLE 9: PIN 1. LOW VOLTAGE GATE 2. DRAIN 3. SOURCE 4. DRAIN 5. DRAIN 6. HIGH VOLTAGE GATE	STYLE 10: PIN 1. D(OUT)+ 2. GND 3. D(OUT)- 4. D(IN)- 5. VBUS 6. D(IN)+	STYLE 11: PIN 1. SOURCE 1 2. DRAIN 2 3. DRAIN 2 4. SOURCE 2 5. GATE 1 6. DRAIN 1/GATE 2	STYLE 12: PIN 1. I/O 2. GROUND 3. I/O 4. I/O 5. VCC 6. I/O
STYLE 13: PIN 1. GATE 1 2. SOURCE 2 3. GATE 2 4. DRAIN 2 5. SOURCE 1 6. DRAIN 1	STYLE 14: PIN 1. ANODE 2. SOURCE 3. GATE 4. CATHODE/DRAIN 5. CATHODE/DRAIN 6. CATHODE/DRAIN	STYLE 15: PIN 1. ANODE 2. SOURCE 3. GATE 4. DRAIN 5. N/C 6. CATHODE	STYLE 16: PIN 1. ANODE/CATHODE 2. BASE 3. EMITTER 4. COLLECTOR 5. ANODE 6. CATHODE	STYLE 17: PIN 1. EMITTER 2. BASE 3. ANODE/CATHODE 4. ANODE 5. CATHODE 6. COLLECTOR	

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