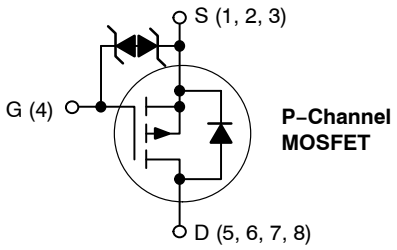
MOSFET - Power, Single P-Channel, WDFN8
-30 V, 3.8 mΩ, -96 A

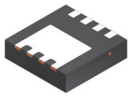
NTTFS008P03P8Z

$V_{(BR)DSS}$	$R_{DS(on)}$	I_D
−30 V	3.8 mΩ @ −10 V	−96 A
	6.5 mΩ @ −4.5 V	



Features
- Ultra Low $R_{DS(on)}$ to Improve System Efficiency
- Advanced Package Technology in 3.3x3.3mm for Space Saving and Excellent Thermal Conduction
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications
- Power Load Switch
- Protection: Reverse Current, Over Voltage, and Reverse Negative Voltage
- Battery Management



WDFN8
CASE 483AW

MARKING DIAGRAM

8P03 = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Lot Traceability Code

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	−30	V
Gate−to−Source Voltage			V_{GS}	±25	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2)	Steady State	T_C = 25°C	I_D	−96	A
		T_C = 85°C		−69	
Power Dissipation $R_{\theta JC}$ (Notes 1, 2)		T_C = 25°C	P_D	50	W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	T_A = 25°C	I_D	−22	A
		T_A = 85°C		−16	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		T_A = 25°C	P_D	2.67	W
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	−418	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to 150	°C
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case − Steady State (Drain) (Note 2)	$R_{\theta JC}$	2.5	°C/W
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	47	°C/W

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 1 in^2, 2 oz. Cu pad. Assuming a 76mm x 76mm x 1.6mm board.

ORDERING INFORMATION

Device	Package	Shipping†
NTTFS008P03P8Z	WDFN8 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 μA		−30			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = −250 μA, ref to 25°C			−8		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = −24 V	T_J = 25°C			−1.0	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±25 V				±10	μA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = −250 μA		−1.0		−3.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	I_D = −250 μA, ref to 25°C			5.9		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = −10 V, I_D = −18 A			2.5	3.8	mΩ
		V_{GS} = −4.5 V, I_D = −14 A			4.3	6.5	
Froward Transconductance	g_{FS}	V_{DS} = −5 V, I_D = −14 A			74		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = −15 V			5600		pF
Output Capacitance	C_{oss}				1940		
Reverse Transfer Capacitance	C_{rss}				1890		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −10 V, V_{DS} = −15 V, I_D = −14 A			134		nC
Threshold Gate Charge	$Q_{G(TH)}$				3		
Gate−to−Source Charge	Q_{GS}				15		
Gate−to−Drain Charge	Q_{GD}				51		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −4.5 V, V_{DS} = −15 V, I_D = −14 A			82		
SWITCHING CHARACTERISTICS, V_{GS} = 4.5 V (Note 3)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = −4.5 V, V_{DS} = −15 V, I_D = −14 A, R_G = 6 Ω			49		ns
Rise Time	t_r				248		
Turn−Off Delay Time	$t_{d(off)}$				95		
Fall Time	t_f				187		
SWITCHING CHARACTERISTICS, V_{GS} = 10 V (Note 3)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = −10 V, V_{DS} = −15 V, I_D = −14 A, R_G = 6 Ω			19		ns
Rise Time	t_r				53		
Turn−Off Delay Time	$t_{d(off)}$				201		
Fall Time	t_f				177		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = −14 A	T_J = 25°C		−0.77	−1.3	V
			T_J = 125°C		−0.63		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = −14 A			52		ns
Charge Time	t_a				21		
Discharge Time	t_b				30		
Reverse Recovery Charge	Q_{RR}				31		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

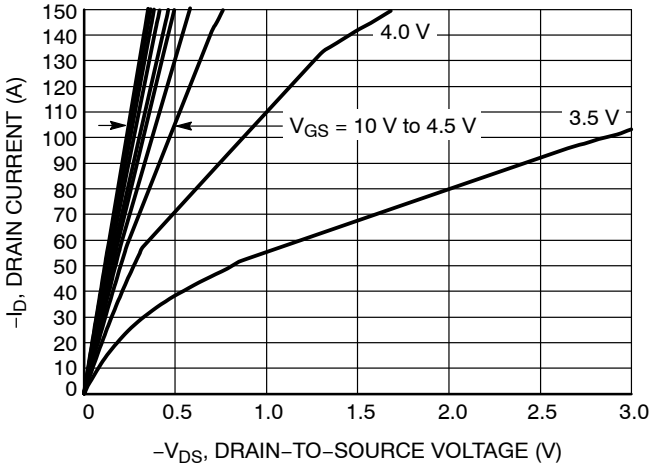


Figure 1. On−Region Characteristics

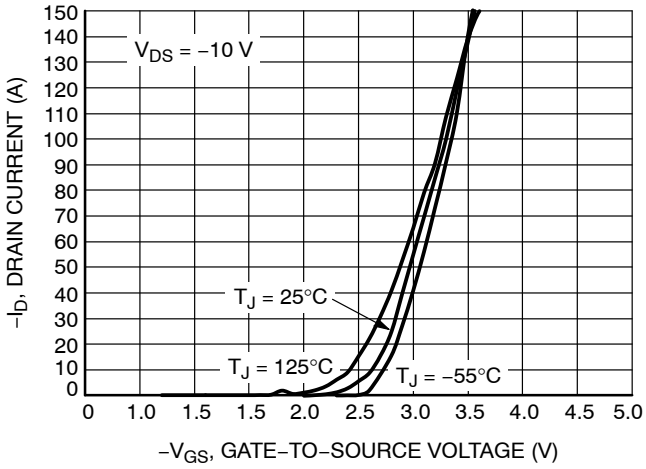


Figure 2. Transfer Characteristics

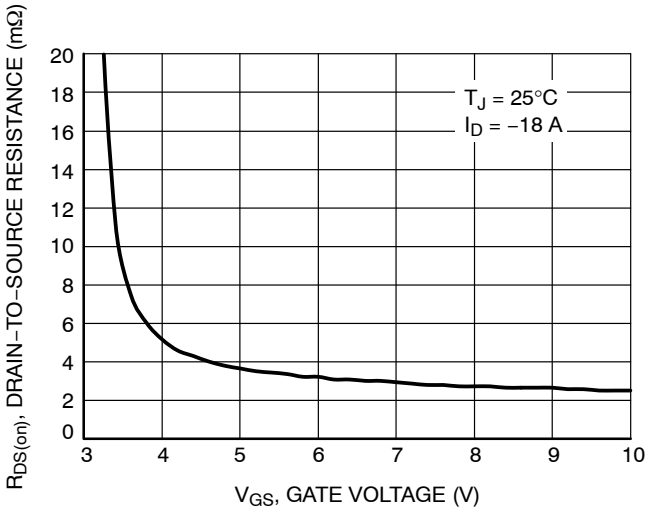


Figure 3. On−Resistance vs. Gate−to−Source Voltage

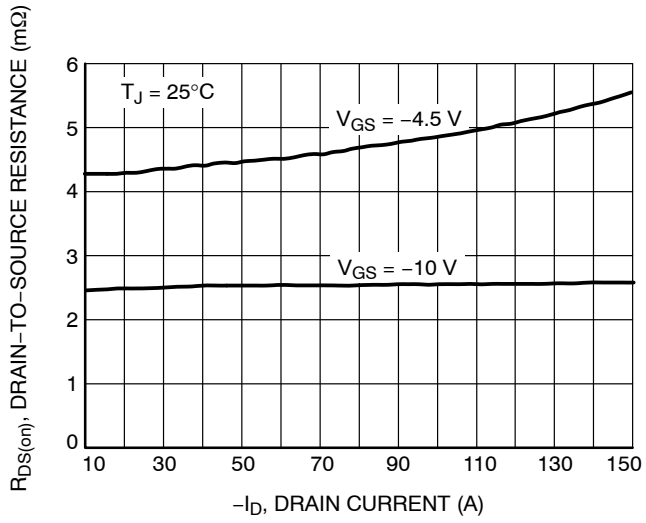


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

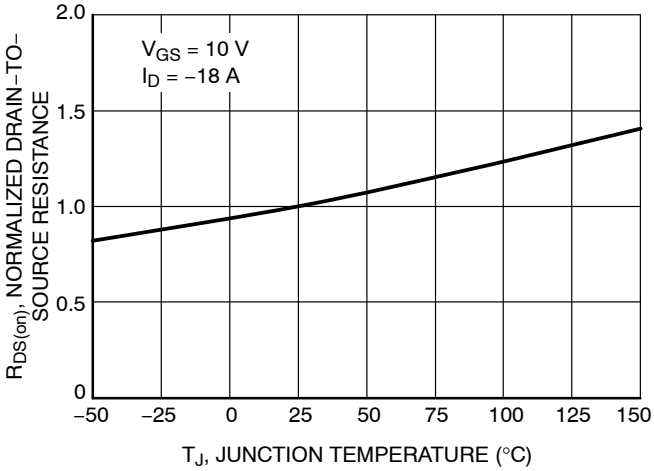


Figure 5. On−Resistance Variation with Temperature

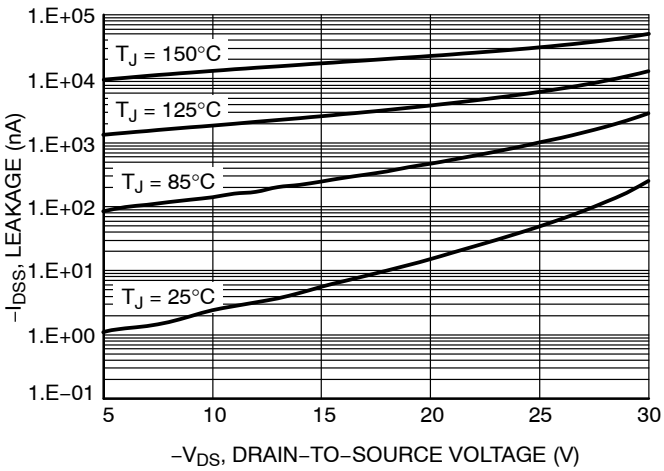


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

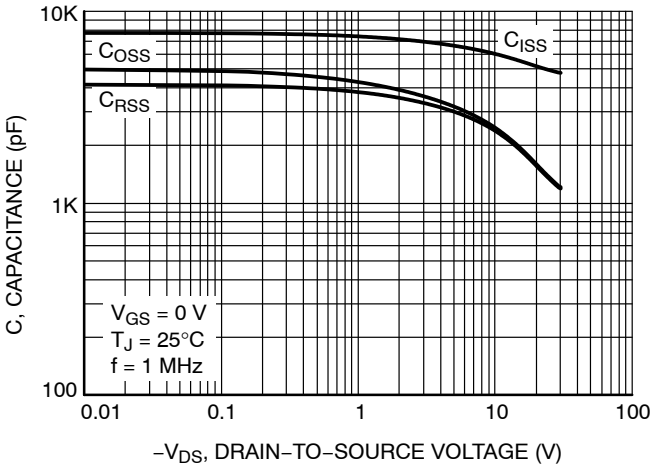


Figure 7. Capacitance Variation

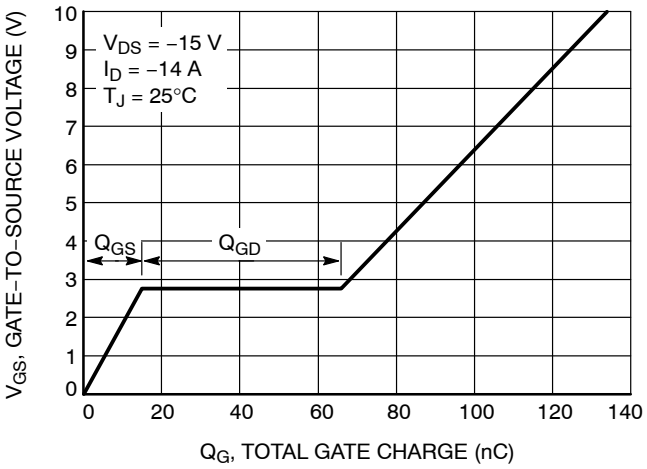


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

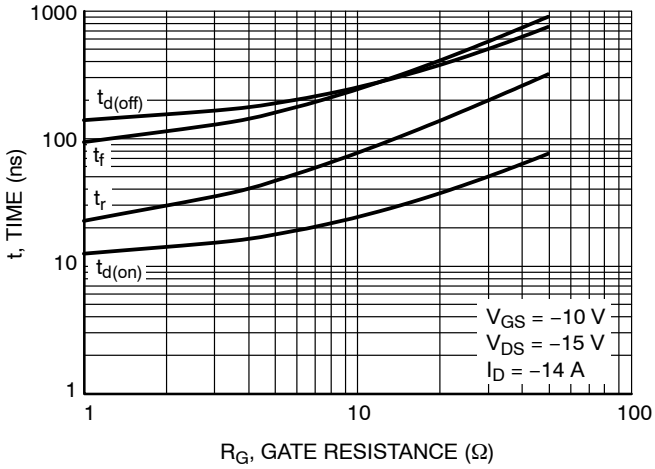


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

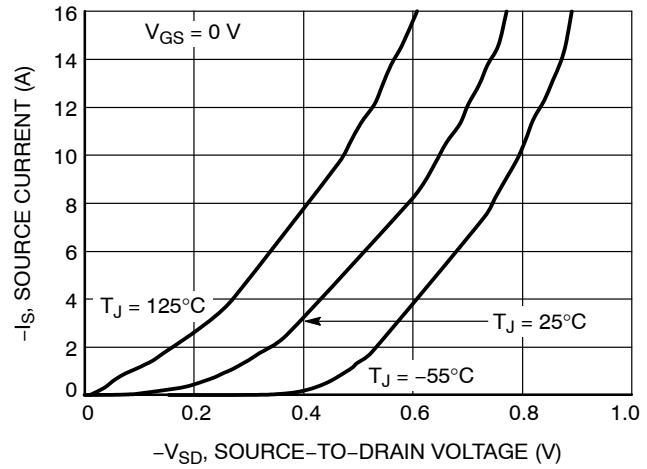


Figure 10. Diode Forward Voltage vs. Current

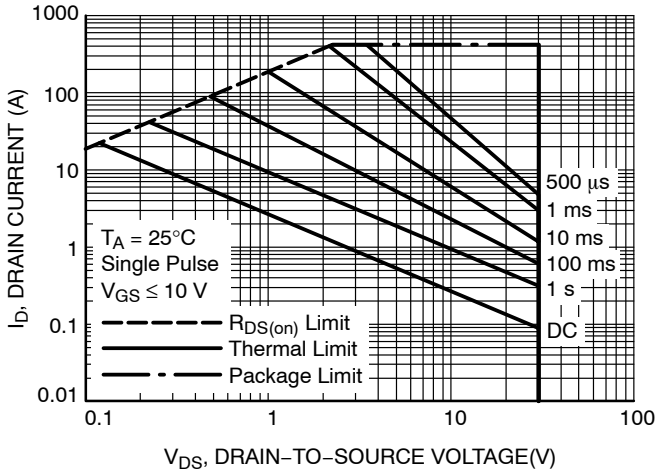


Figure 11. Safe Operating Area

TYPICAL CHARACTERISTICS

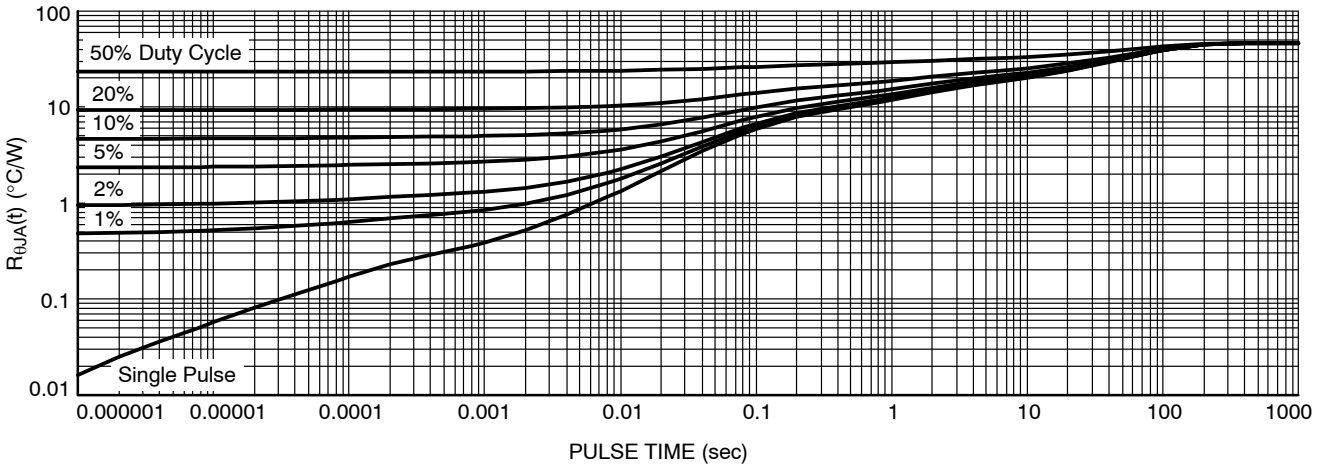
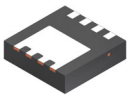
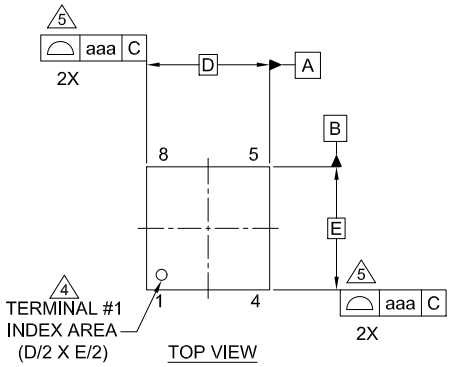


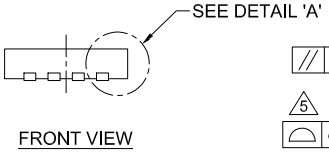
Figure 12. Thermal Characteristics

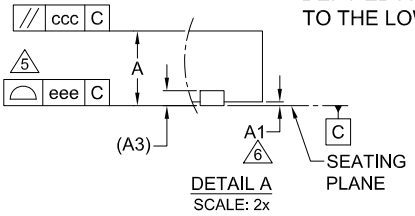


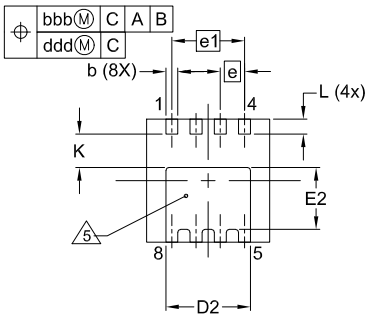
WDFN8 3.30x3.30x0.75, 0.65P
CASE 483AW
ISSUE B

DATE 22 MAR 2024







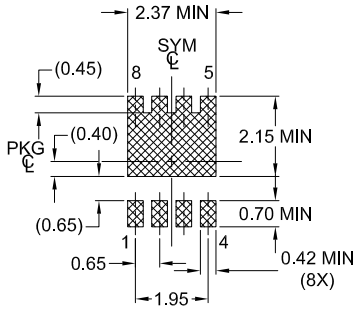


NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEP95 SEC. 3 SPP-12. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD, EMBEDDED METAL OR MARKED FEATURE.
5. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	--	--	0.05
A3		0.20 REF	
b	0.27	0.32	0.37
D		3.30 BSC	
D2	2.17	2.27	2.37
E		3.30 BSC	
E2	1.56	1.66	1.76
e		0.65 BSC	
e1		1.95 BSC	
K	0.90	--	--
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.05	

LAND PATTERN RECOMMENDATION



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**WDFN8 3.30x3.30x0.75, 0.65P**	**PAGE 1 OF 1**

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