PCA9654E, PCA9654EA

8-bit I/O Expander for I²C Bus and SMBus with Interrupt

The PCA9654E/PCA9654EA provides 8 bits of General Purpose parallel Input/Output (GPIO) expansion for I²C–bus/SMBus applications.

The PCA9654E/PCA9654EA consists of 8–bit Configuration (Input or Output selection), Input, Output and Polarity Inversion (active HIGH or active LOW operation) registers. The system master may set the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each Input or Output is kept in the corresponding Input or Output register. The polarity of the read register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

The PCA9654E/PCA9654EA open–drain interrupt ($\overline{INT}$) output is activated when any input state differs from its corresponding input port register state and is used to indicate to the system master that an input state has changed. The power–on reset sets the registers to their default values and initializes the device state machine.

Three hardware pins (AD0, AD1, AD2) vary the fixed I²C bus address and allow up to 64 devices to share the same I²C–bus/SMBus. The PCA9654EA has a different address map from the PCA9654E.

Features

- V_{DD} Operating Range: 1.65 V to 5.5 V
- SDA Sink Capability: 30 mA
- 5.5 V Tolerant I/Os
- Polarity Inversion Register
- Active LOW Interrupt Output
- Low Standby Current
- Noise Filter on SCL/SDA Inputs
- No Glitch on Power–up
- Internal Power–on Reset
- 64 Programmable Slave Addresses Using 3 Address Pins
- 8 I/O Pins which Default to 8 Inputs
- I²C SCL Clock Frequencies Supported:
  - Standard Mode: 100 kHz
  - Fast Mode: 400 kHz
  - Fast Mode +: 1 MHz
- ESD Performance: 4000 V Human Body Model, 400 V Machine Model
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

This document contains information on some products that are still under development. ON Semiconductor reserves the right to change or discontinue these products without notice.

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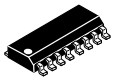
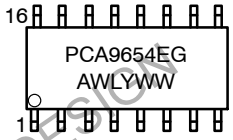
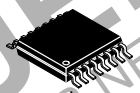
MARKING DIAGRAMS

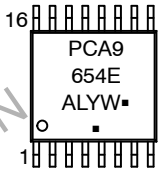


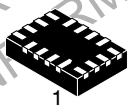
SOIC–16
D SUFFIX
CASE 751B



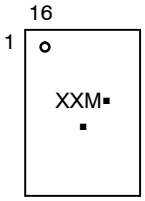


TSSOP–16
DT SUFFIX
CASE 948F

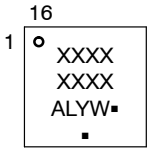


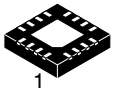


WQFN16
MT SUFFIX
CASE 488AP

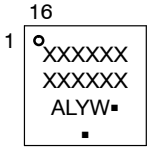


QFN16 3x3
MN SUFFIX
CASE 485G





QFN16 4x4
MN SUFFIX
CASE 485AP



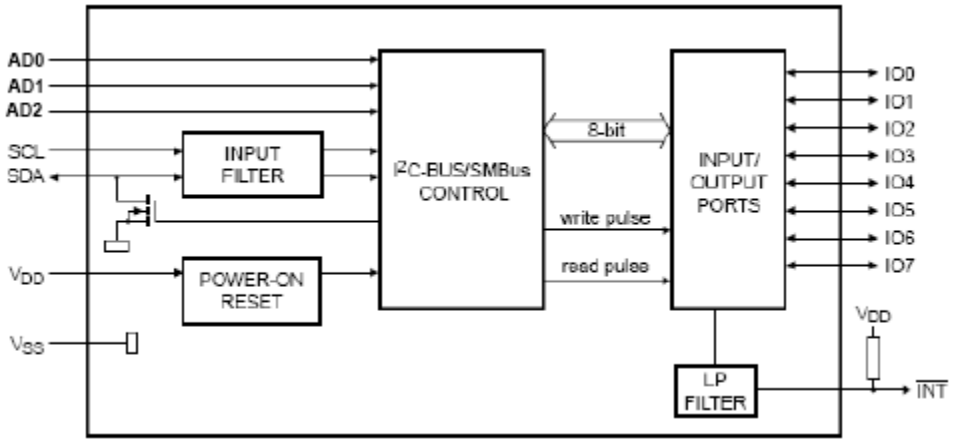
XXXX = Specific Device Code
A = Assembly Location
M = Date Code / Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ▪ = Pb–Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

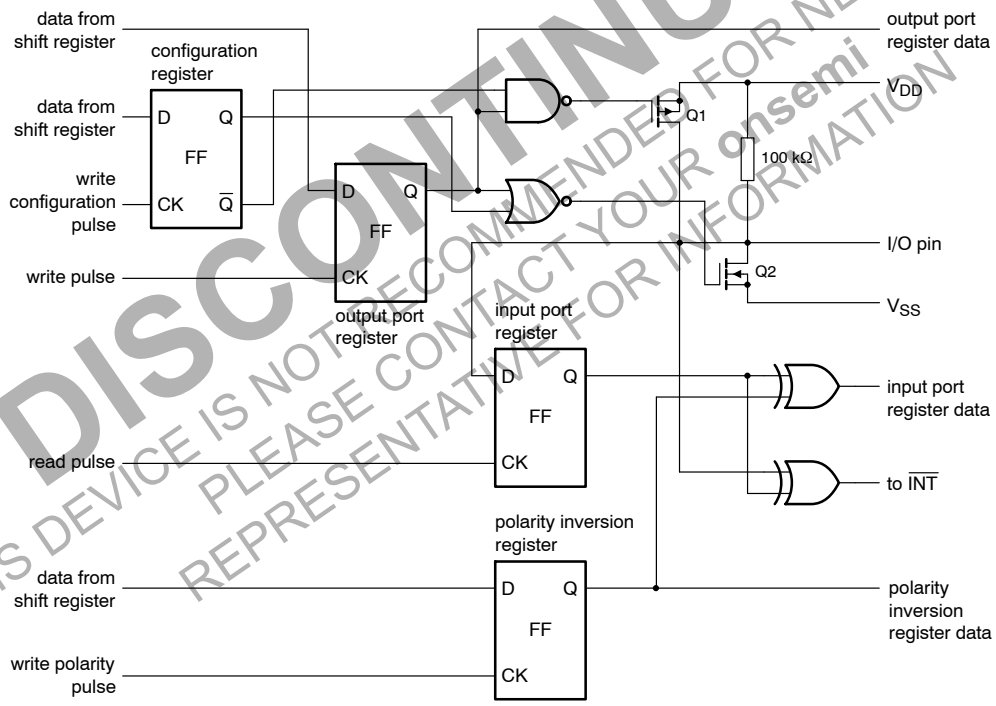
See detailed ordering and shipping information in the package dimensions section on page 17 of this data sheet.

BLOCK DIAGRAM



Remark: All I/Os are set to inputs at reset.

Figure 1. Block Diagram



At power−on reset, all registers return to default values.

Figure 2. Simplified Schematic of I/Os

PIN ASSIGNMENT

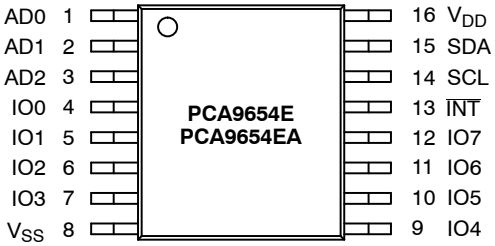


Figure 3. SOIC16 / TSSOP16

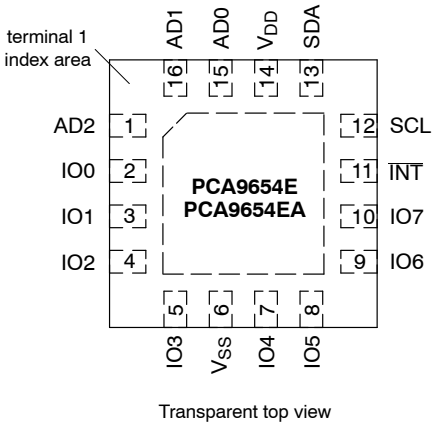


Figure 4. WQFN16 / QFN16

Table 1. PIN DESCRIPTIONS

Symbol	Pin		Description
	SOIC16, TSSOP16	QFN16, WQFN16	
AD0	1	15	Address Input 0
AD1	2	16	Address Input 1
AD2	3	1	Address Input 2
IO0	4	2	I/O 0
IO1	5	3	I/O 1
IO2	6	4	I/O 2
IO3	7	5	I/O 3
V_{SS}	8	6	Supply Ground
IO4	9	7	I/O 4
IO5	10	8	I/O 5
IO6	11	9	I/O 6
IO7	12	10	I/O 7
$\overline{INT}$	13	11	Interrupt Output (active−LOW)
SCL	14	12	Serial Clock Line
SDA	15	13	Serial Data Line
V_{DD}	16	14	Supply Voltage

Table 2. MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{DD}	DC Supply Voltage		−0.5 to +7.0	V
$V_{I/O}$	Input / Output Pin Voltage		−0.5 to +7.0	V
I_I	Input Current		±20	mA
I_O	Output Current		±50	mA
I_{DD}	DC Supply Current		±100	mA
I_{GND}	DC Ground Current		±200	mA
P_{TOT}	Total Power Dissipation		400	mW
P_{OUT}	Power Dissipation per Output		100	mW
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		150	°C
θ_{JA}	Thermal Resistance	SOIC−16 (Note 1) TSSOP−16 WQFN16 3 x 3 QFN16 4 x 4 QFN16	82 124 79 80 80	°C/W
P_D	Power Dissipation in Still Air at 85°C		190	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 4000 > 400 N/A	V
$I_{LATCHUP}$	Latchup Performance Above V_{CC} and Below GND at 125°C (Note 5)		±300	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 2 ounce copper trace no air flow.
2. Tested to EIA / JESD22−A114−A.
3. Tested to EIA / JESD22−A115−A.
4. Tested to JESD22−C101−A.
5. Tested to EIA / JESD78.

Table 3. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{DD}	Positive DC Supply Voltage	1.65	5.5	V
$V_{I/O}$	Switch Input / Output Voltage	0	5.5	V
T_A	Operating Free−Air Temperature	−55	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. DC ELECTRICAL CHARACTERISTICS V_{DD} = 1.65 V to 5.5 V, unless otherwise specified.

Symbol	Parameter	Conditions	T_A = −55°C to +125°C			Unit
			Min	Typ	Max	
SUPPLIES						
I_{DD}	Supply Current	Operating mode; no load; $V_I = V_{DD}$ or 0 V; f_{SCL} = 1 MHz $V_I = V_{DD}$ or 0 V; f_{SCL} = 100 kHz		 250 104	 500 175	μA
I_{STB}	Standby Current	Standby mode; no load; V_I = 0 V; f_{SCL} = 0 Hz; I/O = inputs $V_I = V_{DD}$; f_{SCL} = 0 Hz; I/O = inputs		 550 0.25	 700 1	μA
V_{POR}	Power−On Reset Voltage (Note 6)			1.5		V
INPUT SCL; Input / Output SDA						
V_{IH}	High−Level Input Voltage		0.7 x V_{DD}			V
V_{IL}	Low−Level Input Voltage				0.3 x V_{DD}	V
I_{OL}	Low−Level Output Current	V_{OL} = 0.4 V; V_{DD} < 2.3 V	10			mA
		V_{OL} = 0.4 V; $V_{DD} \geq$ 2.3 V	20			
I_L	Leakage Current	$V_I = V_{DD}$ or GND			±1	μA
C_I	Input Capacitance	V_I = GND			6	pF
I/Os						
V_{IH}	High−Level Input Voltage	2.3 V ≤ V_{CC} ≤ 5.5 V 1.65 V ≤ V_{CC} ≤ 2.3 V	2.0 0.7 x V_{DD}			V
V_{IL}	Low−Level Input Voltage	2.3 V ≤ V_{CC} ≤ 5.5 V 1.65 V ≤ V_{CC} ≤ 2.3 V			0.8 0.3 x V_{DD}	V
I_{OL}	Low−Level Output Current (Note 7)	V_{OL} = 0.5 V; V_{DD} = 1.65 V V_{OL} = 0.5 V; V_{DD} = 2.3 V V_{OL} = 0.5 V; V_{DD} = 3.0 V V_{OL} = 0.5 V; V_{DD} = 4.5 V	8 12 17 25	13 22 28 37		mA
$I_{OL(tot)}$	Total Low−Level Output Current (Note 7)	V_{OL} = 0.5 V; V_{DD} = 4.5 V			200	mA
V_{OH}	High−Level Output Voltage	I_{OH} = −3 mA; V_{DD} = 1.65 V I_{OH} = −4 mA; V_{DD} = 1.65 V I_{OH} = −8 mA; V_{DD} = 2.3 V I_{OH} = −10 mA; V_{DD} = 2.3 V I_{OH} = −8 mA; V_{DD} = 3.0 V I_{OH} = −10 mA; V_{DD} = 3.0 V I_{OH} = −8 mA; V_{DD} = 4.5 V I_{OH} = −10 mA; V_{DD} = 4.5 V	1.2 1.1 1.8 1.7 2.6 2.5 4.1 4.0			V
I_{LH}	Input Leakage Current	V_{DD} = 5.5 V; $V_I = V_{DD}$			1	μA
I_{LL}	Input Leakage Current	V_{DD} = 5.5 V; V_I = GND			−100	μA
$C_{I/O}$	Input / Output Capacitance (Note 8)			3.7	5	pF
INTERRUPT ($\overline{INT}$)						
I_{OL}	Low−Level Output Current	V_{OL} = 0.4 V	6			mA
C_O	Output Capacitance			2.1	5	pF
INPUTS AD0, AD1, AD2						
V_{IH}	High−Level Input Voltage	2.3 V ≤ V_{CC} ≤ 5.5 V 1.65 V ≤ V_{CC} ≤ 2.3 V	2.0 0.7 x V_{DD}			V
V_{IL}	Low−Level Input Voltage	2.3 V ≤ V_{CC} ≤ 5.5 V 1.65 V ≤ V_{CC} ≤ 2.3 V			0.8 0.3 x V_{DD}	V
I_L	Leakage Current	$V_I = V_{DD}$ or GND			±1	μA
C_I	Input Capacitance			2.4	5	pF

6. The power−on reset circuit resets the I^2C bus logic with $V_{DD} < V_{POR}$ and set all I/Os to logic 1 upon power−up. Thereafter, V_{DD} must be lower than 0.2 V to reset the part.
7. Each bit must be limited to a maximum of 25 mA and the total package limited to 200 mA due to internal bussing limits.
8. The value is not tested, but verified on sampling basis.

Table 5. AC ELECTRICAL CHARACTERISTICS V_{DD} = 1.65 V to 5.5 V; T_A = −55°C to +125°C, unless otherwise specified.

Symbol	Parameter	Standard Mode		Fast Mode		Fast Mode +		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency	0	0.1	0	0.4	0	1.0	MHz
t_{BUF}	Bus−Free Time between a STOP and START Condition	4.7		1.3		0.5		μs
$t_{HD:STA}$	Hold Time (Repeated) START Condition	4.0		0.6		0.26		μs
$t_{SU:STA}$	Setup Time for a Repeated START Condition	4.7		0.6		0.26		μs
$t_{SU:STO}$	Setup Time for STOP Condition	4.0		0.6		0.26		μs
$t_{HD:DAT}$	Data Hold Time	0		0		0		ns
$t_{VD:ACK}$	Data Valid Acknowledge Time (Note 9)	0.3	3.45	0.1	0.9	0.05	0.45	μs
$t_{VD:DAT}$	Data Valid Time (Note 10)	300		50		50	450	ns
$t_{SU:DAT}$	Data Setup Time	250		100		50		ns
t_{LOW}	LOW Period of SCL	4.7		1.3		0.5		μs
t_{HIGH}	HIGH Period of SCL	4.0		0.6		0.26		μs
t_f	Fall Time of SDA and SCL (Notes 12 and 13)		300	20 + 0.1C_b (Note 11)	300		120	ns
t_r	Rise Time of SDA and SCL		1000	20 + 0.1C_b (Note 11)	300		120	ns
t_{SP}	Pulse Width of Spikes Suppressed by Input Filter (Note 14)		50		50		50	ns
PORT TIMING: $C_L \leq$ 100 pF (See Figures 7 and 10)								
$t_{V(Q)}$	Data Output Valid Time		350		350		350	ns
$t_{SU(D)}$	Data Input Setup Time	100		100		100		ns
$t_{H(D)}$	Data Input Hold Time	1		1		1		μs
INTERRUPT TIMING: $C_L \leq$ 100 pF (See Figure 10)								
$t_{V(INT\_N)}$	Data Valid Time		4		4		4	μs
$t_{RST(INT\_N)}$	Reset Delay Time		4		4		4	μs

9. $t_{VD:ACK}$ = time for Acknowledgment signal from SCL LOW to SDA (out) LOW.
10. $t_{VD:DAT}$ = minimum time for SDA data out to be valid following SCL LOW.
11. C_b = total capacitance of one bus line in pF.
12. A master device must internally provide a hold time of al least 300 ns for the SDA signal (refer to V_{IL} of the SCL signal) in order to bridge the undefined region SCL's falling edge.
13. The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.
14. Input filters on the SDA and SCL inputs suppress noise spikes less than 50 ns.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Device Address

Following a START condition, the bus master must send the address of the slave it is accessing and the operation it wants to perform (read or write). The address of the PCA9654E/PCA9654EA is shown in Figure 5. Slave address pins AD2, AD1, and AD0 choose 1 of 64 slave addresses. To conserve power, no internal pull−up resistors are incorporated on AD2, AD1, and AD0. Address values can be found on Table 6 “PCA9654E Address Map” and Table 7 “PCA9654EA Address Map”.

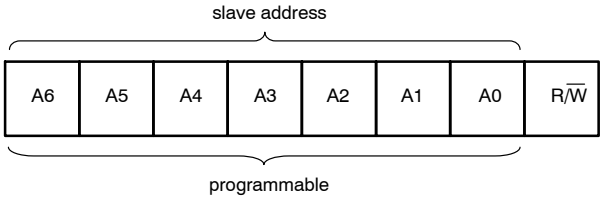


Figure 5. PCA9654E / PCA9654EA Device Address

A logic 1 on the last bit of the first byte selects a read operation while a logic 0 selects a write operation.

Table 6. PCA9654E ADDRESS MAP

Address Input			Slave Address							
AD2	AD1	AD0	A6	A5	A4	A3	A2	A1	A0	HEX
GND	SCL	GND	0	0	1	0	0	0	0	20h
GND	SCL	VDD	0	0	1	0	0	0	1	22h
GND	SDA	GND	0	0	1	0	0	1	0	24h
GND	SDA	VDD	0	0	1	0	0	1	1	26h
VDD	SCL	GND	0	0	1	0	1	0	0	28h
VDD	SCL	VDD	0	0	1	0	1	0	1	2Ah
VDD	SDA	GND	0	0	1	0	1	1	0	2Ch
VDD	SDA	VDD	0	0	1	0	1	1	1	2Eh
GND	SCL	SCL	0	0	1	1	0	0	0	30h
GND	SCL	SDA	0	0	1	1	0	0	1	32h
GND	SDA	SCL	0	0	1	1	0	1	0	34h
GND	SDA	SDA	0	0	1	1	0	1	1	36h
VDD	SCL	SCL	0	0	1	1	1	0	0	38h
VDD	SCL	SDA	0	0	1	1	1	0	1	3Ah
VDD	SDA	SCL	0	0	1	1	1	1	0	3Ch
VDD	SDA	SDA	0	0	1	1	1	1	1	3Eh
GND	GND	GND	0	1	0	0	0	0	0	40h
GND	GND	VDD	0	1	0	0	0	0	1	42h
GND	VDD	GND	0	1	0	0	0	1	0	44h
GND	VDD	VDD	0	1	0	0	0	1	1	46h
VDD	GND	GND	0	1	0	0	1	0	0	48h
VDD	GND	VDD	0	1	0	0	1	0	1	4Ah
VDD	VDD	GND	0	1	0	0	1	1	0	4Ch
VDD	VDD	VDD	0	1	0	0	1	1	1	4Eh
GND	GND	SCL	0	1	0	1	0	0	0	50h
GND	GND	SDA	0	1	0	1	0	0	1	52h
GND	VDD	SCL	0	1	0	1	0	1	0	54h
GND	VDD	SDA	0	1	0	1	0	1	1	56h
VDD	GND	SCL	0	1	0	1	1	0	0	58h
VDD	GND	SDA	0	1	0	1	1	0	1	5Ah
VDD	VDD	SCL	0	1	0	1	1	1	0	5Ch

Table 6. PCA9654E ADDRESS MAP

Address Input			Slave Address							
AD2	AD1	AD0	A6	A5	A4	A3	A2	A1	A0	HEX
VDD	VDD	SDA	0	1	0	1	1	1	1	5Eh
SCL	SCL	GND	1	0	1	0	0	0	0	A0h
SCL	SCL	VDD	1	0	1	0	0	0	1	A2h
SCL	SDA	GND	1	0	1	0	0	1	0	A4h
SCL	SDA	VDD	1	0	1	0	0	1	1	A6h
SDA	SCL	GND	1	0	1	0	1	0	0	A8h
SDA	SCL	VDD	1	0	1	0	1	0	1	AAh
SDA	SDA	GND	1	0	1	0	1	1	0	ACh
SDA	SDA	VDD	1	0	1	0	1	1	1	AEh
SCL	SCL	SCL	1	0	1	1	0	0	0	B0h
SCL	SCL	SDA	1	0	1	1	0	0	1	B2h
SCL	SDA	SCL	1	0	1	1	0	1	0	B4h
SCL	SDA	SDA	1	0	1	1	0	1	1	B6h
SDA	SCL	SCL	1	0	1	1	1	0	0	B8h
SDA	SCL	SDA	1	0	1	1	1	0	1	BAh
SDA	SDA	SCL	1	0	1	1	1	1	0	BCh
SDA	SDA	SDA	1	0	1	1	1	1	1	BEh
SCL	GND	GND	1	1	0	0	0	0	0	C0h
SCL	GND	VDD	1	1	0	0	0	0	1	C2h
SCL	VDD	GND	1	1	0	0	0	1	0	C4h
SCL	VDD	VDD	1	1	0	0	0	1	1	C6h
SDA	GND	GND	1	1	0	0	1	0	0	C8h
SDA	GND	VDD	1	1	0	0	1	0	1	CAh
SDA	VDD	GND	1	1	0	0	1	1	0	CCh
SDA	VDD	VDD	1	1	0	0	1	1	1	CEh
SCL	GND	SCL	1	1	1	0	0	0	0	E0h
SCL	GND	SDA	1	1	1	0	0	0	1	E2h
SCL	VDD	SCL	1	1	1	0	0	1	0	E4h
SCL	VDD	SDA	1	1	1	0	0	1	1	E6h
SDA	GND	SCL	1	1	1	0	1	0	0	E8h
SDA	GND	SDA	1	1	1	0	1	0	1	EAh
SDA	VDD	SCL	1	1	1	0	1	1	0	ECh
SDA	VDD	SDA	1	1	1	0	1	1	1	EEh

Table 7. PCA9654EA ADDRESS MAP

Address Input			Slave Address							
AD2	AD1	AD0	A6	A5	A4	A3	A2	A1	A0	HEX
VSS	SCL	VSS	0	0	0	1	0	0	0	10h
VSS	SCL	VDD	0	0	0	1	0	0	1	12h
VSS	SDA	VSS	0	0	0	1	0	1	0	14h
VSS	SDA	VDD	0	0	0	1	0	1	1	16h
VDD	SCL	VSS	0	0	0	1	1	0	0	18h
VDD	SCL	VDD	0	0	0	1	1	0	1	1Ah
VDD	SDA	VSS	0	0	0	1	1	1	0	1Ch
VDD	SDA	VDD	0	0	0	1	1	1	1	1Eh
VSS	SCL	SCL	0	1	1	0	0	0	0	60h
VSS	SCL	SDA	0	1	1	0	0	0	1	62h
VSS	SDA	SCL	0	1	1	0	0	1	0	64h
VSS	SDA	SDA	0	1	1	0	0	1	1	66h
VDD	SCL	SCL	0	1	1	0	1	0	0	68h
VDD	SCL	SDA	0	1	1	0	1	0	1	6Ah
VDD	SDA	SCL	0	1	1	0	1	1	0	6Ch
VDD	SDA	SDA	0	1	1	0	1	1	1	6Eh
VSS	VSS	VSS	0	1	1	1	0	0	0	70h
VSS	VSS	VDD	0	1	1	1	0	0	1	72h
VSS	VDD	VSS	0	1	1	1	0	1	0	74h
VSS	VDD	VDD	0	1	1	1	0	1	1	76h
VDD	VSS	VSS	0	1	1	1	1	0	0	78h
VDD	VSS	VDD	0	1	1	1	1	0	1	7Ah
VDD	VDD	VSS	0	1	1	1	1	1	0	7Ch
VDD	VDD	VDD	0	1	1	1	1	1	1	7Eh
VSS	VSS	SCL	1	0	0	0	0	0	0	80h
VSS	VSS	SDA	1	0	0	0	0	0	1	82h
VSS	VDD	SCL	1	0	0	0	0	1	0	84h
VSS	VDD	SDA	1	0	0	0	0	1	1	86h
VDD	VSS	SCL	1	0	0	0	1	0	0	88h
VDD	VSS	SDA	1	0	0	0	1	0	1	8Ah
VDD	VDD	SCL	1	0	0	0	1	1	0	8Ch
VDD	VDD	SDA	1	0	0	0	1	1	1	8Eh
SCL	SCL	VSS	1	0	0	1	0	0	0	90h
SCL	SCL	VDD	1	0	0	1	0	0	1	92h
SCL	SDA	VSS	1	0	0	1	0	1	0	94h
SCL	SDA	VDD	1	0	0	1	0	1	1	96h
SDA	SCL	VSS	1	0	0	1	1	0	0	98h
SDA	SCL	VDD	1	0	0	1	1	0	1	9Ah
SDA	SDA	VSS	1	0	0	1	1	1	0	9Ch
SDA	SDA	VDD	1	0	0	1	1	1	1	9Eh
SCL	SCL	SCL	1	1	0	1	0	0	0	D0h

Table 7. PCA9654EA ADDRESS MAP

Address Input			Slave Address							
AD2	AD1	AD0	A6	A5	A4	A3	A2	A1	A0	HEX
SCL	SCL	SDA	1	1	0	1	0	0	1	D2h
SCL	SDA	SCL	1	1	0	1	0	1	0	D4h
SCL	SDA	SDA	1	1	0	1	0	1	1	D6h
SDA	SCL	SCL	1	1	0	1	1	0	0	D8h
SDA	SCL	SDA	1	1	0	1	1	0	1	DAh
SDA	SDA	SCL	1	1	0	1	1	1	0	DCh
SDA	SDA	SDA	1	1	0	1	1	1	1	DEh
SCL	VSS	VSS	1	1	1	1	0	0	0	F0h
SCL	VSS	VDD	1	1	1	1	0	0	1	F2h
SCL	VDD	VSS	1	1	1	1	0	1	0	F4h
SCL	VDD	VDD	1	1	1	1	0	1	1	F6h
SDA	VSS	VSS	1	1	1	1	1	0	0	– (Note 15)
SDA	VSS	VDD	1	1	1	1	1	0	1	FAh
SDA	VDD	VSS	1	1	1	1	1	1	0	FCh
SDA	VDD	VDD	1	1	1	1	1	1	1	FEh
SCL	VSS	SCL	0	0	0	0	0	0	0	– (Note 15)
SCL	VSS	SDA	0	0	0	0	0	0	1	02h
SCL	VDD	SCL	0	0	0	0	0	1	0	04h
SCL	VDD	SDA	0	0	0	0	0	1	1	06h
SDA	VSS	SCL	0	0	0	0	1	0	0	08h
SDA	VSS	SDA	0	0	0	0	1	0	1	0Ah
SDA	VDD	SCL	0	0	0	0	1	1	0	0Ch
SDA	VDD	SDA	0	0	0	0	1	1	1	0Eh

15. The PCA9654EA does not acknowledge this AD2, AD1 and AD0 configuration.

REGISTERS

Command Byte

Table 8. COMMAND BYTE

COMMAND	PROTOCOL	REGISTER
0	Read byte	Input Port
1	Read / Write byte	Output Port
2	Read / Write byte	Polarity Inversion
3	Read / Write byte	Configuration

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

Register 0 – Input Port Register

This register is a read−only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writes to this register have no effect.

The default ‘X’ is determined by the externally applied logic level, normally ‘1’ when no external signal externally applied because of the internal pull−up resistors.

Table 9. INPUT PORT REGISTER

Bit	7	6	5	4	3	2	1	0
Symbol	I7	I6	I5	I4	I3	I2	I1	I0
Access	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X

Register 1 – Output Port Register

This register reflects the outgoing logic levels of the pins defined as outputs by Register 3. Bit values in this register have no effect on pins defined as inputs. Reads from this register return the value that is in the flip−flop controlling the output selection, **not** the actual pin value.

Table 10. OUTPUT PORT REGISTER

Bit	7	6	5	4	3	2	1	0
Symbol	O7	O6	O5	O4	O3	O2	O1	O0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	1	1	1	1

Register 2 – Polarity Inversion Register

This register allows the user to invert the polarity of the Input Port register data. If a bit in this register is set (written with ‘1’), the corresponding Input Port data is inverted. If a bit in this register is cleared (written with a ‘0’), the Input Port data polarity is retained.

Table 11. POLARITY INVERSION REGISTER

Bit	7	6	5	4	3	2	1	0
Symbol	N7	N6	N5	N4	N3	N2	N1	N0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Register 3 – Configuration Register

This register configures the directions of the I/O pins. If a bit in this register is set, the corresponding port pin is enabled as an input with high−impedance output driver. If a bit in this register is cleared, the corresponding port pin is enabled as an output. At reset, the I/Os are configured as inputs with a weak pull−up to V_{DD}.

Table 12. CONFIGURATION REGISTER

Bit	7	6	5	4	3	2	1	0
Symbol	C7	C6	C5	C4	C3	C2	C1	C0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	1	1	1	1

Power−on Reset

When power is applied to V_{DD}, an internal Power−On Reset (POR) holds the PCA9654E/PCA9654EA in a reset condition until V_{DD} has reached V_{POR}. At that point, the reset condition is released and the PCA9654E/ PCA9654EA registers and state machine will initialize to their default states. Thereafter, V_{DD} must be lowered below 0.2 V to reset the device.

For a power reset cycle, V_{DD} must be lowered below 0.2 V and then restored to the operating voltage.

Interrupt Output

The open−drain interrupt output is activated when one of the port pins changes state and the pin is configured as an input. The interrupt is deactivated when the input returns to its previous state or the Input Port register is read.

Note that changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

I/O Port (Figure 2)

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high−impedance input with a weak pull−up (100 kΩ typ.) to V_{DD}. The input voltage may be raised above V_{DD} to a maximum of 5.5 V.

If the I/O is configured as an output, then either Q1 or Q2 is enabled, depending on the state of the Output Port register. Care should be exercised if an external voltage is applied to an I/O configured as an output because of the low−impedance paths that exist between the pin and either V_{DD} or V_{SS}.

BUS TRANSACTIONS

Data is transmitted to the PCA9654E/PCA9654EA registers using the Write mode as shown in Figure 6 and Figure 7. Data is read from the PCA9654E/PCA9654EA registers using the Read mode as shown in Figure 8 and Figure 9. These devices do not implement an auto−increment function, so once a command byte has been sent, the register which was addressed will continue to be accessed by reads until a new command byte has been sent.

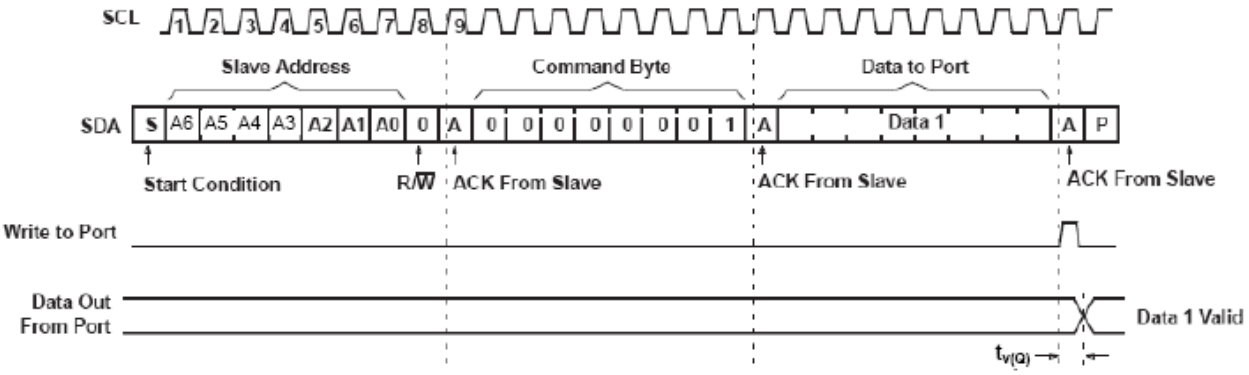


Figure 6. Write to Output Port Registers

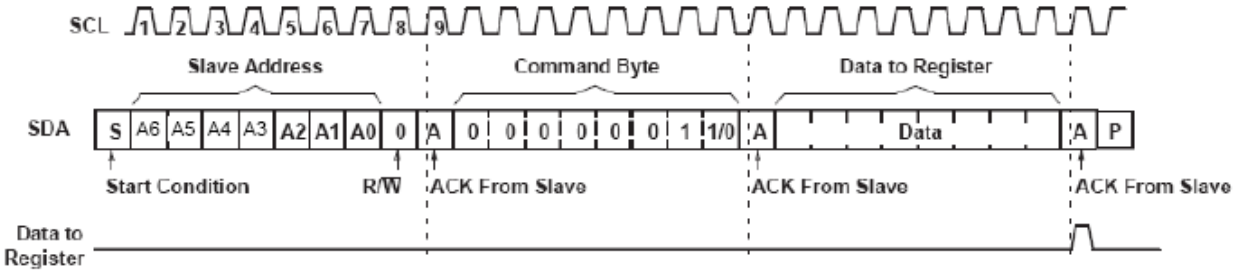


Figure 7. Write to Configuration or Polarity Inversion Register

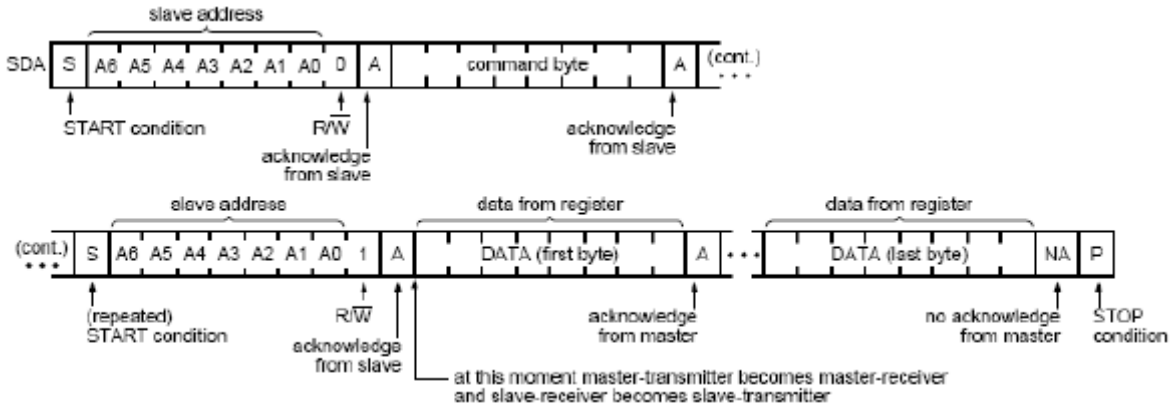
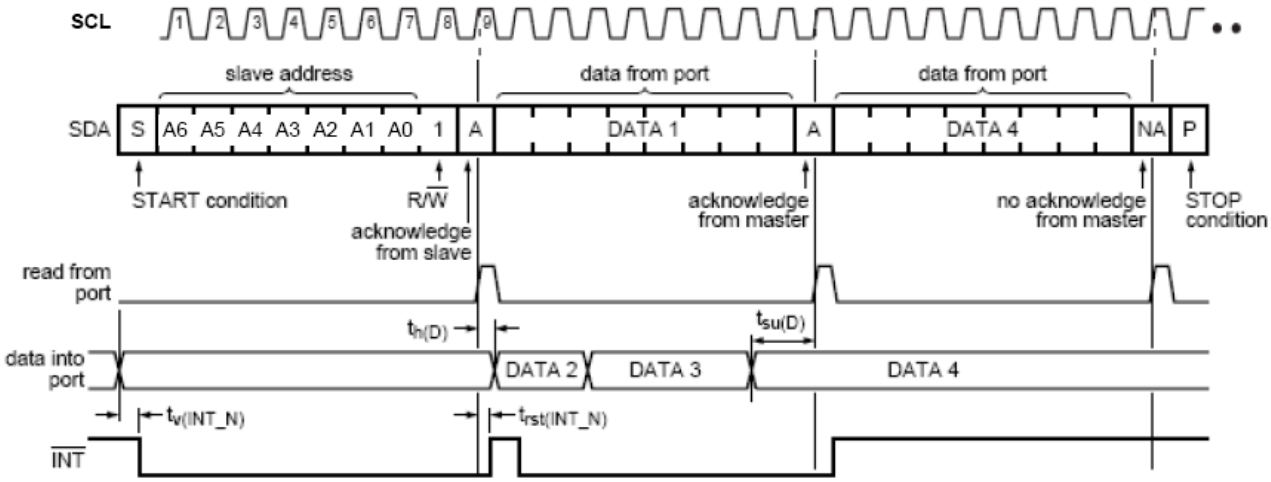


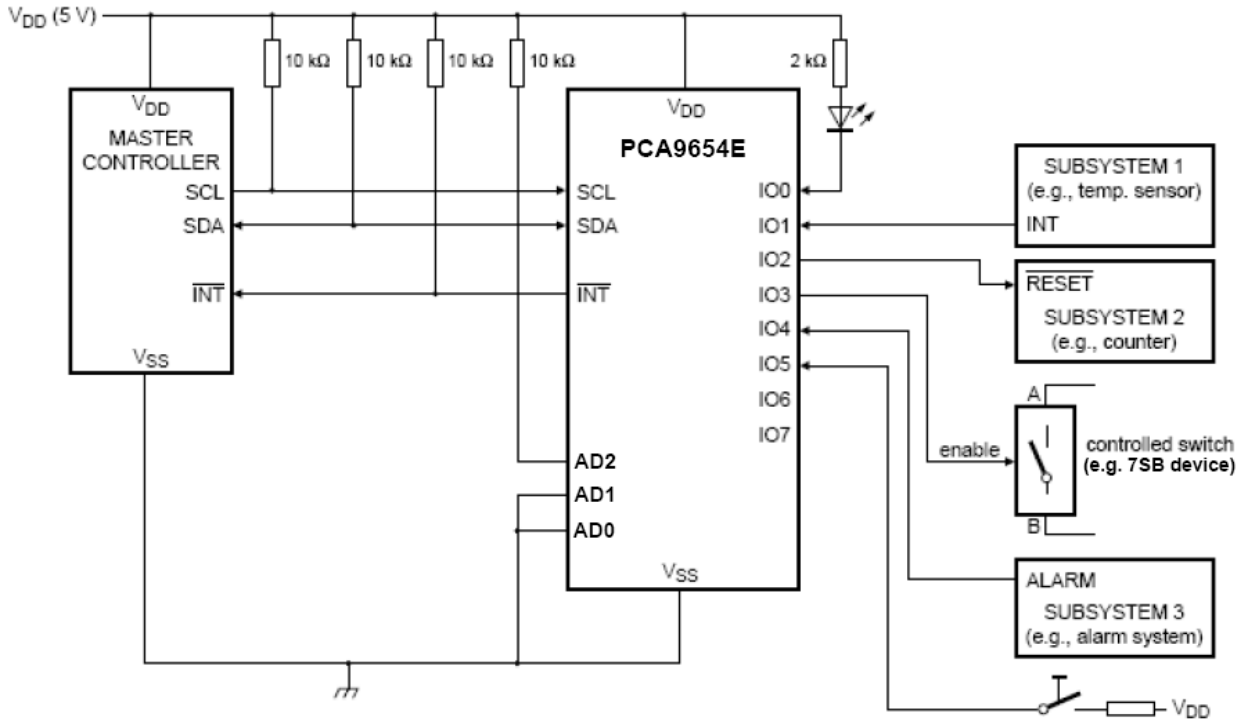
Figure 8. Read from Register



This figure assumes the command byte has previously been programmed with 00h.
Transfer of data can be stopped at any moment by a STOP condition.

Figure 9. Read Input Port Register

APPLICATION INFORMATION



Device address configured as 0100 100X for this example.
IO0, IO1, IO2 configured as outputs.
IO3, IO4, IO5 configured as inputs.
IO6 and IO7 are not used and must be configured as outputs.

Figure 10. Typical Application

Characteristics of the I²C−Bus

The I²C−bus is for 2−way, 2−line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull−up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 11).

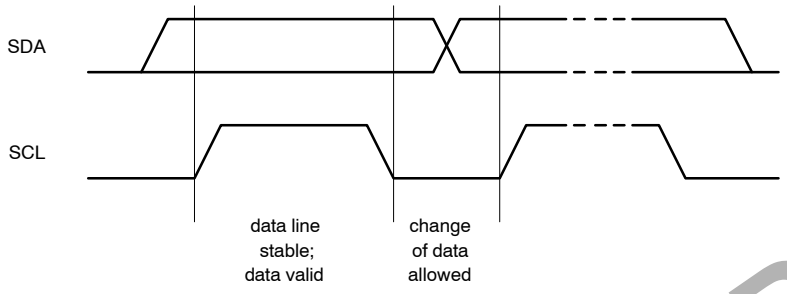


Figure 11. Bit Transfer

START and STOP Conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH−to−LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW−to−HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 12).

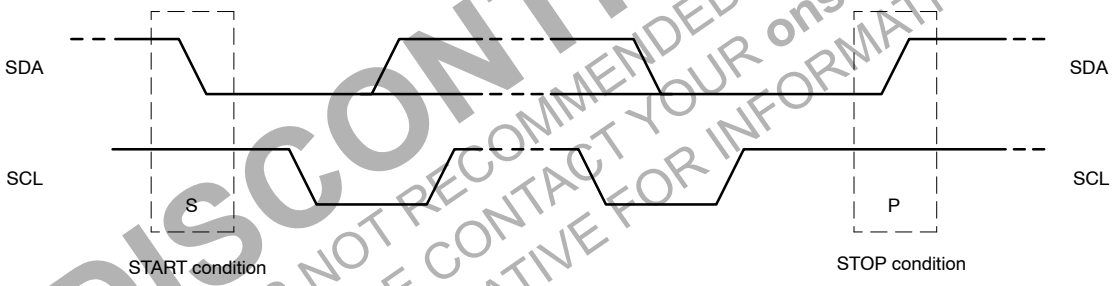


Figure 12. Definition of START and STOP Conditions

System Configuration

A device generating a message is a ‘transmitter’; a device receiving is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’ (see Figure 13).

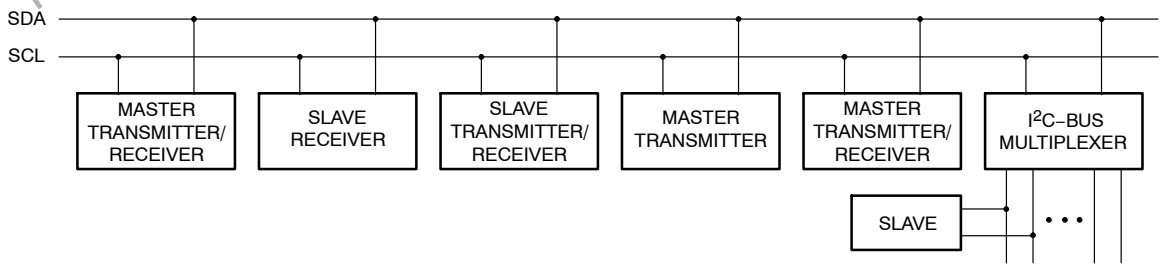


Figure 13. System Configuration

Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set−up time and hold time must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

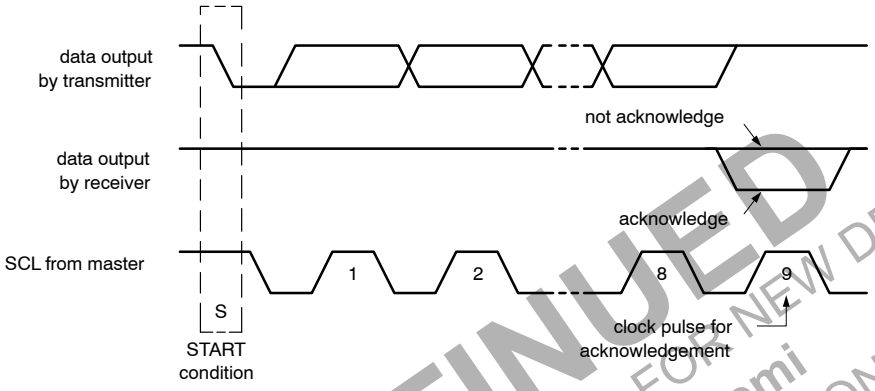


Figure 14. Acknowledgement of the I²C Bus

TIMING AND TEST SETUP

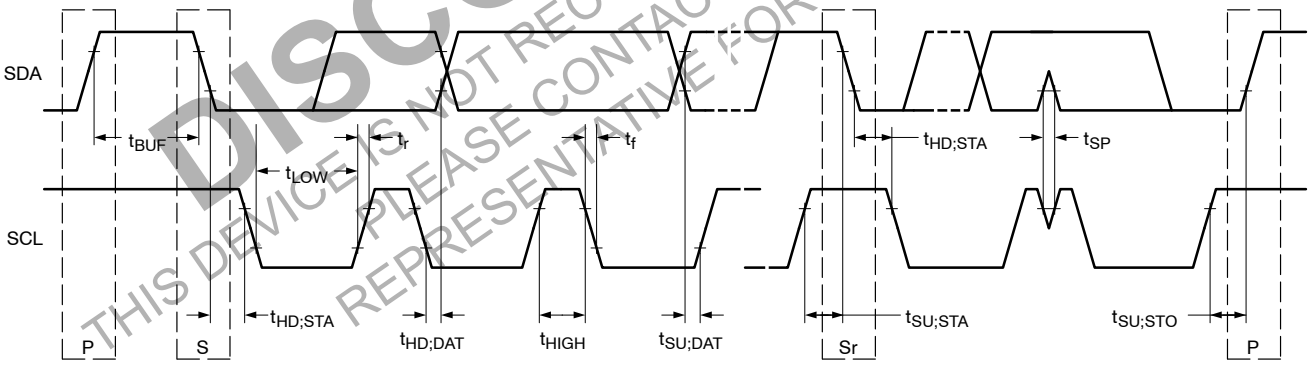
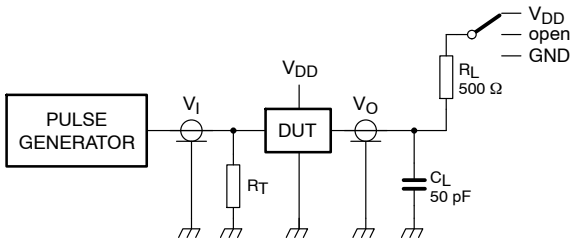


Figure 15. Definition of Timing on the I²C Bus



R_L = load resistor.
C_L = load capacitance includes jig and probe capacitance.
R_T = termination resistance should be equal to the output impedance of Z_o of the pulse generators.

Figure 16. Test Circuitry for Switching Times

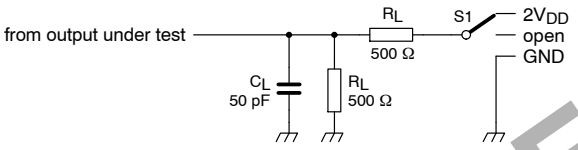


Figure 17. Load Circuit

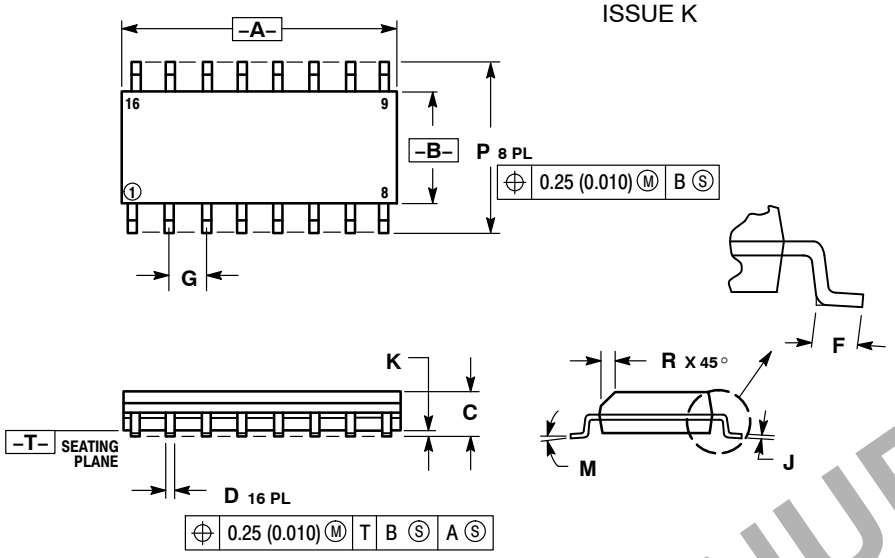
ORDERING INFORMATION

Device	Package	Shipping†
PCA9654EDR2G	SOIC−16 (Pb−Free)	2500 / Tape & Reel
PCA9654EDTR2G	TSSOP−16 (Pb−Free)	2500 / Tape & Reel
PCA9654EMTTBG (In Development)	WQFN16 (Pb−Free)	3000 / Tape & Reel
PCA9654E3MNTWG (In Development)	QFN16 (3x3) (Pb−Free)	3000 / Tape & Reel
PCA9654E4MNTWG (In Development)	QFN16 (4x4) (Pb−Free)	2000 / Tape & Reel
PCA9654EADR2G (In Development)	SOIC−16 (Pb−Free)	2500 / Tape & Reel
PCA9654EADTR2G (In Development)	TSSOP−16 (Pb−Free)	2500 / Tape & Reel
PCA9654EAMTTBG (In Development)	WQFN16 (Pb−Free)	3000 / Tape & Reel
PCA9654EA3MNTWG (In Development)	QFN16 (3x3) (Pb−Free)	3000 / Tape & Reel
PCA9654EA4MNTWG (In Development)	QFN16 (4x4) (Pb−Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

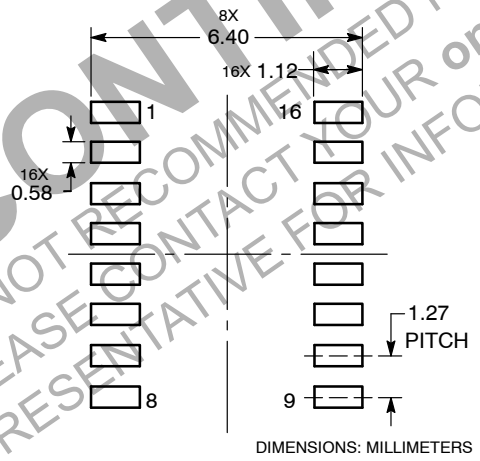
SOIC−16
CASE 751B−05
ISSUE K



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

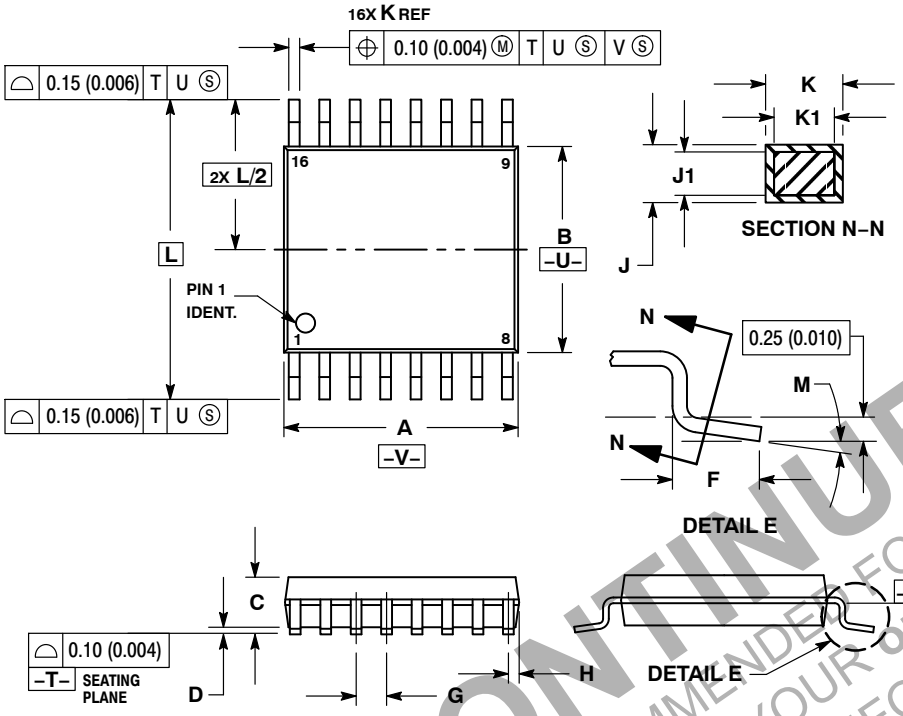
SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

PACKAGE DIMENSIONS

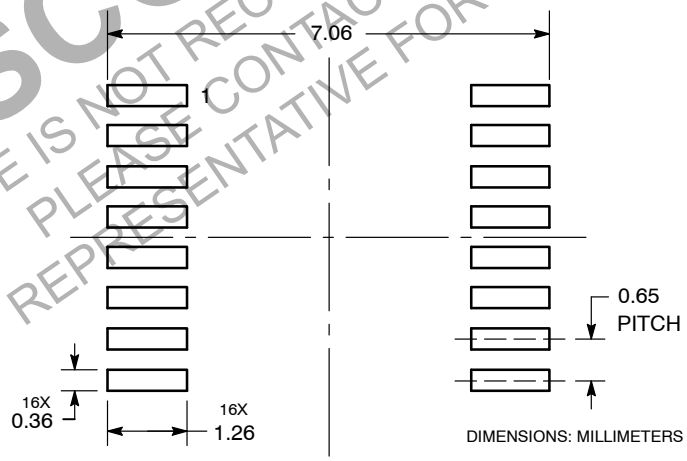
TSSOP−16
CASE 948F
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

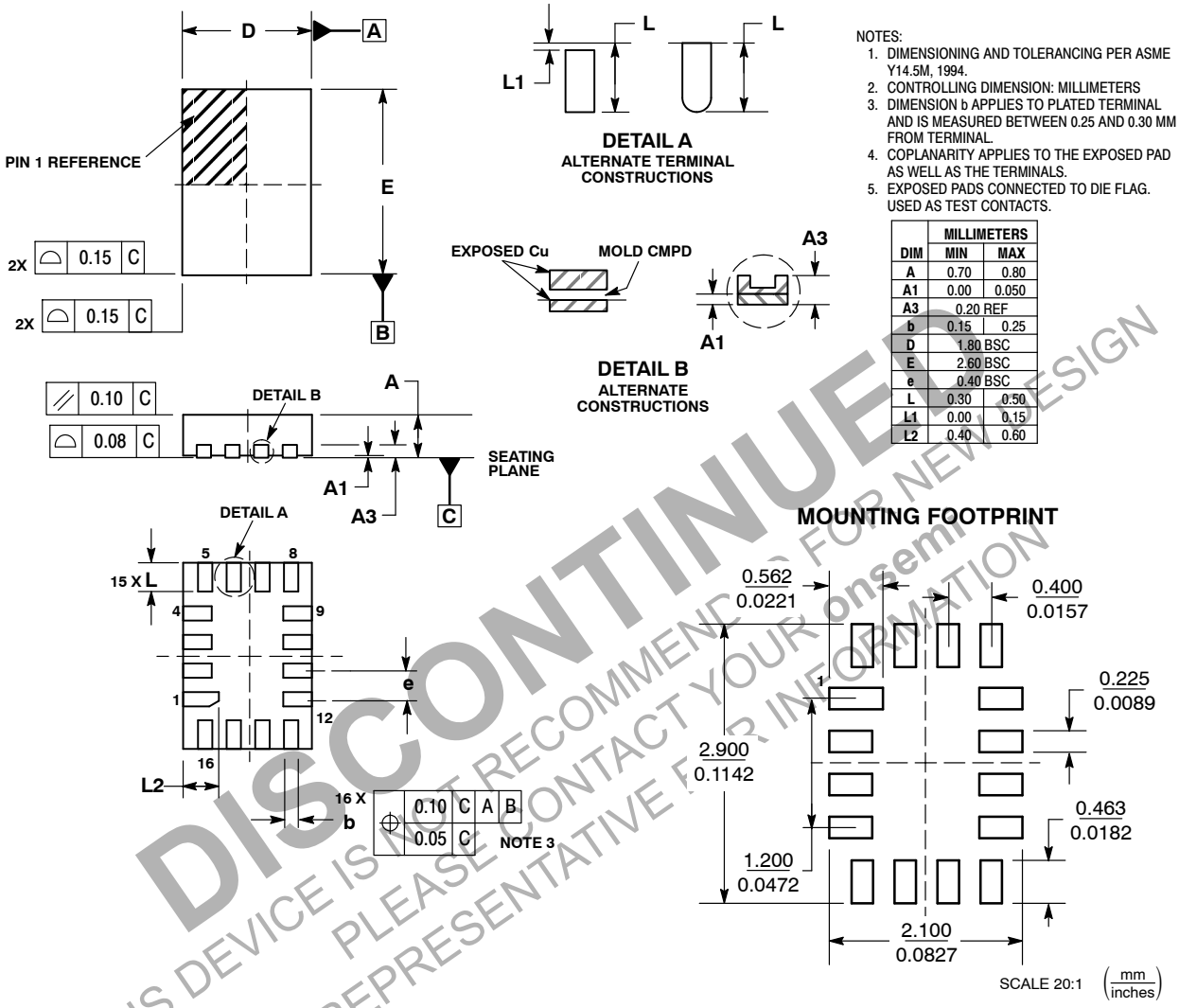
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



PACKAGE DIMENSIONS

WQFN16, 1.8x2.6, 0.4P
CASE 488AP
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. EXPOSED PADS CONNECTED TO DIE FLAG. USED AS TEST CONTACTS.

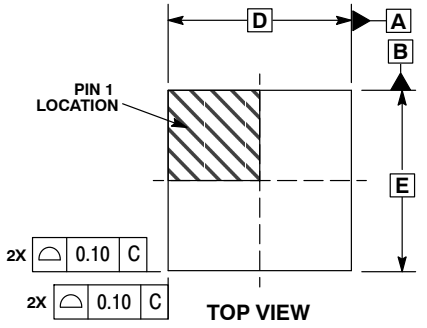
DIM	MILLIMETERS MIN	MAX
A	0.70	0.80
A1	0.00	0.050
A3	0.20 REF	
b	0.15	0.25
D	1.80 BSC	
E	2.60 BSC	
e	0.40 BSC	
L	0.30	0.50
L1	0.00	0.15
L2	0.40	0.60

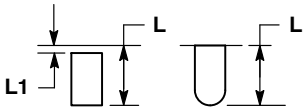
MOUNTING FOOTPRINT

SCALE 20:1 (mm / inches)

PACKAGE DIMENSIONS

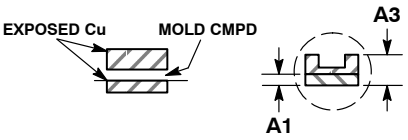
QFN16 3x3, 0.5P
CASE 485G
ISSUE F

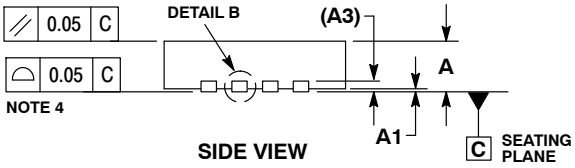


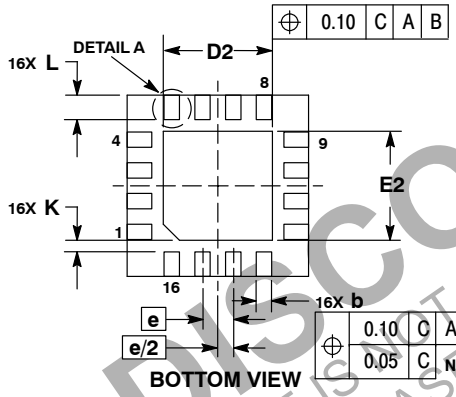


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

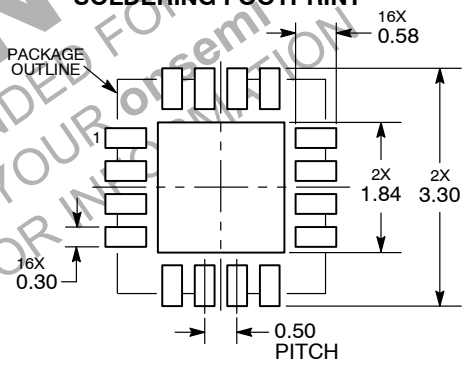
	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3		0.20 REF	
b	0.18	0.24	0.30
D		3.00 BSC	
D2	1.65	1.75	1.85
E		3.00 BSC	
E2	1.65	1.75	1.85
e		0.50 BSC	
K		0.18 TYP	
L	0.30	0.40	0.50
L1	0.00	0.08	0.15







RECOMMENDED SOLDERING FOOTPRINT*

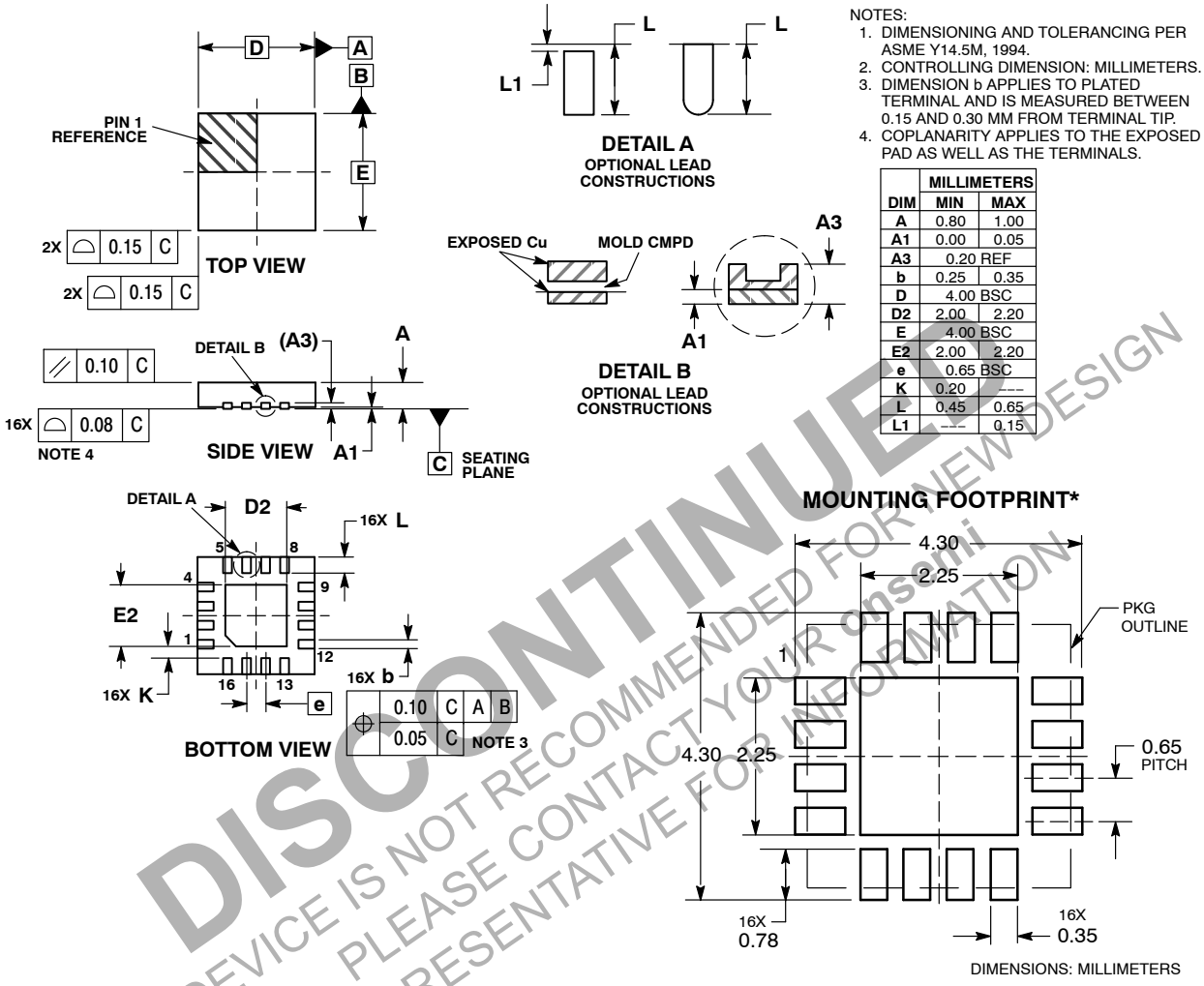


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

QFN16 4x4, 0.65P
CASE 485AP
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	4.00 BSC	
D2	2.00	2.20
E	4.00 BSC	
E2	2.00	2.20
e	0.65 BSC	
K	0.20	---
L	0.45	0.65
L1	---	0.15

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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