QPC7512

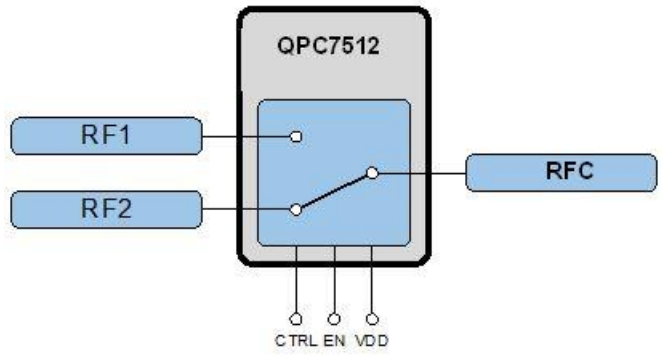
CATV SPDT Reflective Switch (5 – 3300 MHz)

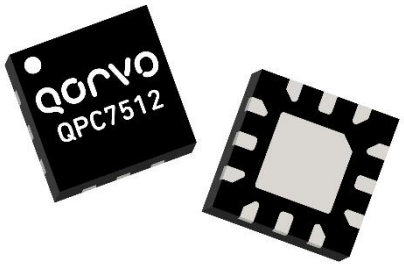
General Description

The QPC7512 is a high isolation Silicon on Insulator (SOI) single pole double throw (SPDT) reflective switch designed for use in CATV, satellite set top and other high-performance communications systems.

Featuring a single supply with a single CMOS/TTL compatible control line, QPC7512 features low insertion loss and high isolation throughout its bandwidth making it an optimal choice for operation from 5MHz to 3.3GHz. QPC7512 offers excellent linearity and power handling capability thanks to its SOI process and does not require blocking caps on the RF ports if DC is not present on the RF ports. QPC7512 is packaged in a space saving 2.0 x 2.0 mm 12 lead QFN.

Functional Block Diagram





2.0 x 2.0mm 12-lead QFN

Product Features

- 5MHz to 3300MHz Operation
- Optimized for 75Ω Applications (can be also be used in 50Ω applications).
- Low Insertion Loss: 0.22dB at 1GHz
- High Isolation: 42dB at 1GHz
- High IP3: 75dBm at 1GHz
- Compatible with Low Voltage Logic (V_{HIGH} Minimum = 1.3V)
- No External DC Blocking Capacitors Required on RF Paths Unless DC is Applied Externally
- 2000V HBM ESD Rating on All Ports

Applications

- Extended Spectrum DOCSIS
- CATV Amplifiers
- CATV Head End
- Fiber Deep Nodes
- Cable Set Top Box
- Satellite Set Top Box

Ordering Information

Part Number	Description
QPC7512SB	Sample Bag with 5 pieces
QPC7512SR	Short Reel with 100 pieces
QPC7512TR7	Standard Reel with 2,500 pieces
QPC7512PCK-01	75 Ω PCBA with 5-piece sample bag

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−50 to +150°C
Operating Temperature	−40 to +105°C
Maximum V_{DD}	6.0V
Maximum V_{EN}, V_{CTRL}	3.0V
PIN Max (CW)	+30dBm(5-25MHz) +33dBm (25-500MHz) +36dBm (>500MHz)
Hot Switching Max PIN (75ohm Load)	+30dBm

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Device Voltage (V_{DD})	+2.7	+5.0	+5.5	V
Device Current, 5V (I_{DD})		91		µA
Device Current, 3V (I_{DD})		85		
V_{EN}, V_{CTRL} High	1.3		2.7	V
V_{EN}, V_{CTRL} Low	0		0.45	V

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Conditions(1)	Min	Typ	Max	Units
Operational Frequency Range (1)		5		3300	MHz
Insertion Loss	5MHz		0.15		dB
	5-1000MHz		0.22		dB
	1000-2000MHz		0.33		dB
	2000-3000MHz		0.40		dB
	3300MHz		0.45		dB
Isolation, RFC - RFx	5 – 50MHz		71		dB
	50-1000MHz		42		dB
	1000-2000MHz		35		dB
	2000-3000MHz		29		dB
	3300MHz		27		dB
Isolation, RF1 – RF2	5 – 50MHz		71		dB
	50-1000MHz		43		dB
	1000-2000MHz		35		dB
	2000-3000MHz		29		dB
	3300 MHz		27		dB
Input Return Loss; RFC	5 – 50MHz		40		dB
	50-1000MHz		22		dB
	1000-2000MHz		20		dB
	2000-3000MHz		23		dB
	3300MHz		33		dB
Output Return Loss; RFx	5 – 50MHz		40		dB
	50-1000MHz		22		dB
	1000-2000MHz		20		dB
	2000-3000MHz		23		dB
	3300 MHz		28		dB

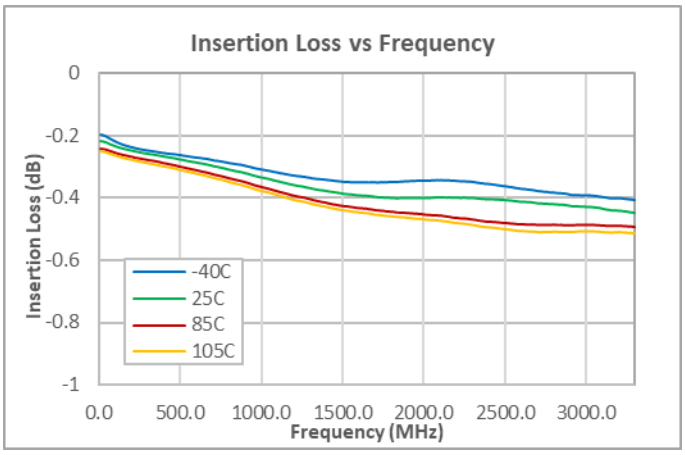
Notes:
1. Test conditions unless otherwise noted: V_{DD} = +3.3V, Temp = +25°C, 75Ω test system, QPC7512-4000(C) EVB.

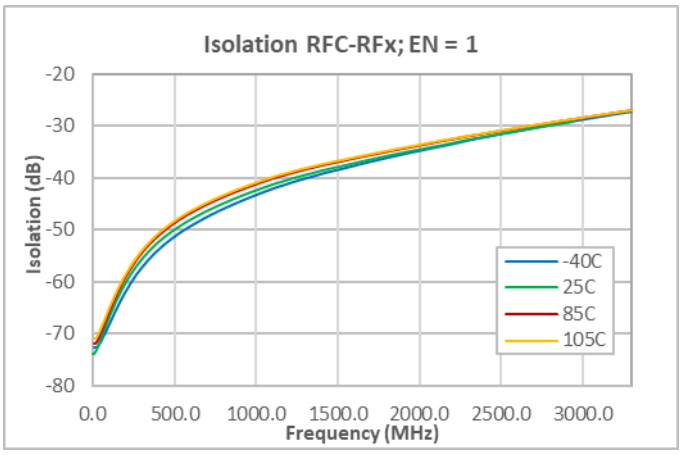
Electrical Specifications (cont'd.)

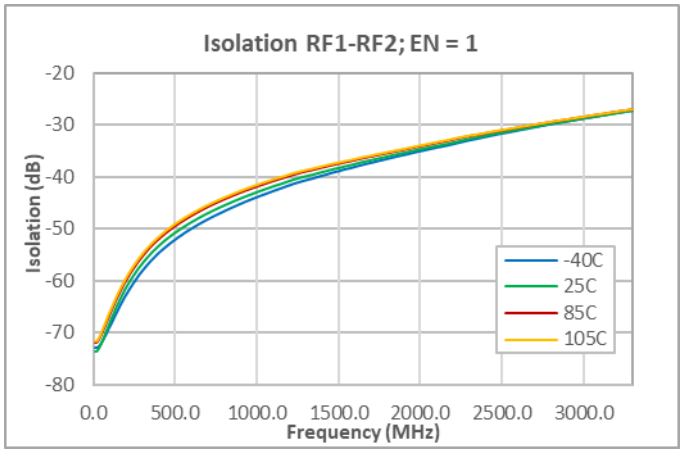
Parameter	Conditions[1]	Min	Typ	Max	Units
P0.1 dB Compression [2][3]	5MHz		34		dBm
	10-50MHz		36		
	50-3300MHz		43		
CSO	41dBmV/ch, 137 Channels		>100		dBc
CTB	41dBmV/ch, 137 Channels		>100		dBc
XMOD	41dBmV/ch, 137 Channels		>90		dBc
2nd Harmonic	17MHz, 12dBm tone		-102.3		dBc
3rd Harmonic	17MHz, 12dBm tone		-119.9		dBc
Output IP2	1000MHz, 12dBm per tone		133.0		dBm
Output IP3	1000MHz, 12dBm per tone		74.8		dBm
Internal Spurious[4]	F = 2MHz		-154		dBm/Hz
	F > 5MHz		-157		
Switching Time	50% Control to 10% / 90% RF		2	5	µS

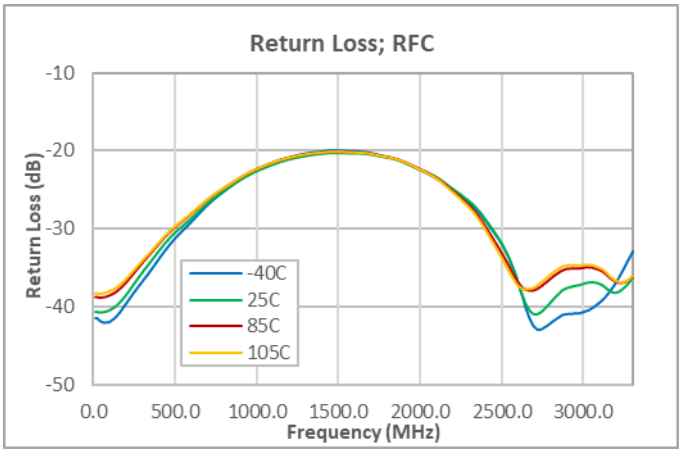
Notes:
1. Test conditions unless otherwise noted: V_{DD} = +3.3 V, Temp = +25°C, 75Ω test system.
2. Measured in a 50 Ω system.
3. Exceeds Absolute Maximum Power Handling limit. Not recommended for operation.
4. Fundamental peak at 2MHz. Resolution bandwidth 100KHz.

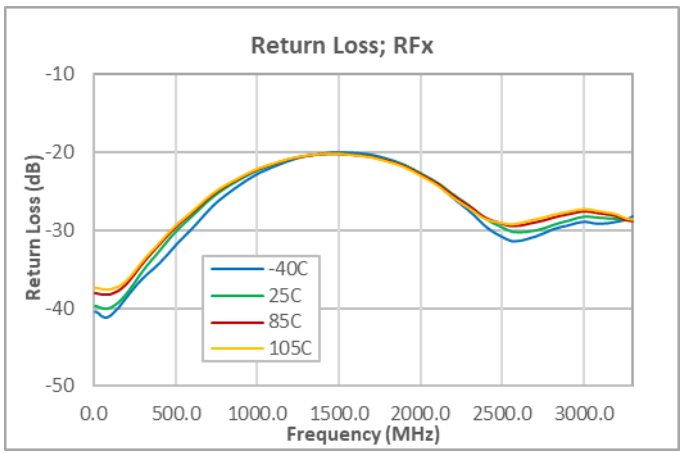
Performance Plots

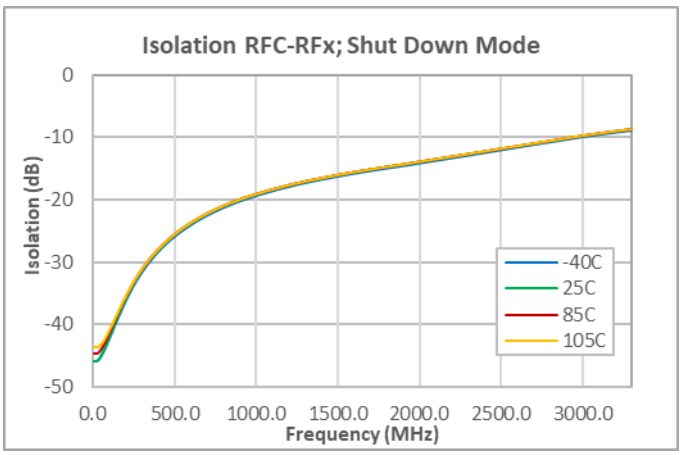








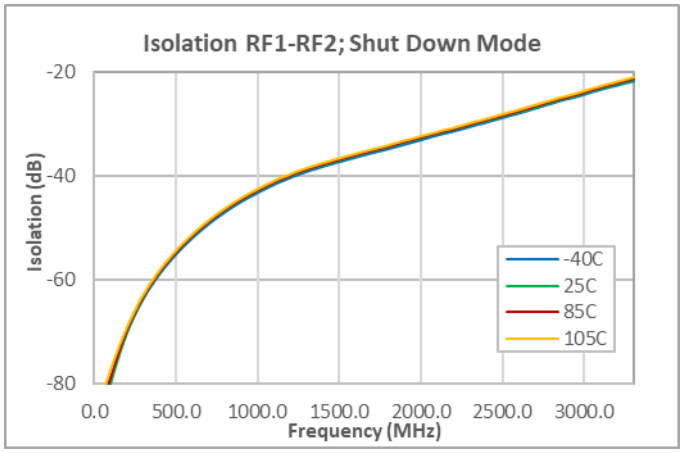


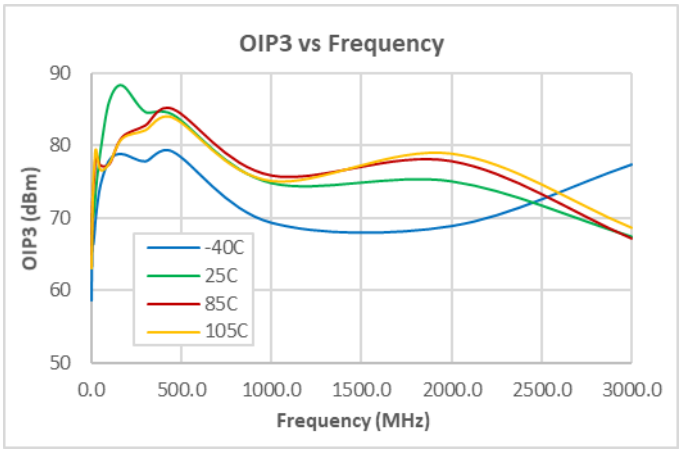


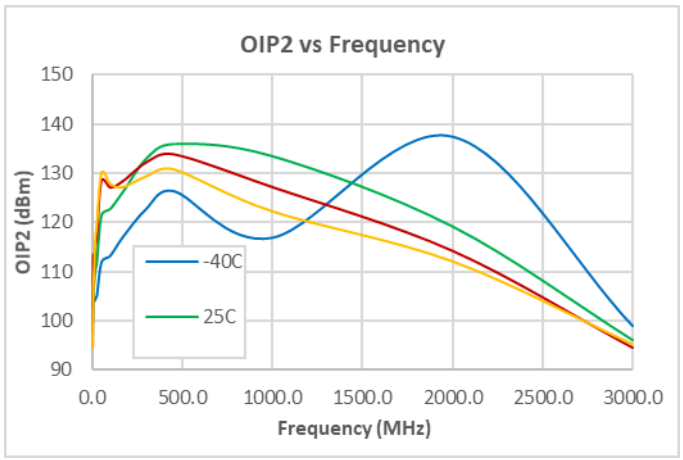
Test Conditions:

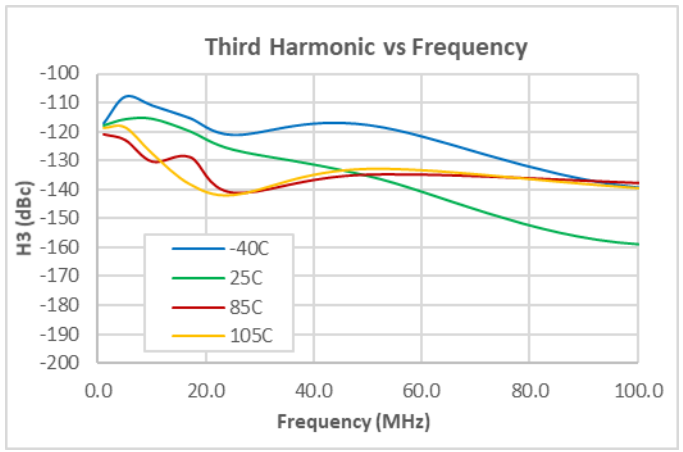
1. Test conditions unless otherwise noted: V_{DD} =+3.3V, Z_o = 75Ω

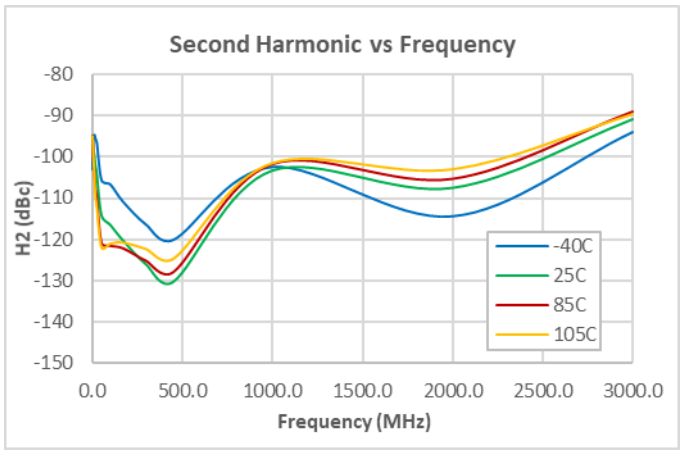
Performance Plots (cont'd.)

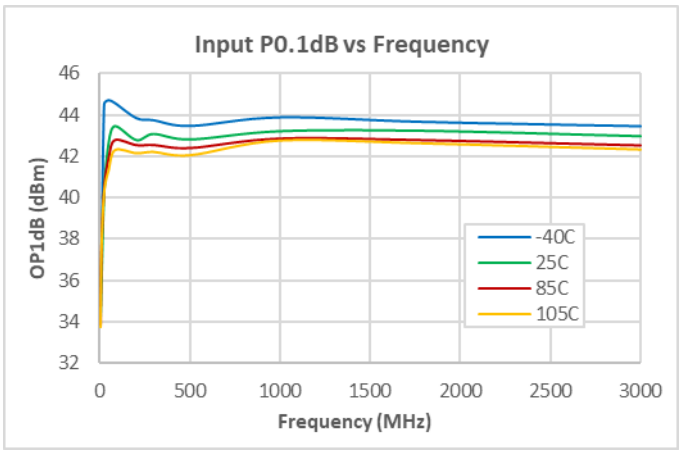








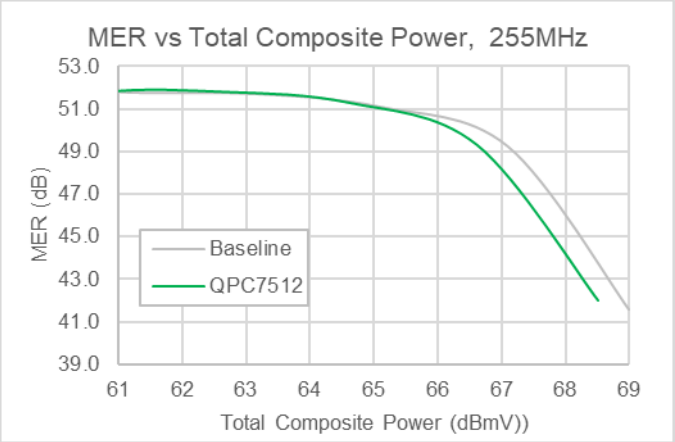


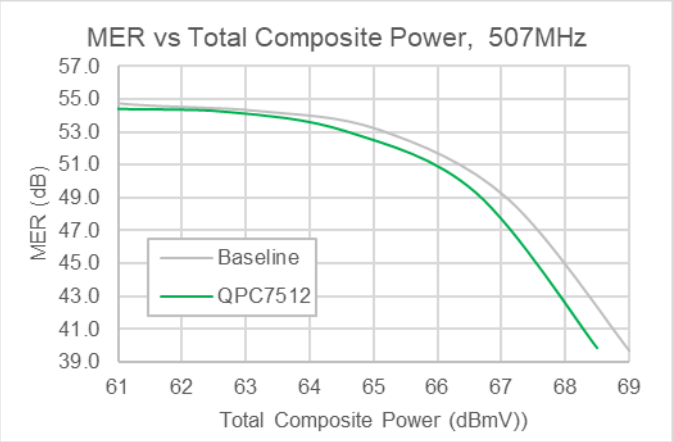


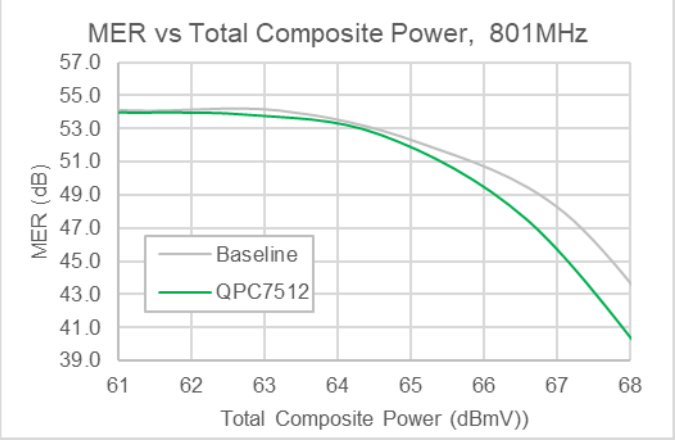
Test Conditions:

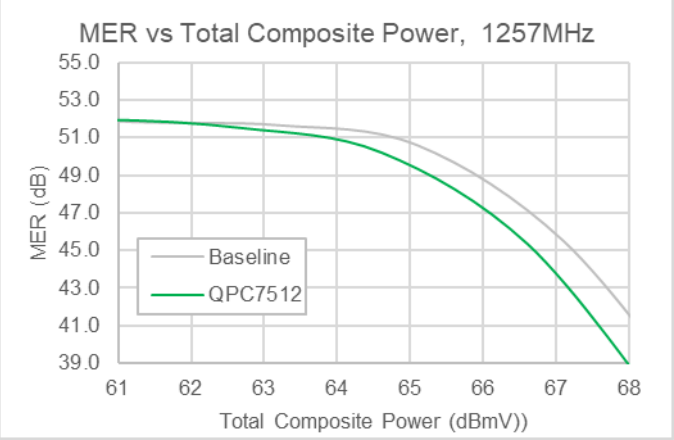
1. Test conditions unless otherwise noted: V_{DD} =+3.3V, Z_o = 75Ω, QPC7512-4000(C) EVB
2. IIP3, IP2: 75Ω, +12dBm per tone.

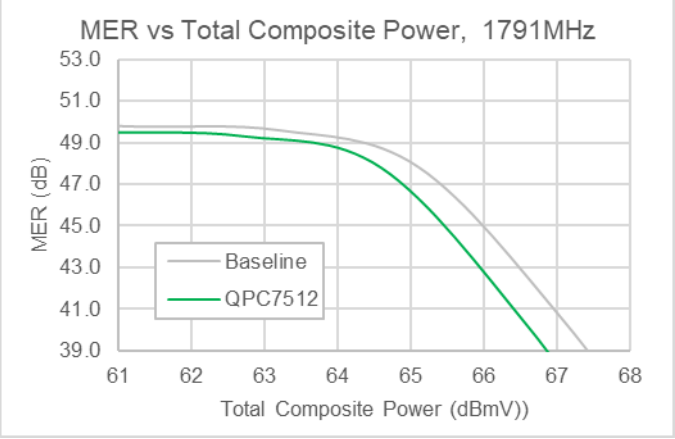
Performance Plots (cont'd.)

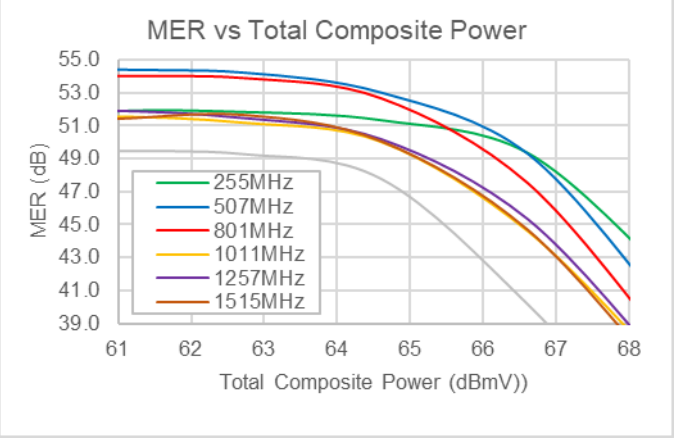








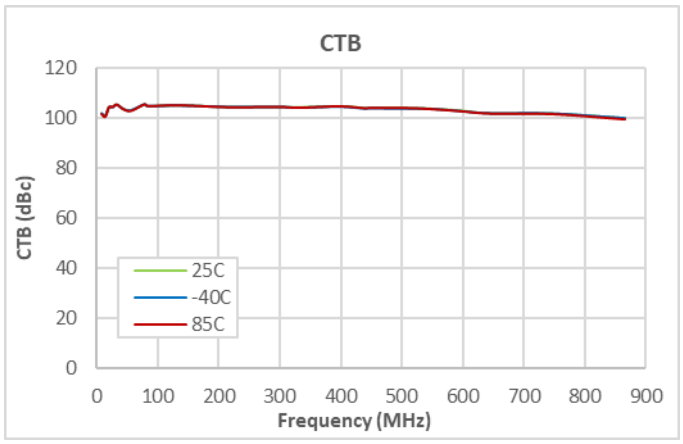


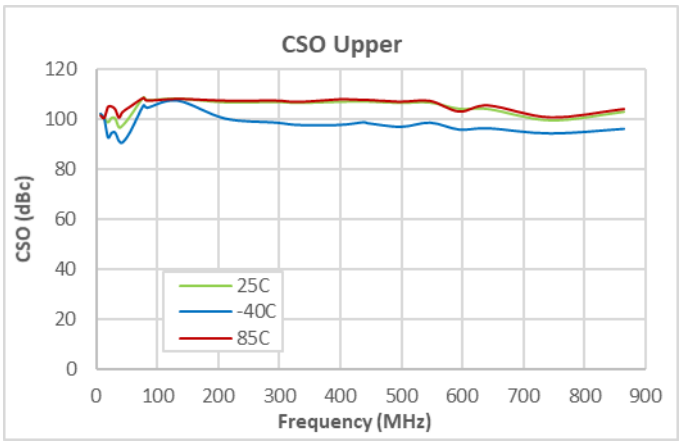


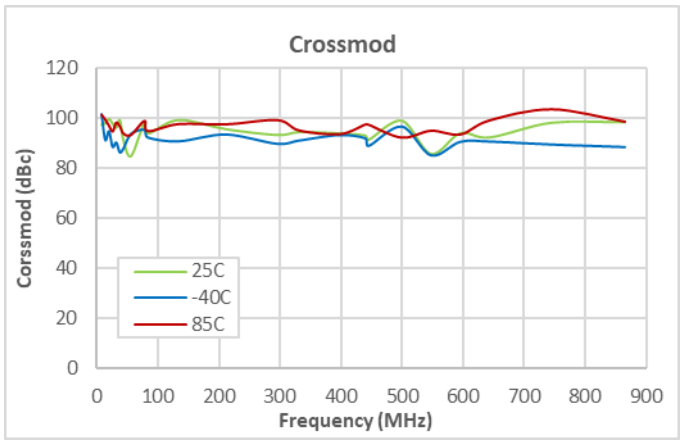
Test Conditions:

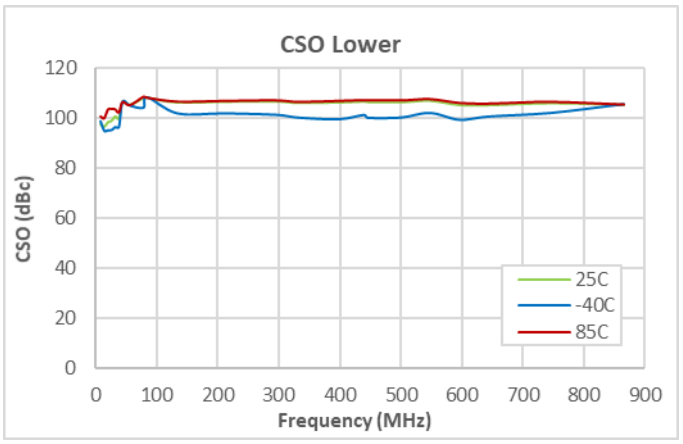
1. Test conditions unless otherwise noted: V_{DD} =+3.3V, Z_o = 75Ω, QPC7512-4000(C) EVB
2. 280Ch 256QAM ITU-T J.83 Annex B; 108-1791MHz; 0dB Tilt, 0dB Offset. Source Corrected (4.3dB maximum correction). Baseline represents QPL1823 8V output.

Performance Plots (cont'd.)





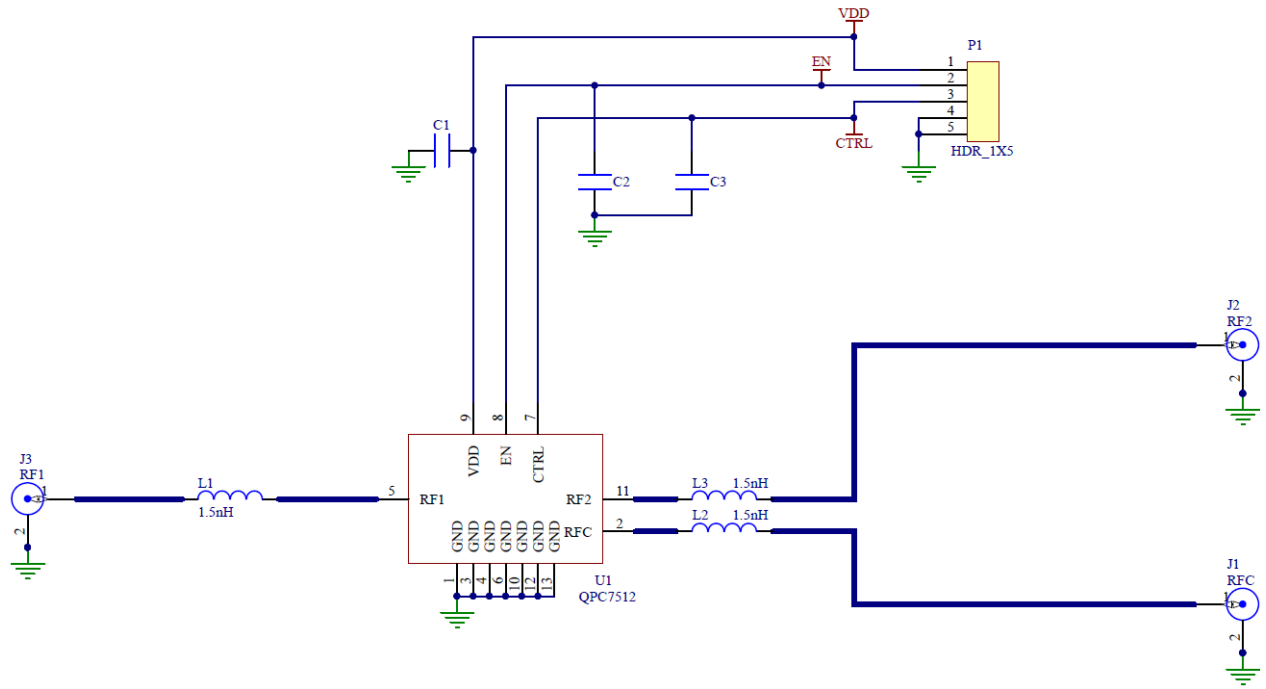




Test Conditions:

1. Test conditions unless otherwise noted: V_{DD} =+3.3V, Z_o = 75Ω
2. 41dBmV/Channel, 137 Channels, Flat Tilt.

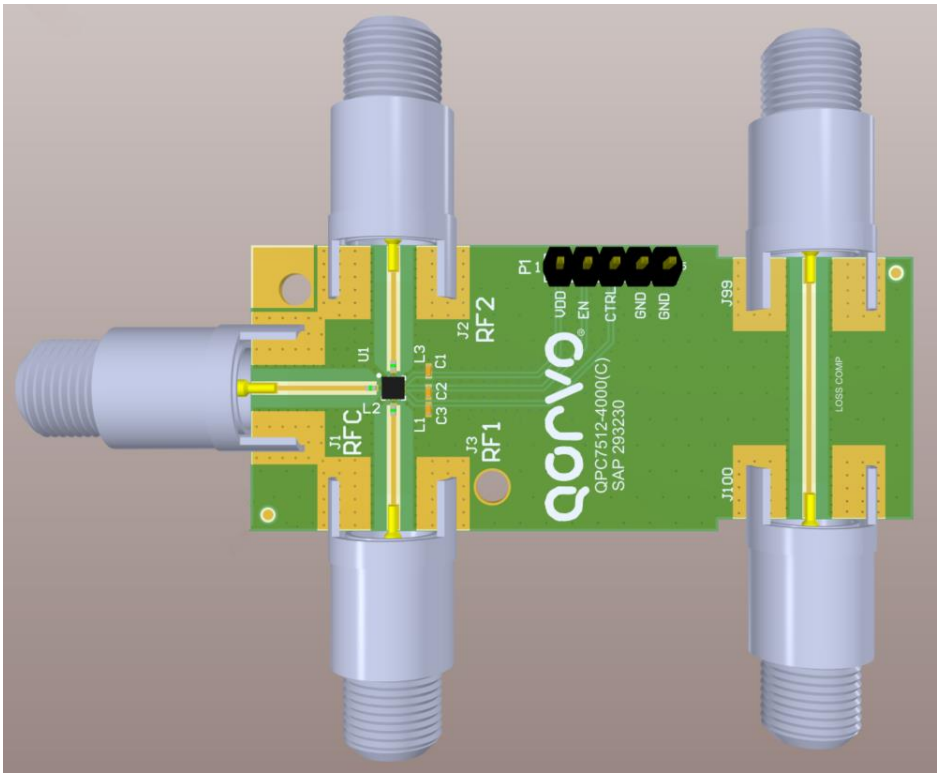
Evaluation Board Schematic; QPC7512-4000(C)



Evaluation Board Bill of Materials

Ref Designator	Description	Manufacturer	Part Number
PCB	PCB, QPC7512	Qorvo	QPC7512-4000(C)
U1	QPC7512 Switch	Qorvo	QPC7512
C1	CAP, 0.01uF, 10%, 25V, X8R, 0402	TDK	C1005X8R1E103K
C2, C3	CAP, 100pF, 1%, 50V, C0G, 0402	AVX Asia Limited	04025A101FAT2A
L1, L2, L3	IND, 1.5nH, +/-0.1nH, M/L, 0402	Murata	LQG15HS1N5B02D
P1	CONN, HDR, ST, 5-PIN, 0.100"	Sullins	PBC05SAAN
J1, J2, J3, J99, J100	CONN, F FEM EDGE MOUNT, 75 OHMS, 0.065"	Genesis Technology USA	GT20-300204

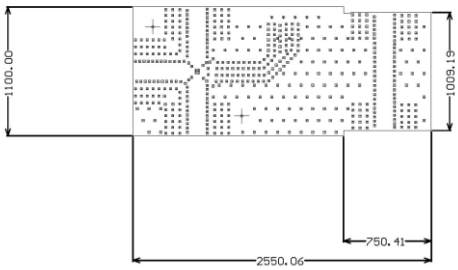
Evaluation Board Layout; QPC7512-4000(C)



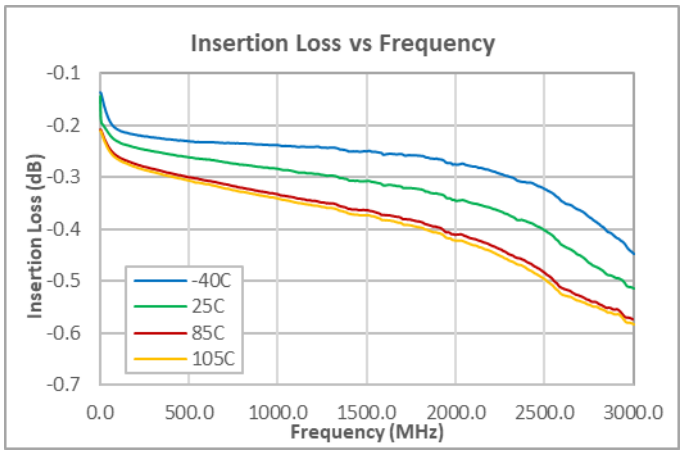
EVB PCB Material and Stack-up

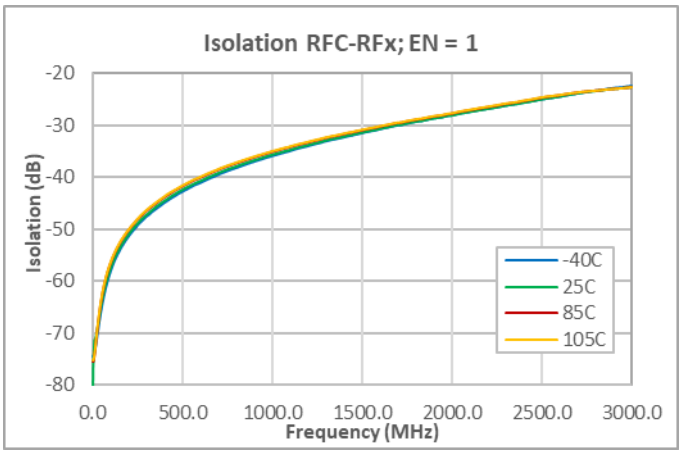
Board Material: 0.020" RO4003C, ε_r=3.38
Final Plating: 0.5oz Copper
Board Dimension: 1.1" x 2.55"
Total Thickness: 50.2 mils

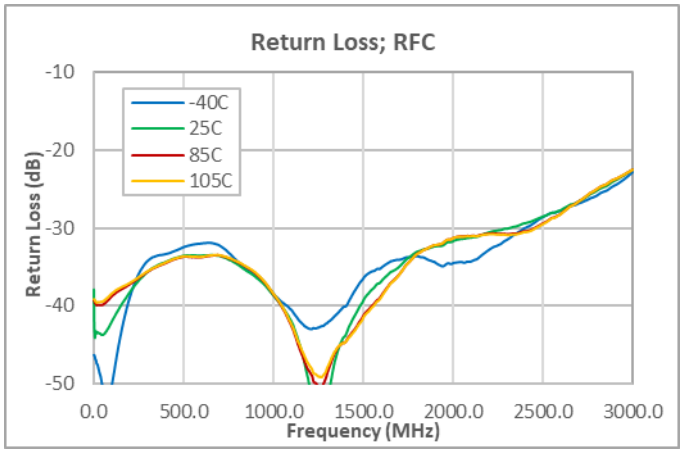
Layer	Name	Material	Thickness	Constant
1	Top Overlay			
2	Top Solder	Solder Resist	0.40mil	3.5
3	Top Layer	Copper	0.70mil	
4	Dielectric1	RO4003C	20.00mil	3.38
5	MidLayer1	Copper	1.40mil	
6	Dielectric2	370HR	4.22mil	3.7
7	MidLayer2	Copper	1.40mil	
8	Dielectric3	370HR	21.00mil	4.34
9	Bottom Layer	Copper	0.70mil	
10	Bottom Solder	Solder Resist	0.40mil	3.5

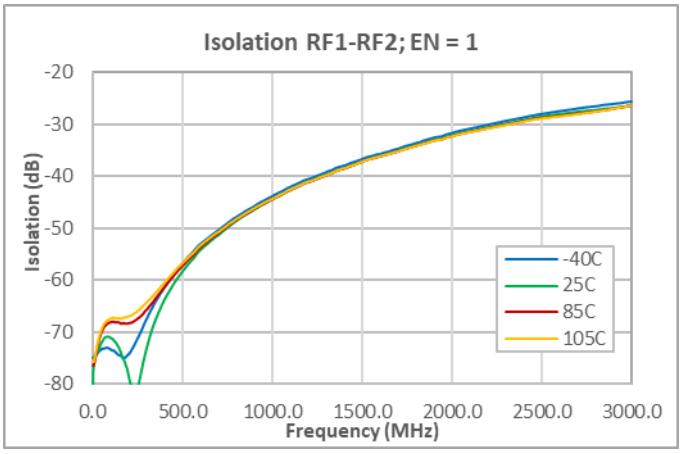


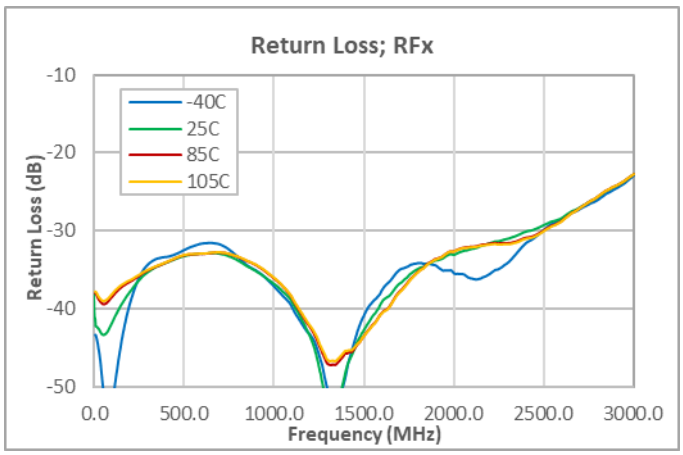
Additional Applications; Low Frequency Isolation Improvement

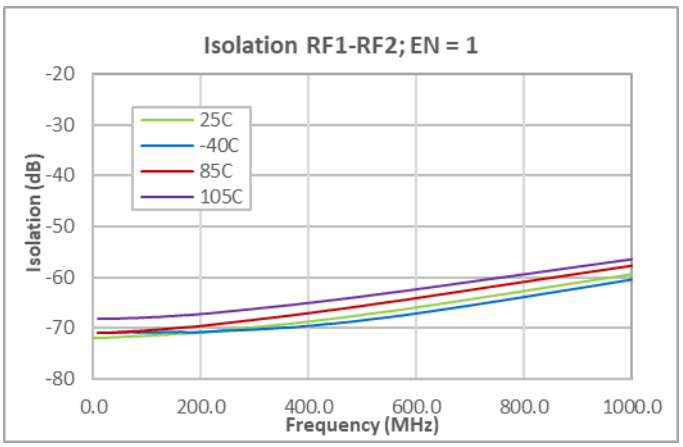








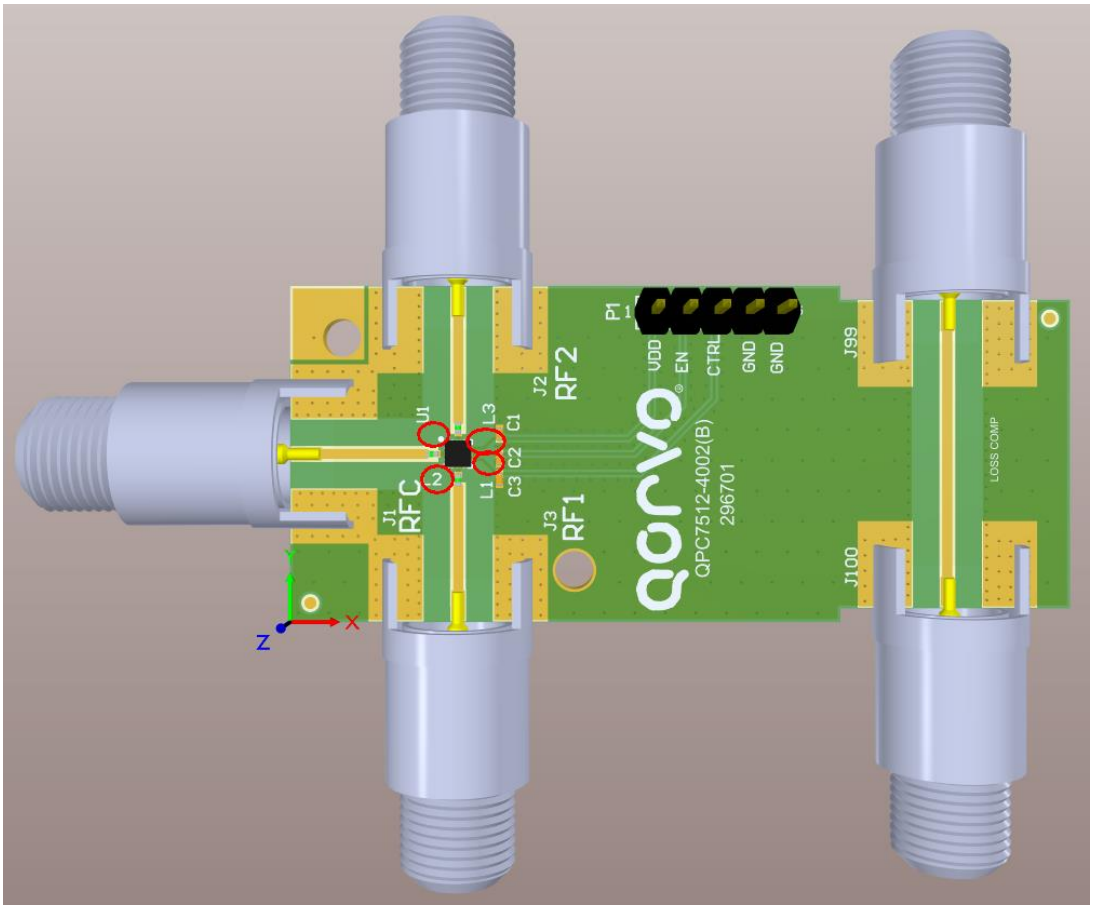




Test Conditions:

1. Test conditions unless otherwise noted: V_{DD} =+5V, Z_o = 75Ω, QPC7512-4002(B) EVB (pg 11)

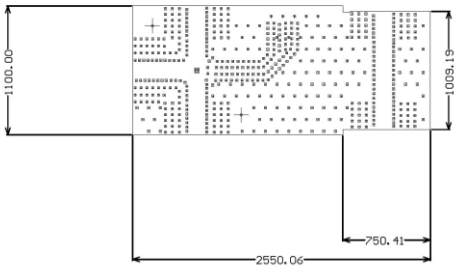
Additional Applications; Low Frequency Isolation Improvement, QPC7512-4002(B)



EVB PCB Material and Stack-up

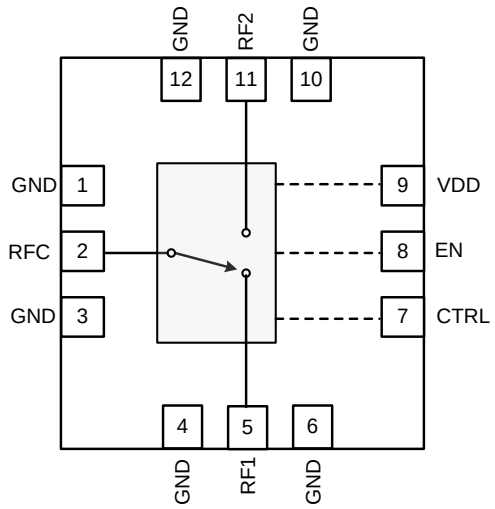
Board Material: 0.032" RO4003C, ε_r=3.38
Final Plating: 0.5oz Copper
Board Dimension: 1.1" x 2.55"
Total Thickness: 62.9 mils

Layer	Name	Material	Thickness	Constant
1	Top Overlay			
2	Top Solder	Solder Resist	0.40mil	3.5
3	Top Layer	Copper	0.70mil	
4	Dielectric1	RO4003C	32.00mil	3.38
5	MidLayer1	Copper	1.40mil	
6	Dielectric2	370HR	5.90mil	3.7
7	MidLayer2	Copper	1.40mil	
8	Dielectric3	370HR	20.00mil	4.34
9	Bottom Layer	Copper	0.70mil	
10	Bottom Solder	Solder Resist	0.40mil	3.5



1. Low frequency RF1-RF2 isolation can be improved using microstrip topology and not connecting top copper ground plane between the ports (refer to QPC7512-4002 layout shown above). RFC-RFx isolation and ioslation above 1.2GHz will begin to degrade versus using top copper isolating ground.
2. QPC7512-4000 EVB layout (pg. 9) uses microstrop toplogy with isolating ground connected between ports to improve RFC-RFx isolation and 1.2 to 3.3GHz isolation.
3. Thicker dielectrics can also employ CPWG with solid ground between the ports to improve isolation.
4. Matching inductors L1, L2, L3 are used to improve return loss through 3.3GHz. For operation over lower bandwidths, the inductors may be reduced or eliminated to reduce loss.
5. L1, L2, L3 adjusted to 1.1nH (LQG15HS1N1B02D) to improve return loss through 1.8GHz.

Pin Configuration and Description



Top View

Pin Number	Label	Description
1, 3	GND	No internal connection but recommend connecting to ground for proper mounting integrity.
4, 6, 10, 12	GND	Internally connected and must be grounded on board.
2	RFC	Single ended Common Port.
5	RF1	Single Ended RF port.
7	CTRL	Switch logic control input.
8	EN	Shutdown logic control input.
9	VDD	Supply Voltage.
11	RF2	Single ended RF port.
Backside Pad	GND	Ground connection. The back side of the package should be soldered to the ground plane. PCB vias under the device are required.

Notes:
1. Both RF pins must be held at $0V_{DC}$ or require external DC blocking capacitors.
2. The ground paddle must be soldered to the ground plane for proper switch performance.

Power Up / Down and Operational Controls

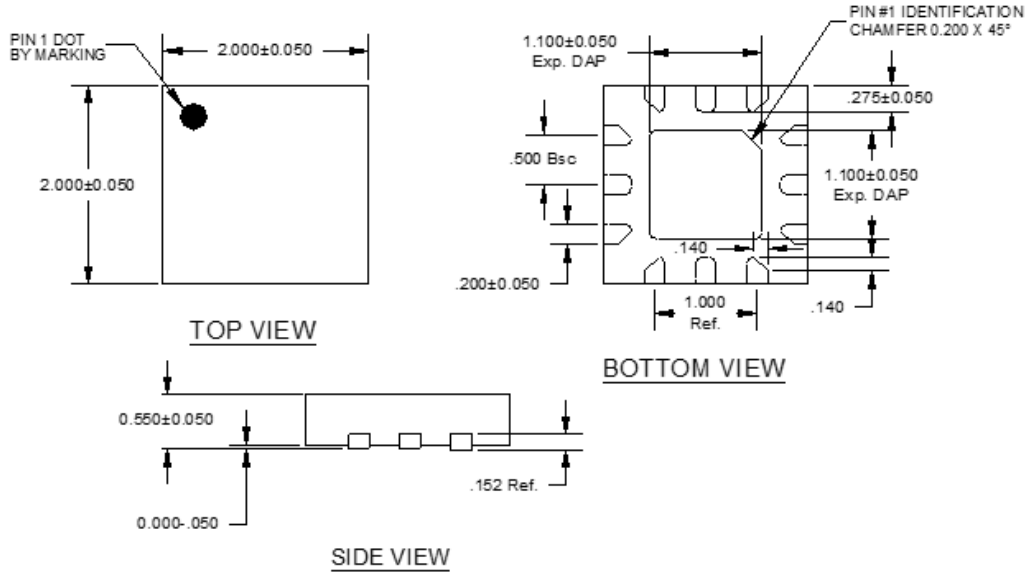
Scenario 1	Sequence for power up and power down from the supply that is connected to QPC7522 VDD Pin.
Power Up	Turn on VDD (supply), then EN, then CTRL. Then (20 µs or greater), apply RF signal.
Power Down	Turn off RF signal, then CTRL, then EN, turn off VDD (supply).
Scenario 2	Sequence for going in and out of shutdown mode, keeping the VDD supply on, but disabling/enabling QPC7522 by the EN pin.
Power Up	Turn on EN (enable), then CTRL, then (5 µs or greater), turn on RF Signal.
Power Down	Turn off RF signal, then CTRL, then EN (disable).
Scenario 3	When changing switch positions between RF1 and RF2, no RF signal should be applied to any RF.
Switching Ports	Turn off RF signal, then change CTRL state, then wait (5 µs or greater), then turn on RF signal.

Note: Hot switching of RF signals allowable within Abs Max limits on pg2.

Logic Table

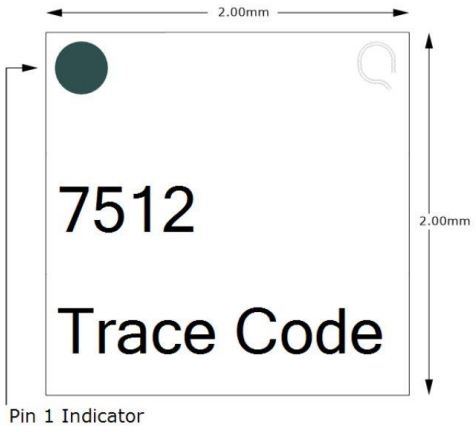
V_{CTRL}	V_{EN}	RFC-RF1	RFC-RF2
1	1	OFF	ON
0	1	ON	OFF
X	0	OFF	OFF
VDD = 2.7 – 5.0 V			

Package Dimensions



Notes:
1. All dimensions are in millimeters. Angles are in degrees.

Package Marking



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 2 (2000V)	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	C3 (1000V)	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 1	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) soldering process.
Solder profiles available upon request.

Contact plating: MatteSn

RoHS Compliance

This part is compliant with EU 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU. This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Tel: 1-844-890-8163

Web: www.qorvo.com

Email: customer.support@qorvo.com

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