S-19100xxxA Series

AUTOMOTIVE, 125°C OPERATION, 10 V VOLTAGE DETECTOR WITH DELAY FUNCTION (EXTERNAL DELAY TIME SETTING)

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The S-19100xxxA Series, developed by using CMOS technology, is a voltage detector IC for automotive 125°C operation. The detection voltage is fixed internally with an accuracy of ±3.0% ($-V_{DET}$ = 2.4 V). It operates with current consumption of 270 nA typ.
The release signal can be delayed by setting a capacitor externally, and the delay time accuracy at Ta = +25°C is ±15%. The operation temperature range is Ta = −40°C to +125°C. Two output forms Nch open-drain and CMOS output are available.
Compared with conventional CMOS voltage detectors, the S-19100xxxA Series has super-low current consumption and small packages.

ABLIC Inc. offers FIT rate calculated based on actual customer usage conditions in order to support customer functional safety design.
For more information regarding our FIT rate calculation, contact our sales representatives.

Caution This product can be used in vehicle equipment and in-vehicle equipment. Before using the product for these purposes, it is imperative to contact our sales representatives.

■ Features

- Detection voltage: 1.2 V to 4.6 V (0.1 V step)
- Detection voltage accuracy: ±3.0% (2.4 V ≤ $-V_{DET}$ ≤ 4.6 V, Ta = −40°C to +125°C)
  ±(2.5% + 12 mV) (1.2 V ≤ $-V_{DET}$ < 2.4 V, Ta = −40°C to +125°C)
- Current consumption: 270 nA typ. (1.2 V ≤ $-V_{DET}$ < 2.3 V)
- Operation voltage range: 0.6 V to 10.0 V (CMOS output product)
- Hysteresis width*1: 5% ±2% (Ta = −40°C to +125°C)
- Delay time accuracy: ±15% (C_D = 4.7 nF, Ta = +25°C)
- Output form: Nch open-drain output (active "L")
  CMOS output (active "L")
- Operation temperature range: Ta = −40°C to +125°C
- Lead-free (Sn 100%), halogen-free
- AEC-Q100 qualified*2

***1.** The product without hysteresis width is also available.
***2.** Contact our sales representatives for details.

■ Applications

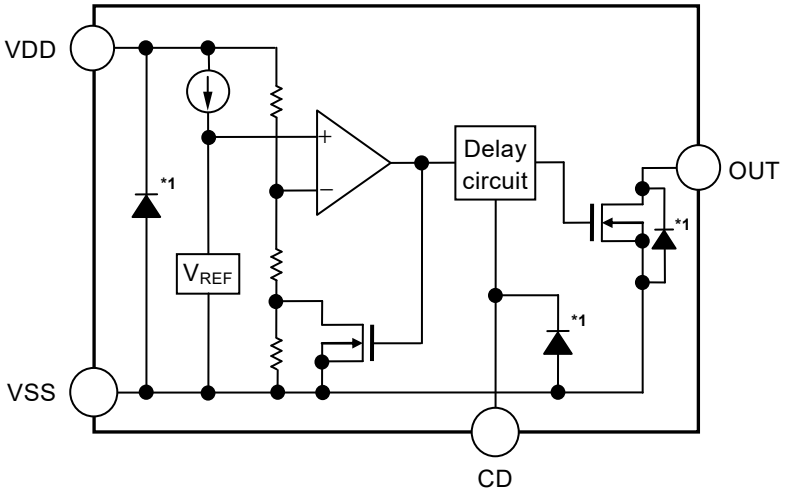
- For automotive use (engine, transmission, suspension, ABS, related-devices for EV / HEV / PHEV, etc.)

■ Packages

- SOT-23-5
- SC-82AB

■ Block Diagrams

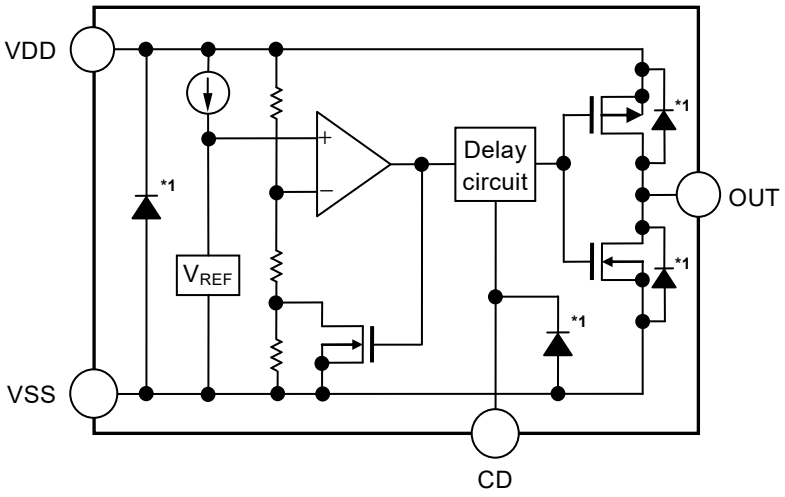
1. Nch open-drain output product



***1.** Parasitic diode

Figure 1

2. CMOS output product



***1.** Parasitic diode

Figure 2

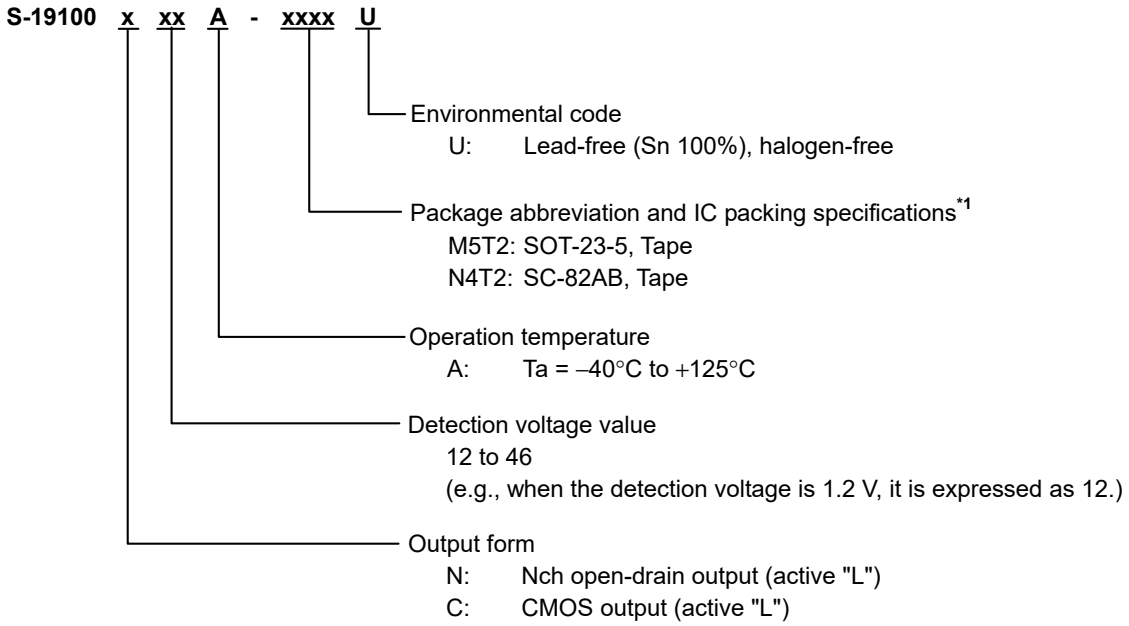
■ AEC-Q100 Qualified

This IC supports AEC-Q100 for operation temperature grade 1.
Contact our sales representatives for details of AEC-Q100 reliability specification.

■ Product Name Structure

Users can select the output form, the detection voltage value and the package type for the S-19100xxxA Series. Refer to "**1. Product name**" regarding the contents of product name, "**2. Packages**" regarding the package drawings and "**3. Product name list**" regarding details of product name.

1. Product name



***1.** Refer to the tape drawing.

2. Packages

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel
SOT-23-5	MP005-A-P-SD	MP005-A-C-SD	MP005-A-R-SD
SC-82AB	NP004-A-P-SD	NP004-A-C-SD NP004-A-C-S1	NP004-A-R-SD

3. Product name list

3. 1 Nch open-drain output product

Table 2

Detection Voltage	SOT-23-5	SC-82AB
1.2 V ± (2.5% + 12 mV)	S-19100N12A-M5T2U	S-19100N12A-N4T2U
1.3 V ± (2.5% + 12 mV)	S-19100N13A-M5T2U	S-19100N13A-N4T2U
1.4 V ± (2.5% + 12 mV)	S-19100N14A-M5T2U	S-19100N14A-N4T2U
1.5 V ± (2.5% + 12 mV)	S-19100N15A-M5T2U	S-19100N15A-N4T2U
1.6 V ± (2.5% + 12 mV)	S-19100N16A-M5T2U	S-19100N16A-N4T2U
1.7 V ± (2.5% + 12 mV)	S-19100N17A-M5T2U	S-19100N17A-N4T2U
1.8 V ± (2.5% + 12 mV)	S-19100N18A-M5T2U	S-19100N18A-N4T2U
1.9 V ± (2.5% + 12 mV)	S-19100N19A-M5T2U	S-19100N19A-N4T2U
2.0 V ± (2.5% + 12 mV)	S-19100N20A-M5T2U	S-19100N20A-N4T2U
2.1 V ± (2.5% + 12 mV)	S-19100N21A-M5T2U	S-19100N21A-N4T2U
2.2 V ± (2.5% + 12 mV)	S-19100N22A-M5T2U	S-19100N22A-N4T2U
2.3 V ± (2.5% + 12 mV)	S-19100N23A-M5T2U	S-19100N23A-N4T2U
2.4 V ± 3.0%	S-19100N24A-M5T2U	S-19100N24A-N4T2U
2.5 V ± 3.0%	S-19100N25A-M5T2U	S-19100N25A-N4T2U
2.6 V ± 3.0%	S-19100N26A-M5T2U	S-19100N26A-N4T2U
2.7 V ± 3.0%	S-19100N27A-M5T2U	S-19100N27A-N4T2U
2.8 V ± 3.0%	S-19100N28A-M5T2U	S-19100N28A-N4T2U
2.9 V ± 3.0%	S-19100N29A-M5T2U	S-19100N29A-N4T2U
3.0 V ± 3.0%	S-19100N30A-M5T2U	S-19100N30A-N4T2U
3.1 V ± 3.0%	S-19100N31A-M5T2U	S-19100N31A-N4T2U
3.2 V ± 3.0%	S-19100N32A-M5T2U	S-19100N32A-N4T2U
3.3 V ± 3.0%	S-19100N33A-M5T2U	S-19100N33A-N4T2U
3.4 V ± 3.0%	S-19100N34A-M5T2U	S-19100N34A-N4T2U
3.5 V ± 3.0%	S-19100N35A-M5T2U	S-19100N35A-N4T2U
3.6 V ± 3.0%	S-19100N36A-M5T2U	S-19100N36A-N4T2U
3.7 V ± 3.0%	S-19100N37A-M5T2U	S-19100N37A-N4T2U
3.8 V ± 3.0%	S-19100N38A-M5T2U	S-19100N38A-N4T2U
3.9 V ± 3.0%	S-19100N39A-M5T2U	S-19100N39A-N4T2U
4.0 V ± 3.0%	S-19100N40A-M5T2U	S-19100N40A-N4T2U
4.1 V ± 3.0%	S-19100N41A-M5T2U	S-19100N41A-N4T2U
4.2 V ± 3.0%	S-19100N42A-M5T2U	S-19100N42A-N4T2U
4.3 V ± 3.0%	S-19100N43A-M5T2U	S-19100N43A-N4T2U
4.4 V ± 3.0%	S-19100N44A-M5T2U	S-19100N44A-N4T2U
4.5 V ± 3.0%	S-19100N45A-M5T2U	S-19100N45A-N4T2U
4.6 V ± 3.0%	S-19100N46A-M5T2U	S-19100N46A-N4T2U

3. 2 CMOS output product

Table 3

Detection Voltage	SOT-23-5	SC-82AB
1.2 V ± (2.5% + 12 mV)	S-19100C12A-M5T2U	S-19100C12A-N4T2U
1.3 V ± (2.5% + 12 mV)	S-19100C13A-M5T2U	S-19100C13A-N4T2U
1.4 V ± (2.5% + 12 mV)	S-19100C14A-M5T2U	S-19100C14A-N4T2U
1.5 V ± (2.5% + 12 mV)	S-19100C15A-M5T2U	S-19100C15A-N4T2U
1.6 V ± (2.5% + 12 mV)	S-19100C16A-M5T2U	S-19100C16A-N4T2U
1.7 V ± (2.5% + 12 mV)	S-19100C17A-M5T2U	S-19100C17A-N4T2U
1.8 V ± (2.5% + 12 mV)	S-19100C18A-M5T2U	S-19100C18A-N4T2U
1.9 V ± (2.5% + 12 mV)	S-19100C19A-M5T2U	S-19100C19A-N4T2U
2.0 V ± (2.5% + 12 mV)	S-19100C20A-M5T2U	S-19100C20A-N4T2U
2.1 V ± (2.5% + 12 mV)	S-19100C21A-M5T2U	S-19100C21A-N4T2U
2.2 V ± (2.5% + 12 mV)	S-19100C22A-M5T2U	S-19100C22A-N4T2U
2.3 V ± (2.5% + 12 mV)	S-19100C23A-M5T2U	S-19100C23A-N4T2U
2.4 V ± 3.0%	S-19100C24A-M5T2U	S-19100C24A-N4T2U
2.5 V ± 3.0%	S-19100C25A-M5T2U	S-19100C25A-N4T2U
2.6 V ± 3.0%	S-19100C26A-M5T2U	S-19100C26A-N4T2U
2.7 V ± 3.0%	S-19100C27A-M5T2U	S-19100C27A-N4T2U
2.8 V ± 3.0%	S-19100C28A-M5T2U	S-19100C28A-N4T2U
2.9 V ± 3.0%	S-19100C29A-M5T2U	S-19100C29A-N4T2U
3.0 V ± 3.0%	S-19100C30A-M5T2U	S-19100C30A-N4T2U
3.1 V ± 3.0%	S-19100C31A-M5T2U	S-19100C31A-N4T2U
3.2 V ± 3.0%	S-19100C32A-M5T2U	S-19100C32A-N4T2U
3.3 V ± 3.0%	S-19100C33A-M5T2U	S-19100C33A-N4T2U
3.4 V ± 3.0%	S-19100C34A-M5T2U	S-19100C34A-N4T2U
3.5 V ± 3.0%	S-19100C35A-M5T2U	S-19100C35A-N4T2U
3.6 V ± 3.0%	S-19100C36A-M5T2U	S-19100C36A-N4T2U
3.7 V ± 3.0%	S-19100C37A-M5T2U	S-19100C37A-N4T2U
3.8 V ± 3.0%	S-19100C38A-M5T2U	S-19100C38A-N4T2U
3.9 V ± 3.0%	S-19100C39A-M5T2U	S-19100C39A-N4T2U
4.0 V ± 3.0%	S-19100C40A-M5T2U	S-19100C40A-N4T2U
4.1 V ± 3.0%	S-19100C41A-M5T2U	S-19100C41A-N4T2U
4.2 V ± 3.0%	S-19100C42A-M5T2U	S-19100C42A-N4T2U
4.3 V ± 3.0%	S-19100C43A-M5T2U	S-19100C43A-N4T2U
4.4 V ± 3.0%	S-19100C44A-M5T2U	S-19100C44A-N4T2U
4.5 V ± 3.0%	S-19100C45A-M5T2U	S-19100C45A-N4T2U
4.6 V ± 3.0%	S-19100C46A-M5T2U	S-19100C46A-N4T2U

■ Pin Configurations

1. SOT-23-5

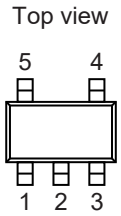


Figure 3

Table 4

Pin No.	Symbol	Description
1	OUT	Voltage detection output pin
2	VDD	Input voltage pin
3	VSS	GND pin
4	NC*1	No connection
5	CD	Connection pin for delay capacitor

***1.** The NC pin is electrically open.
The NC pin can be connected to the VDD pin or the VSS pin.

2. SC-82AB

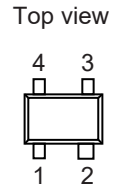


Figure 4

Table 5

Pin No.	Symbol	Description
1	VSS	GND pin
2	VDD	Input voltage pin
3	CD	Connection pin for delay capacitor
4	OUT	Voltage detection output pin

■ Absolute Maximum Ratings

Table 6

(Ta = –40°C to +125°C unless otherwise specified)

Item		Symbol	Absolute Maximum Rating	Unit
Power supply voltage		V_{DD} – V_{SS}	12	V
CD pin input voltage		V_{CD}	V_{SS} – 0.3 to V_{DD} + 0.3	V
Output voltage	Nch open-drain output product	V_{OUT}	V_{SS} – 0.3 to 12.0	V
	CMOS output product		V_{SS} – 0.3 to V_{DD} + 0.3	V
Output current		I_{OUT}	50	mA
Operation ambient temperature		T_{opr}	–40 to +125	°C
Storage temperature		T_{stg}	–40 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 7

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	SOT-23-5	Board A	–	192	–	°C/W
			Board B	–	160	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W
		SC-82AB	Board A	–	236	–	°C/W
			Board B	–	204	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ **Power Dissipation**" and "**Test Board**" for details.

■ Electrical Characteristics

1. Nch open-drain output product

Table 8

(Ta = –40°C to +125°C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Detection voltage*1	$-V_{DET}$	1.2 V ≤ $-V_{DET}$ < 2.4 V		$-V_{DET(S)} \times 0.975 - 0.012$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.025 + 0.012$	V	1
		2.4 V ≤ $-V_{DET}$ ≤ 4.6 V		$-V_{DET(S)} \times 0.97$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.03$	V	1
Hysteresis width	V_{HYS}	–		$-V_{DET} \times 0.03$	$-V_{DET} \times 0.05$	$-V_{DET} \times 0.07$	V	1
Current consumption	I_{SS}	V_{DD} = $+V_{DET}$ + 0.6 V	1.2 V ≤ $-V_{DET}$ < 2.3 V	–	0.27	1.80	µA	2
			2.3 V ≤ $-V_{DET}$ < 3.6 V	–	0.42	2.20	µA	2
			3.6 V ≤ $-V_{DET}$ ≤ 4.6 V	–	0.39	2.20	µA	2
Operation voltage	V_{DD}	–		0.8	–	10.0	V	1
Output current	I_{OUT}	Output transistor Nch V_{DS}*2 = 0.5 V	V_{DD} = 0.7 V S-19100N12 to 14	0.14	0.40	–	mA	3
			V_{DD} = 1.2 V S-19100N15 to 46	0.68	1.33	–	mA	3
			V_{DD} = 2.4 V S-19100N27 to 46	1.12	2.39	–	mA	3
Leakage current	I_{LEAK}	Output transistor Nch V_{DD} = 10.0 V, V_{OUT} = 10.0 V		–	–	2.40	µA	3
Delay time	t_D	C_D = 4.7 nF		10.0	26.0	57.0	ms	4

***1.** $-V_{DET}$: Actual detection voltage value, $-V_{DET(S)}$: Set detection voltage value (The center value of the detection voltage range in **Table 2**.)

***2.** V_{DS}: Drain-to-source voltage of the output transistor

2. CMOS output product

Table 9

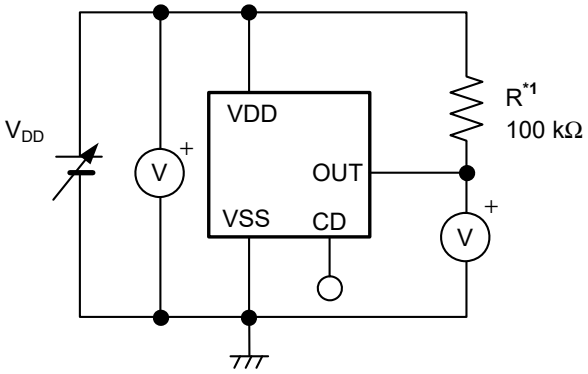
(Ta = –40°C to +125°C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Detection voltage*1	$-V_{DET}$	1.2 V ≤ $-V_{DET}$ < 2.4 V		$-V_{DET(S)} \times 0.975 - 0.012$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.025 + 0.012$	V	1
		2.4 V ≤ $-V_{DET}$ ≤ 4.6 V		$-V_{DET(S)} \times 0.97$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.03$	V	1
Hysteresis width	V_{HYS}	–		$-V_{DET} \times 0.03$	$-V_{DET} \times 0.05$	$-V_{DET} \times 0.07$	V	1
Current consumption	I_{SS}	V_{DD} = $+V_{DET}$ + 0.6 V	1.2 V ≤ $-V_{DET}$ < 2.3 V	–	0.27	1.80	µA	2
			2.3 V ≤ $-V_{DET}$ < 3.6 V	–	0.42	2.20	µA	2
			3.6 V ≤ $-V_{DET}$ ≤ 4.6 V	–	0.39	2.20	µA	2
Operation voltage	V_{DD}	–		0.6	–	10.0	V	1
Output current	I_{OUT}	Output transistor Nch V_{DS}*2 = 0.5 V	V_{DD} = 0.7 V S-19100C12 to 14	0.14	0.40	–	mA	3
			V_{DD} = 1.2 V S-19100C15 to 46	0.68	1.33	–	mA	3
			V_{DD} = 2.4 V S-19100C27 to 46	1.12	2.39	–	mA	3
		Output transistor Pch V_{DS}*2 = 0.5 V	V_{DD} = 4.8 V S-19100C12 to 39	1.42	2.60	–	mA	5
			V_{DD} = 6.0 V S-19100C40 to 46	1.58	2.86	–	mA	5
Delay time	t_D	C_D = 4.7 nF		10.0	26.0	57.0	ms	4

***1.** $-V_{DET}$: Actual detection voltage value, $-V_{DET(S)}$: Set detection voltage value (The center value of the detection voltage range in **Table 3**.)

***2.** V_{DS}: Drain-to-source voltage of the output transistor

■ Test Circuits



***1.** R is unnecessary for CMOS output product.

Figure 5 Test Circuit 1

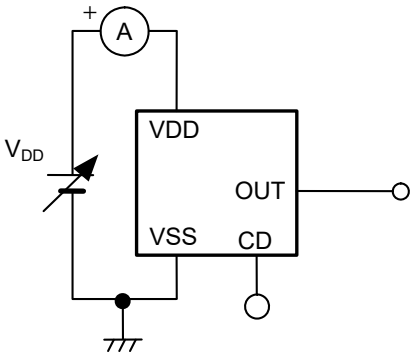


Figure 6 Test Circuit 2

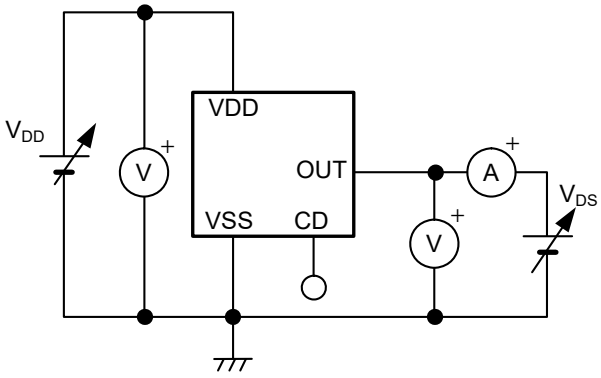
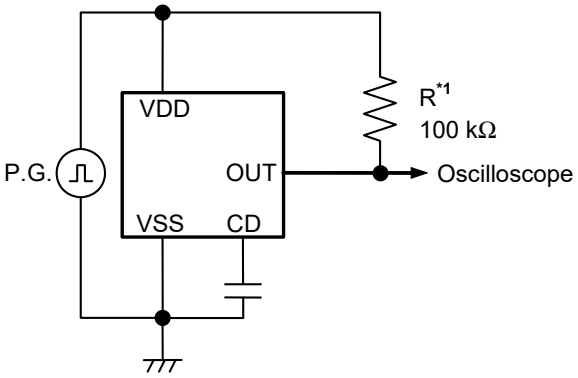


Figure 7 Test Circuit 3



***1.** R is unnecessary for CMOS output product.

Figure 8 Test Circuit 4

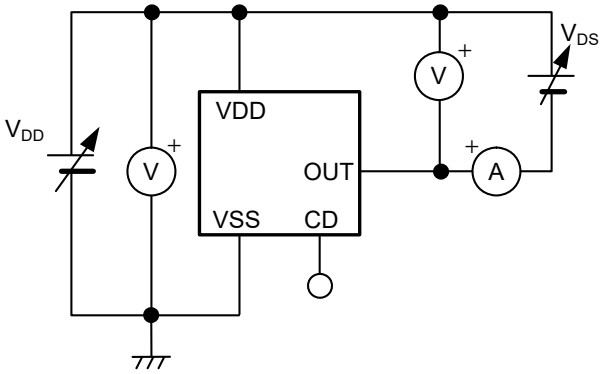


Figure 9 Test Circuit 5

■ Timing Charts

1. Nch open-drain output product

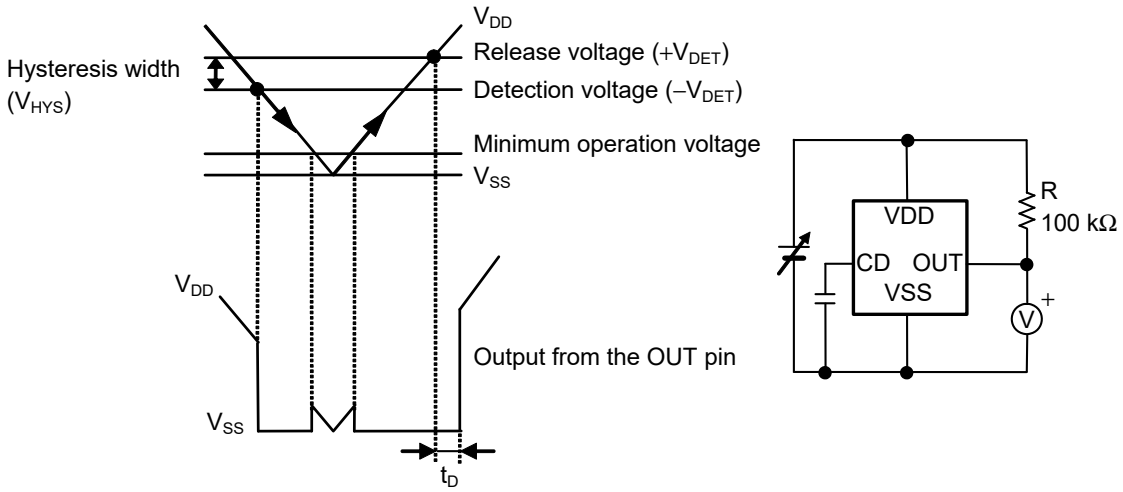
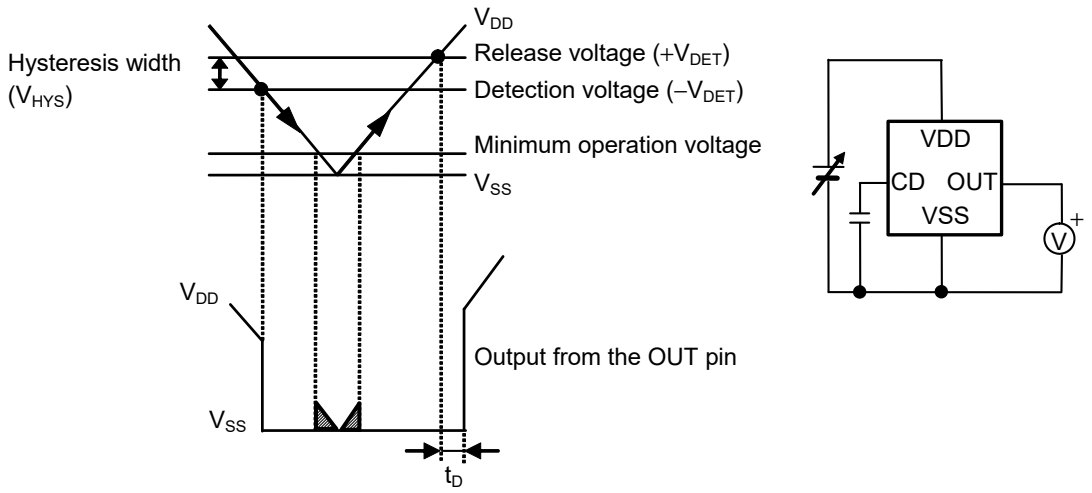


Figure 10

2. CMOS output product



Remark When V_{DD} is the minimum operation voltage or less, the output voltage from the OUT pin is indefinite in the shaded area.

Figure 11

■ Operation

1. Basic operation: CMOS output (active "L") product

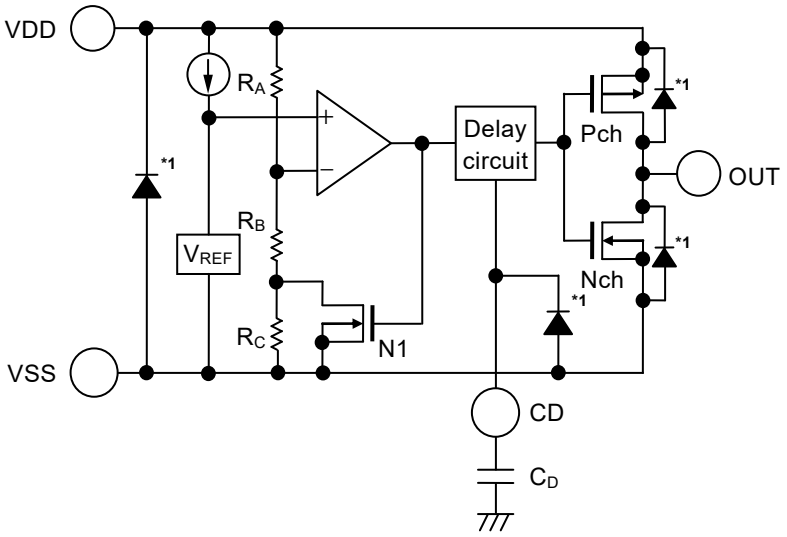
(1) When the power supply voltage (V_{DD}) is the release voltage ($+V_{DET}$) or higher, the Nch transistor is turned off and the Pch transistor is turned on to output V_{DD} ("H"). Since the Nch transistor N1 in **Figure 12** is turned off, the input voltage to the comparator is $\frac{(R_B + R_C) \bullet V_{DD}}{R_A + R_B + R_C}$.

(2) Even if V_{DD} decreases to $+V_{DET}$ or lower, V_{DD} is output when V_{DD} is higher than the detection voltage ($-V_{DET}$). When V_{DD} decreases to $-V_{DET}$ (point A in **Figure 13**) or lower, the Nch transistor is turned on and the Pch transistor is turned off, and then V_{SS} ("L") is output. At this time, the Nch transistor N1 in **Figure 12** is turned on, and the input voltage to the comparator is $\frac{R_B \bullet V_{DD}}{R_A + R_B}$.

(3) The output is unstable if V_{DD} further decreases to the IC's minimum operation voltage or lower, and the output is V_{DD} when the output is pulled up.

(4) V_{SS} is output when V_{DD} increases to the minimum operation voltage or higher. Even if V_{DD} exceeds $-V_{DET}$, the output is V_{SS} when V_{DD} is lower than $+V_{DET}$.

(5) When V_{DD} increases to $+V_{DET}$ (point B in **Figure 13**) or higher, the Nch transistor is turned off and the Pch transistor is turned on, and then V_{DD} is output. At this time, V_{DD} is output from the OUT pin after the elapse of the delay time (t_D).



***1.** Parasitic diode

Figure 12 Operation 1

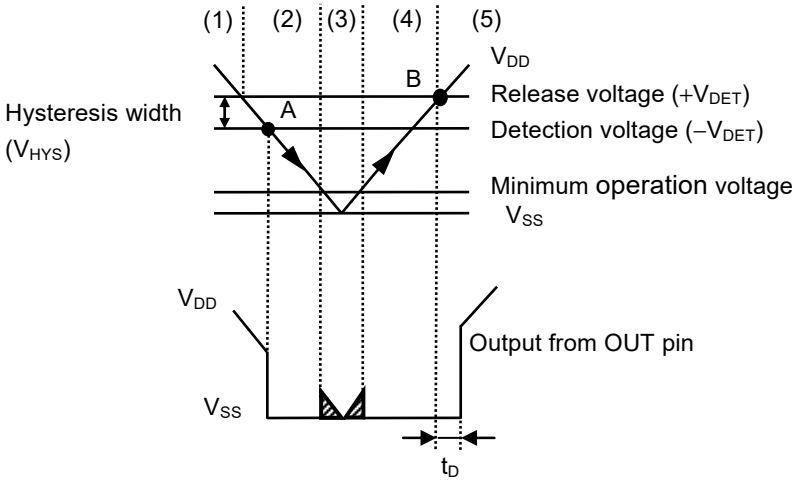


Figure 13 Operation 2

2. Delay circuit

The delay circuit delays the output signal to the OUT pin from the time at which the power supply voltage (V_{DD}) exceeds the release voltage ($+V_{DET}$) when the power supply voltage (V_{DD}) is turned on. The output signal is not delayed when V_{DD} decreases to the detection voltage ($-V_{DET}$) or less (refer to "**Figure 13 Operation 2**").
The delay time (t_D) is determined by the time constant of the built-in constant current (approx. 100 nA) and the attached delay capacitor (C_D), or the delay time when the CD pin is open (t_{D0}), and calculated from the following equation. When the C_D value is sufficiently large, the t_{D0} value can be ignored.

t_D [ms] = Delay coefficient $\times$ C_D [nF] + t_{D0} [ms]

Table 10 Delay Coefficient

Operation Temperature	Delay Coefficient		
	Min.	Typ.	Max.
Ta = +125°C	1.96	3.50	5.15
Ta = +105°C	2.58	3.70	5.40
Ta = +25°C	4.70	5.47	6.24
Ta = −40°C	5.64	8.40	12.01

Table 11 Delay Time

Operation Temperature	Delay Time when CD pin is Open (t_{D0})		
	Min.	Typ.	Max.
Ta = −40°C to +125°C	0.01 ms	0.10 ms	0.80 ms

Caution 1. When the CD pin is open, a double pulse shown in Figure 14 may appear at release. To avoid the double pulse, attach 100 pF or more capacitor to the CD pin. Do not apply voltage to the CD pin from the exterior.

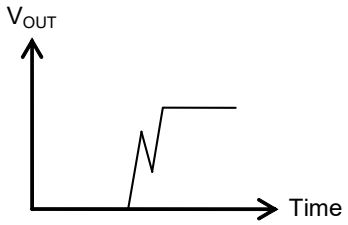
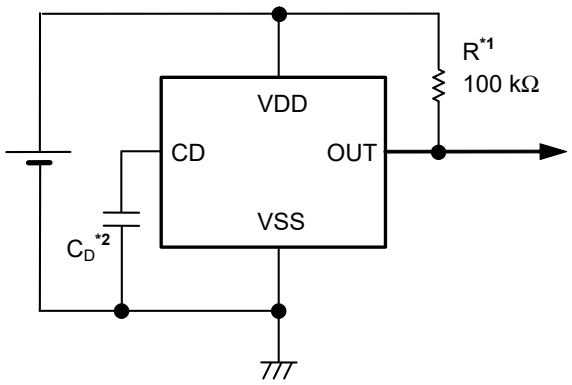


Figure 14

2. **Mounted board layout should be made in such a way that no current flows into or flows from the CD pin since the impedance of the CD pin is high, otherwise correct delay time cannot be provided.**
3. **There is no limit for the capacitance of C_D as long as the leakage current of the capacitor can be ignored against the built-in constant current value. Leakage current causes deviation in delay time. When the leakage current is larger than the built-in constant current, no release takes place.**

■ Standard Circuit



***1.** R is unnecessary for CMOS output products.
***2.** The delay capacitor (C_D) should be connected directly to the CD pin and the VSS pin.

Figure 15

Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

■ Explanation of Terms

1. Detection voltage ($-V_{DET}$)

The detection voltage is a voltage at which the output in **Figure 18** turns to "L". The detection voltage varies slightly among products of the same specification. The variation of detection voltage between the specified minimum ($-V_{DET}$ min.) and the maximum ($-V_{DET}$ max.) is called the detection voltage range (refer to **Figure 16**).

Example: In the S-19100C20A, the detection voltage is either one in the range of $1.938\ V \le -V_{DET} \le 2.062\ V$. This means, at the operation temperature –40°C to +125°C, some S-19100C20A have $-V_{DET} = 1.938$ V and some have $-V_{DET} = 2.062$ V.

2. Release voltage ($+V_{DET}$)

The release voltage is a voltage at which the output in **Figure 18** turns to "H". The release voltage varies slightly among products of the same specification. The variation of release voltages between the specified minimum ($+V_{DET}$ min.) and the maximum ($+V_{DET}$ max.) is called the release voltage range (refer to **Figure 17**). The value is calculated from the actual detection voltage ($-V_{DET}$) of a product and is in the range of $-V_{DET} \times 1.03 \le +V_{DET} \le -V_{DET} \times 1.07$.

Example: In the S-19100C20A, the release voltage is either one in the range of $1.997\ V \le +V_{DET} \le 2.206\ V$. This means, at the operation temperature –40°C to +125°C, some S-19100C20A have $+V_{DET} = 1.997$ V and some have $+V_{DET} = 2.206$ V.

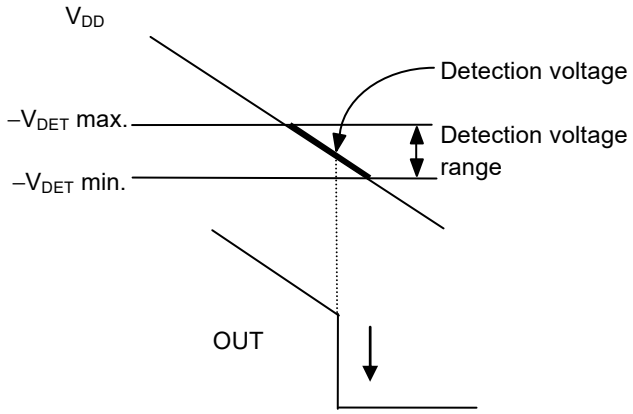


Figure 16 Detection Voltage

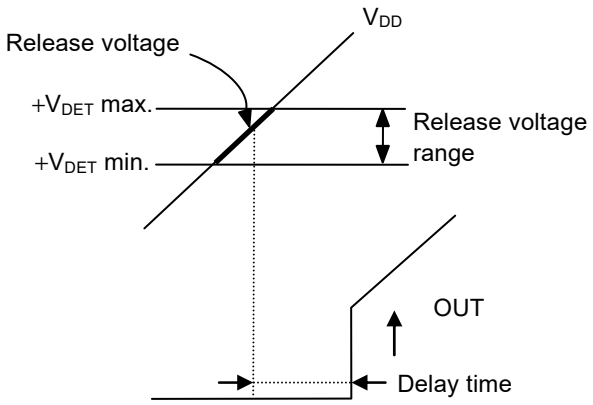
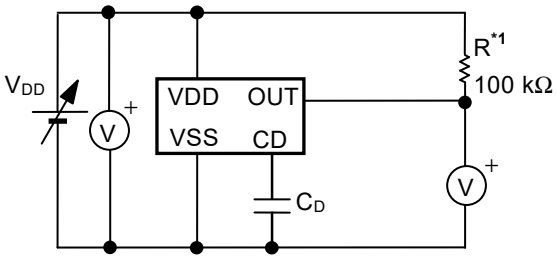


Figure 17 Release Voltage



***1.** R is unnecessary for CMOS output product.

Figure 18 Test Circuit of Detection Voltage and Release Voltage

3. Hysteresis width (V_{HYS})

The hysteresis width is the voltage difference between the detection voltage and the release voltage (the voltage at point B − the voltage at point A = V_{HYS} in "**Figure 13 Operation 2**"). Setting the hysteresis width between the detection voltage and the release voltage to prevent malfunction caused by noise on the input voltage.

4. Delay time (t_D)

The delay time in the S-19100xxxA Series is a period from the input voltage to the VDD pin exceeding the release voltage ($+V_{DET}$) until the output from the OUT pin inverts. The delay time changes according to the delay capacitor (C_D).

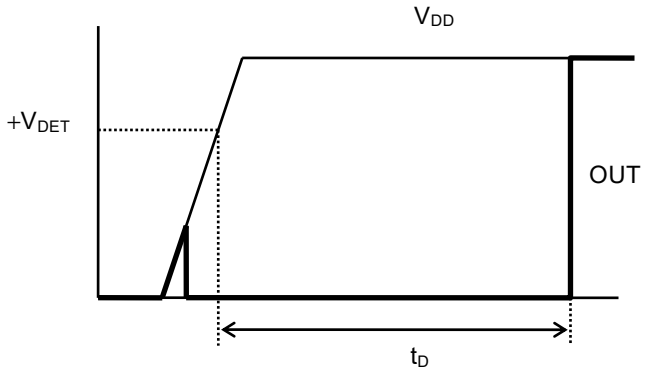


Figure 19 Delay Time

5. Feed-through current

Feed-through current is a current that flows instantaneously at the time of detection and release of a voltage detector. The feed-through current is large in CMOS output product, small in Nch open-drain output product.

6. Oscillation

In applications where a resistor is connected to the voltage detector input (**Figure 20**), taking a CMOS output (active "L") product for example, the feed-through current which is generated when the output goes from "L" to "H" (release) causes a voltage drop equal to [feed-through current] × [input resistance] across the resistor. When the input voltage drops below the detection voltage ($-V_{DET}$) as a result, the output voltage goes to low level. In this state, the feed-through current stops and its resultant voltage drop disappears, and the output goes from "L" to "H". The feed-through current is then generated again, a voltage drop appears, and repeating the process finally induces oscillation.

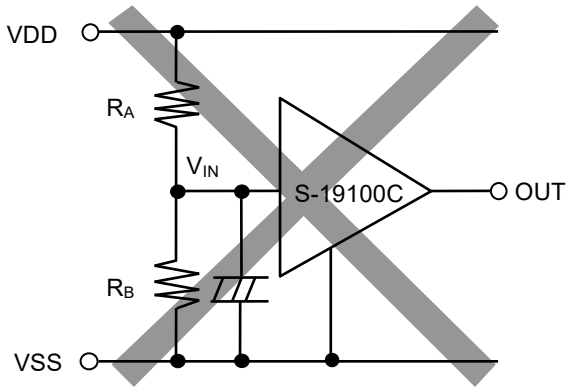


Figure 20 Example for Bad Implementation Due to Detection Voltage Change

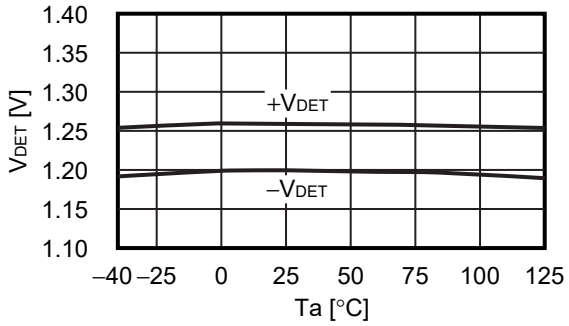
■ Precautions

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- In CMOS output product, the feed-through current flows at the detection and the release. If the input impedance is high, oscillation may occur due to the voltage drop by the feed-through current during releasing.
- In CMOS output product, oscillation may occur when a pull-down resistor is used, and falling speed of the power supply voltage (V_{DD}) is slow near the detection voltage.
- When designing for mass production using an application circuit described herein, the product deviation and temperature characteristics of the external parts should be taken into consideration. ABLIC Inc. shall not bear any responsibility for patent infringements related to products using the circuits described herein.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

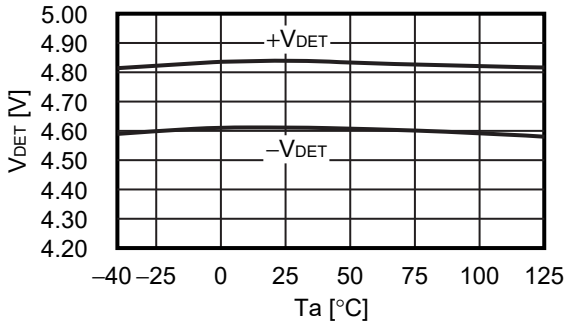
■ Characteristics (Typical Data)

1. Detection voltage (V_{DET}) vs. Temperature (Ta)

S-19100N12

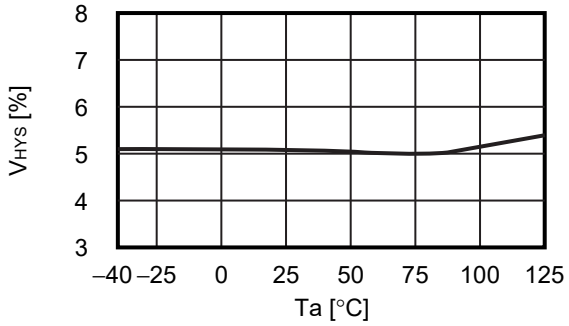


S-19100N46

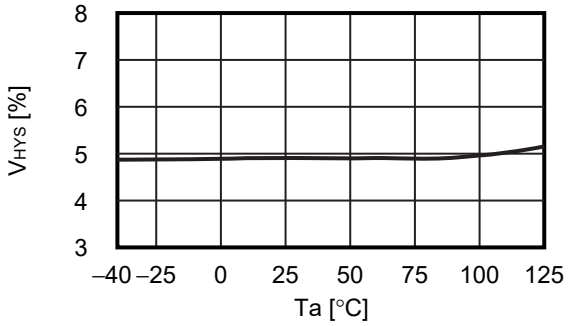


2. Hysteresis width (V_{HYS}) vs. Temperature (Ta)

S-19100N12

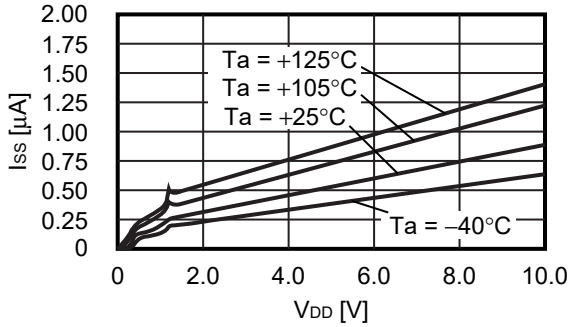


S-19100N46

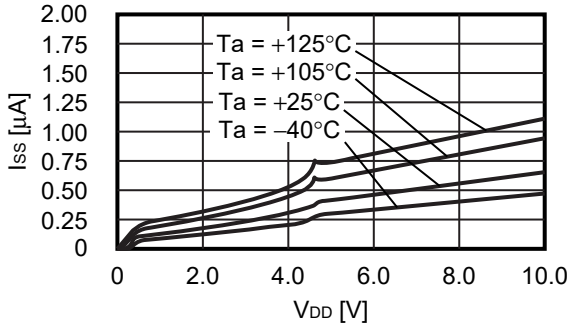


3. Current consumption (I_{SS}) vs. Input voltage (V_{DD})

S-19100C12

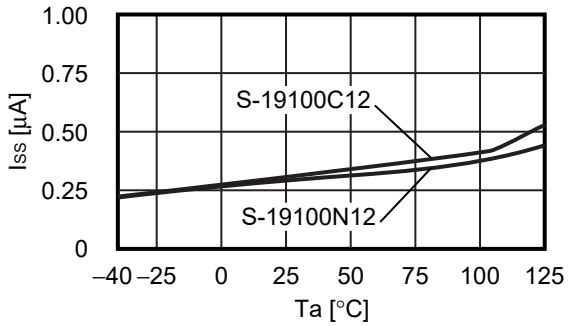


S-19100C46

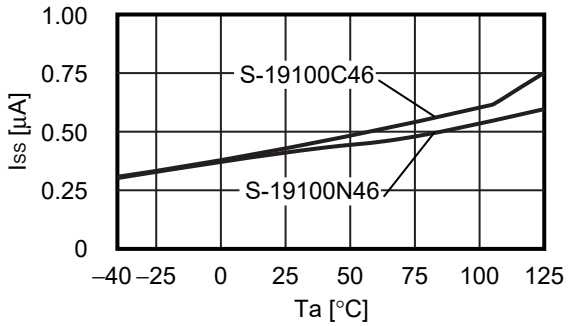


4. Current consumption (I_{SS}) vs. Temperature (Ta)

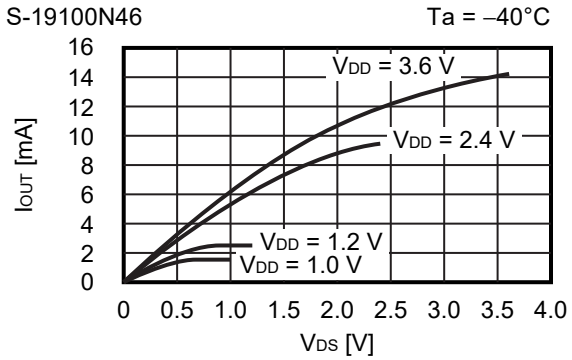
S-19100N12/19100C12 $V_{DD} = +V_{DET} + 0.6$ V

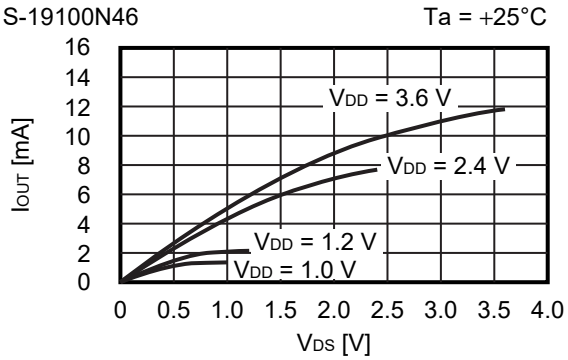


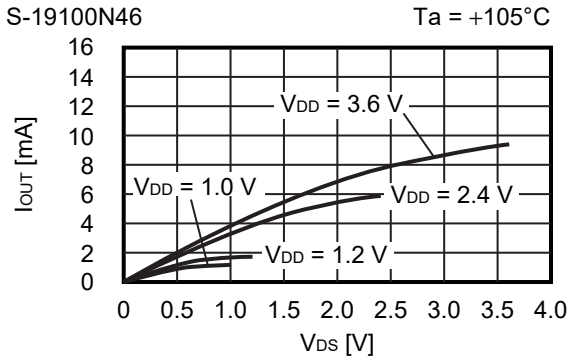
S-19100N46/19100C46 $V_{DD} = +V_{DET} + 0.6$ V

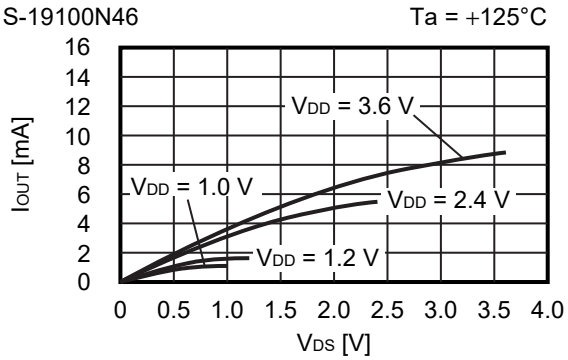


5. Nch transistor output current (I_{OUT}) vs. V_{DS}

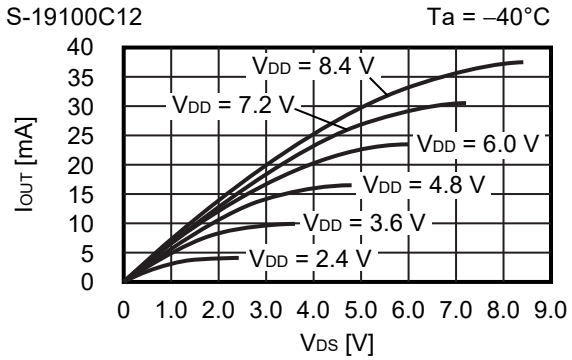


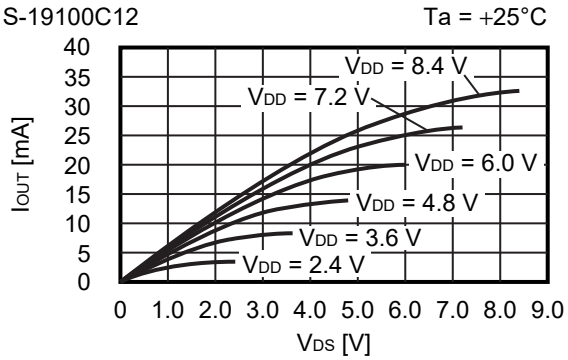


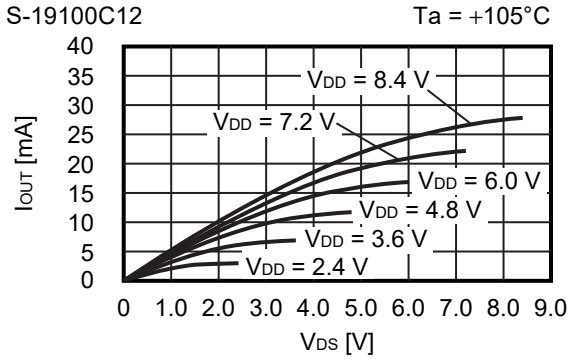


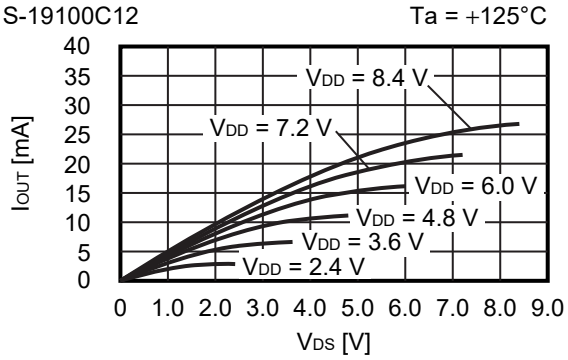


6. Pch transistor output current (I_{OUT}) vs. V_{DS}





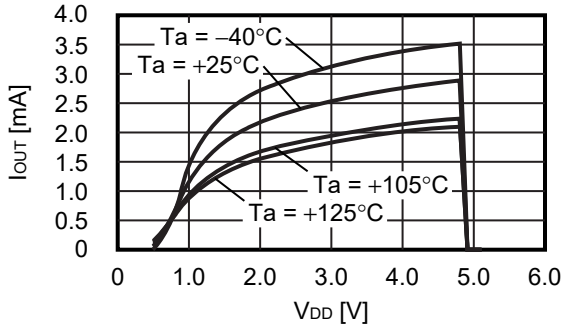




Remark V_{DS}: Drain-to-source voltage of the output transistor

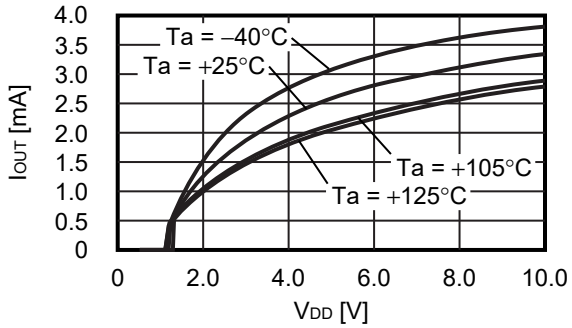
7. Nch transistor output current (I_{OUT}) vs. Input voltage (V_{DD})

S-19100N46 V_{DS} = 0.5 V



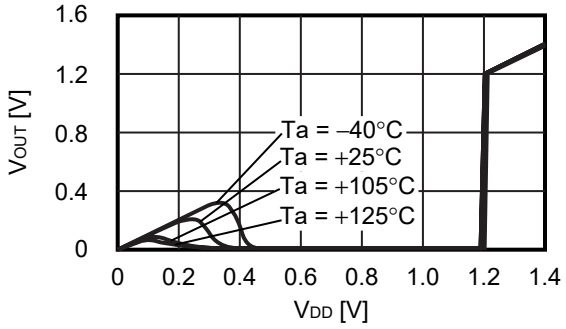
8. Pch transistor output current (I_{OUT}) vs. Input voltage (V_{DD})

S-19100C12 V_{DS} = 0.5 V

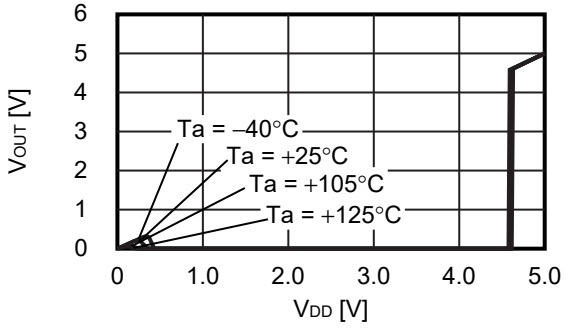


9. Minimum operation voltage (V_{OUT}) vs. Input voltage (V_{DD})

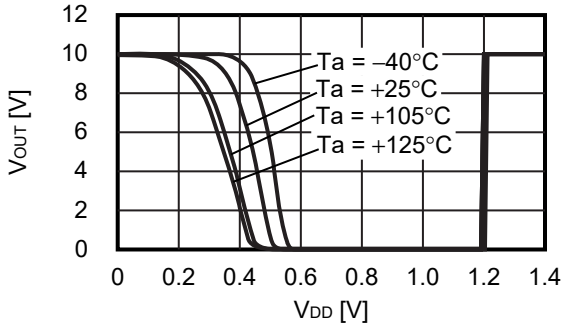
S-19100N12 Pull-up to V_{DD}
Pull-up resistance: 100 kΩ



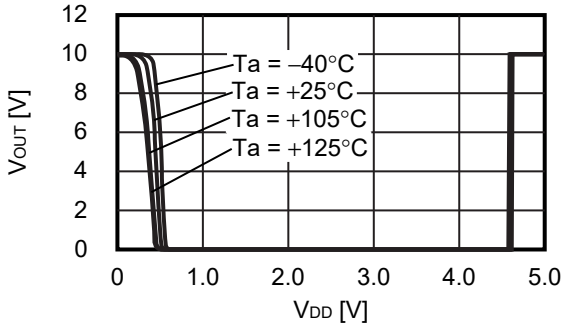
S-19100N46 Pull-up to V_{DD}
Pull-up resistance: 100 kΩ



S-19100N12 Pull-up to 10 V
Pull-up resistance: 100 kΩ



S-19100N46 Pull-up to 10 V
Pull-up resistance: 100 kΩ

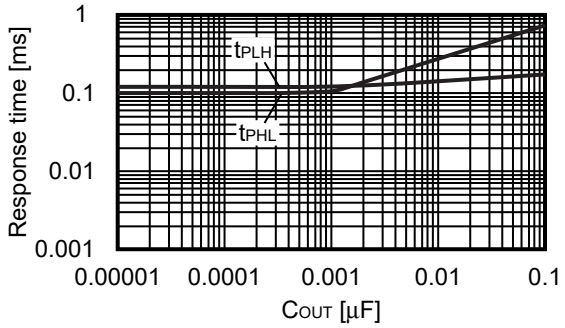


Remark V_{DS}: Drain-to-source voltage of the output transistor

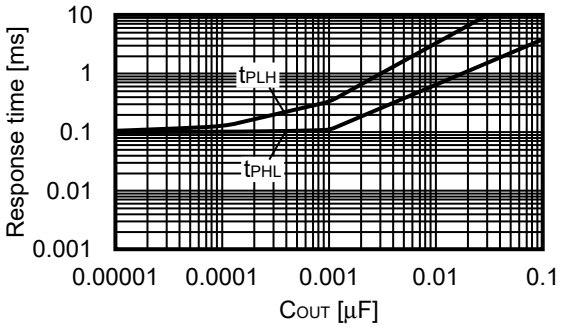
10. Dynamic response characteristics vs. Output pin capacitance (C_{OUT}) (CD pin; open)

10. 1 $-V_{DET}$ = 1.2 V

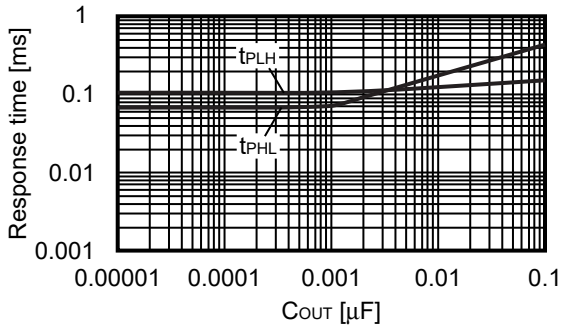
S-19100C12 Ta = −40°C



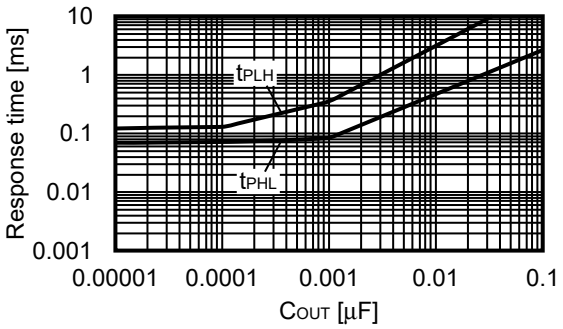
S-19100N12 Ta = −40°C



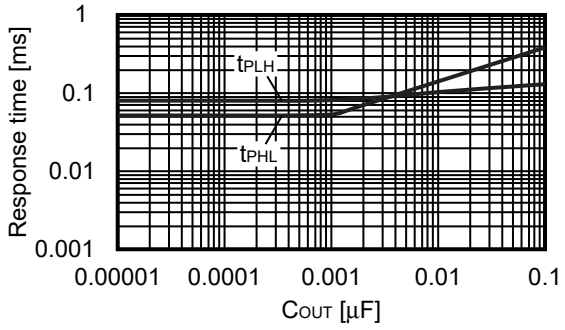
S-19100C12 Ta = +25°C



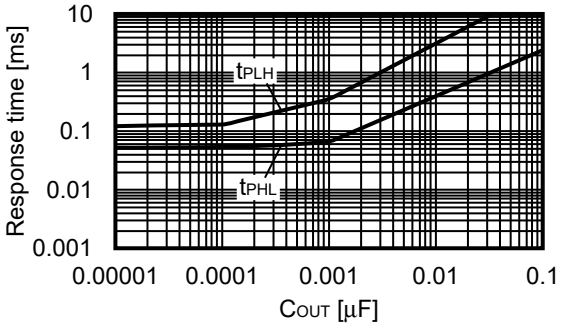
S-19100N12 Ta = +25°C



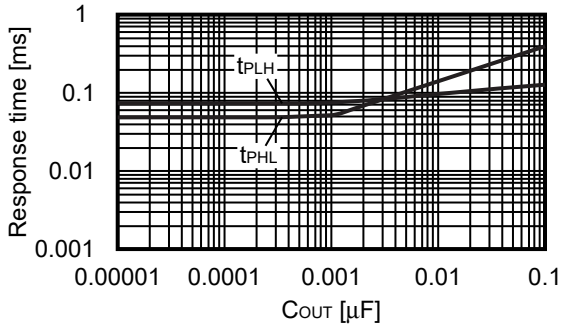
S-19100C12 Ta = +105°C



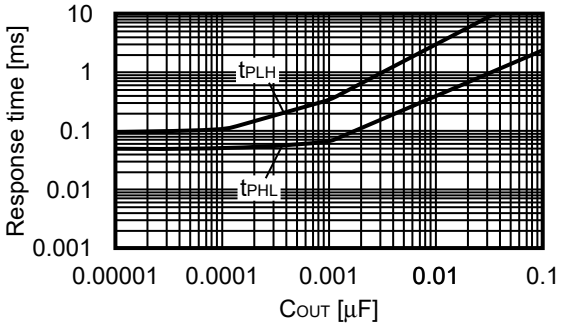
S-19100N12 Ta = +105°C



S-19100C12 Ta = +125°C

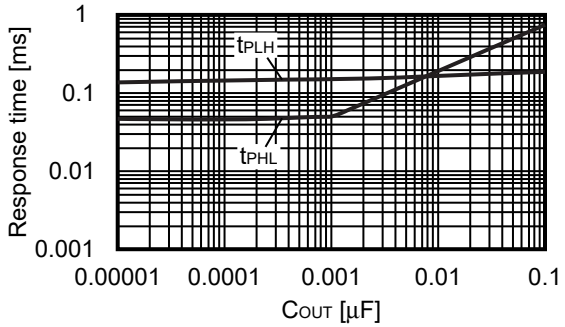


S-19100N12 Ta = +125°C

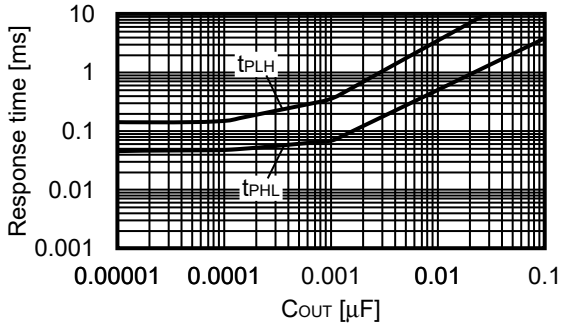


10. 2 $-V_{DET}$ = 4.6 V

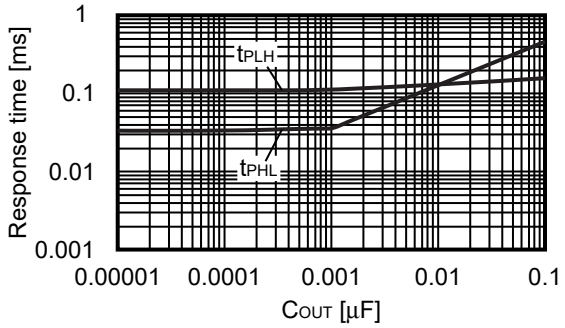
S-19100C46 Ta = –40°C



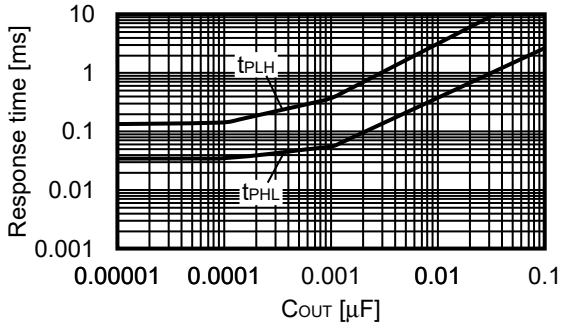
S-19100N46 Ta = –40°C



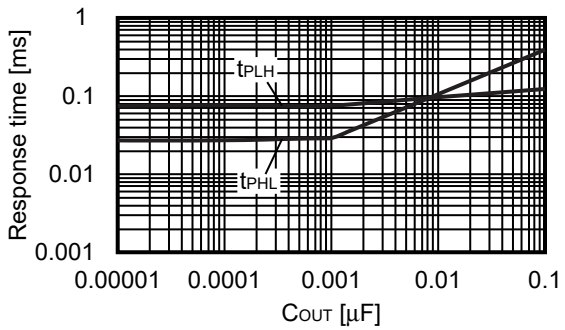
S-19100C46 Ta = +25°C



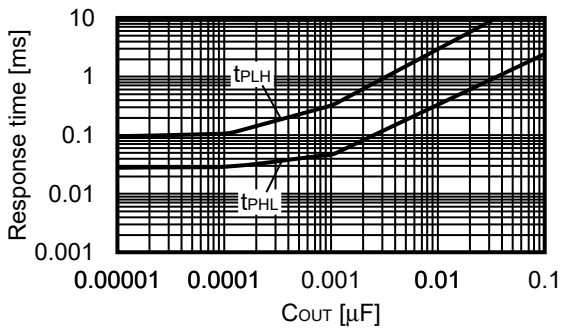
S-19100N46 Ta = +25°C



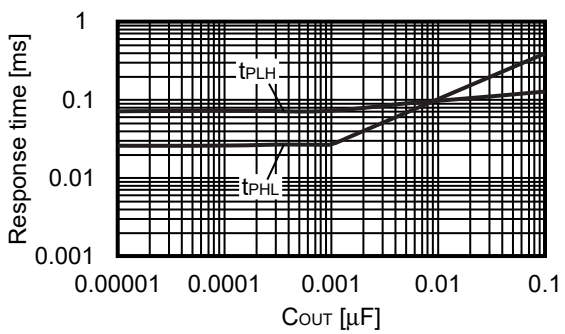
S-19100C46 Ta = +105°C



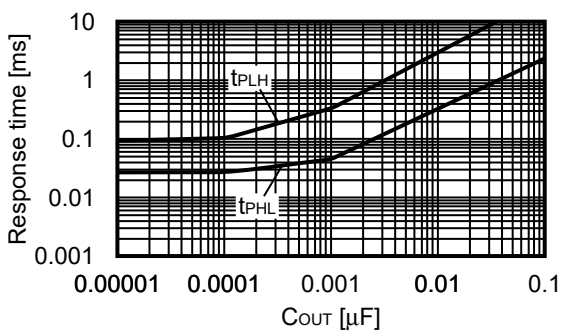
S-19100N46 Ta = +105°C

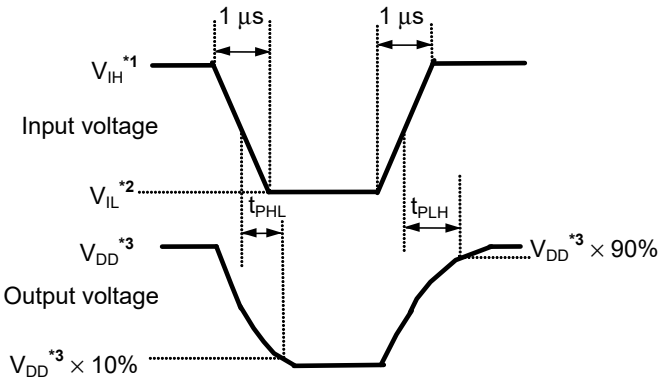


S-19100C46 Ta = +125°C



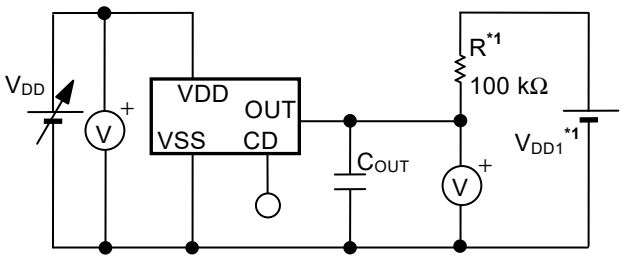
S-19100N46 Ta = +125°C





***1.** V_{IH} = 10 V
***2.** V_{IL} = 0.8 V
***3**. CMOS output product: V_{DD}
Nch open-drain product: V_{DD1}

Figure 21 Test Condition of Response Time



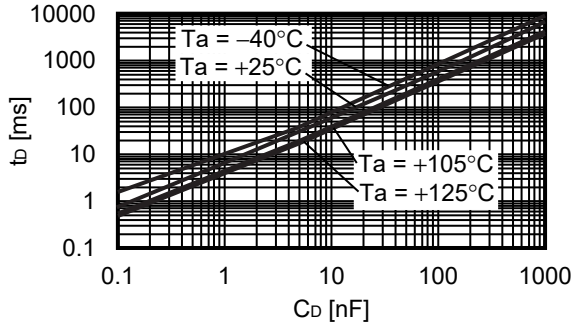
***1.** R and V_{DD1} are unnecessary for CMOS output product.

Figure 22 Test Circuit of Response Time

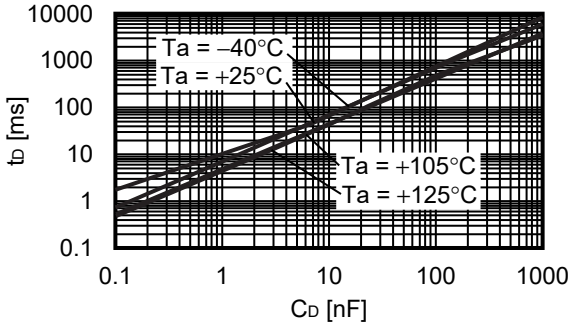
Caution 1. The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.
2. When the CD pin is open, a double pulse may appear at release. To avoid the double pulse, attach 100 pF or more capacitor to the CD pin. Response time when detecting (t_{PHL}) is not affected by CD pin capacitance. Besides, response time when releasing (t_{PLH}) can be set the delay time by attaching CD pin. Refer to "11. Delay time (t_D) vs. CD pin capacitance (C_D) (without output pin capacitance) for details.

11. Delay time (t_D) vs. CD pin capacitance (C_D) (without output pin capacitance)

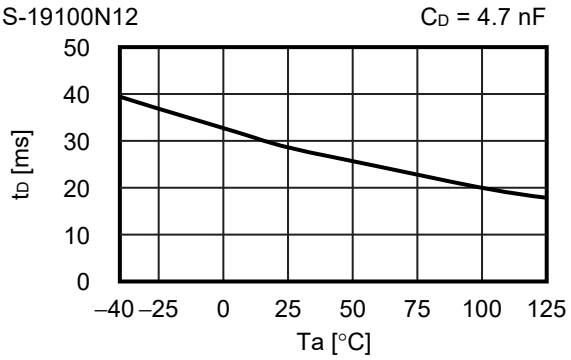
S-19100C12

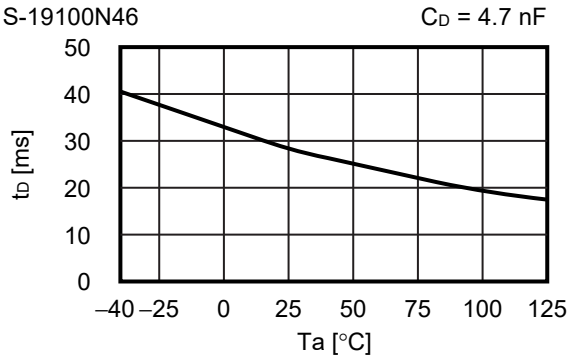


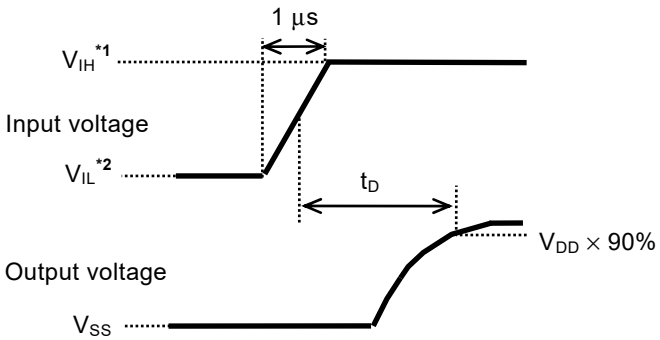
S-19100C46



12. Delay time (t_D) vs. Temperature (Ta)

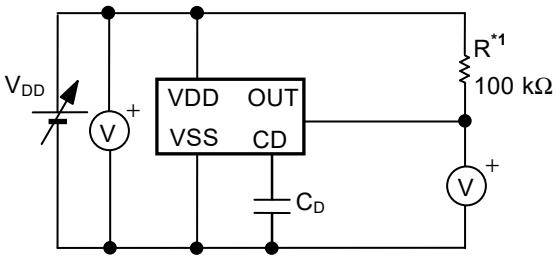






*1. V_{IH} = 10 V
*2. V_{IL} = 0.8 V

Figure 23 Test Condition of Delay Time



*1. R is unnecessary for CMOS output product.

Figure 24 Test Circuit of Delay Time

**Caution The above connection diagram and constant will not guarantee successful operation.
Perform thorough evaluation using the actual application to set the constant.**

■ Application Circuit Examples

1. Microcomputer reset circuits

In microcomputers, when the power supply voltage is lower than the minimum operation voltage, an unspecified operation may be performed or the contents of the memory register may be lost. When power supply voltage returns to the normal level, the microcomputer needs to be initialized. Otherwise, the microcomputer may malfunction after that. Reset circuits to protect microcomputer in the event of current being momentarily switched off or lowered.
Using the S-19100xxxA Series which has the low minimum operation voltage, a high-accuracy detection voltage and hysteresis, reset circuits can be easily constructed as seen in **Figure 25** and **Figure 26**.

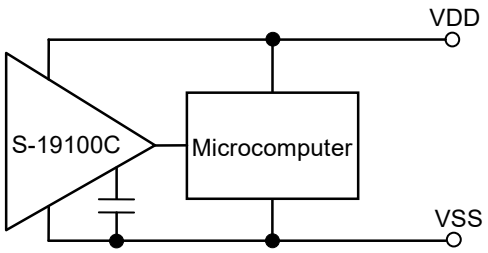


Figure 25 Example of Reset Circuit (CMOS Output Product)

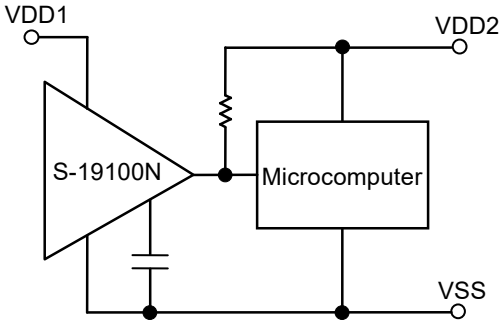
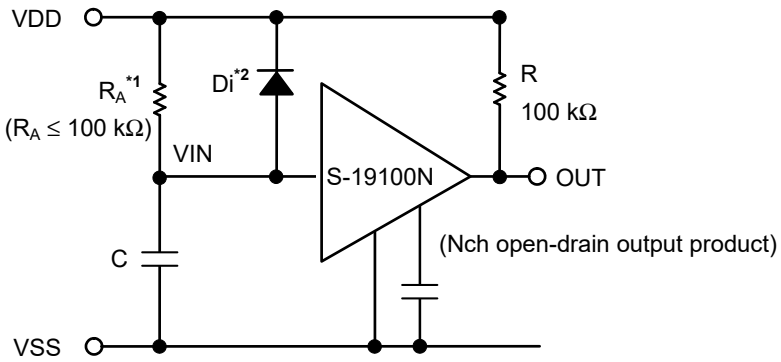


Figure 26 Example of Reset Circuit (Nch Open-drain Output Product)

Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

2. Power-on reset circuit (Nch open-drain output product only)

A power-on reset circuit can be constructed using the S-19100NxxA Series.



***1.** R_A should be 100 kΩ or less to prevent oscillation.

***2.** Diode (Di) instantaneously discharges the charge stored in the capacitor (C) at the power falling. Di can be removed when the delay of the falling time is not important.

Figure 27

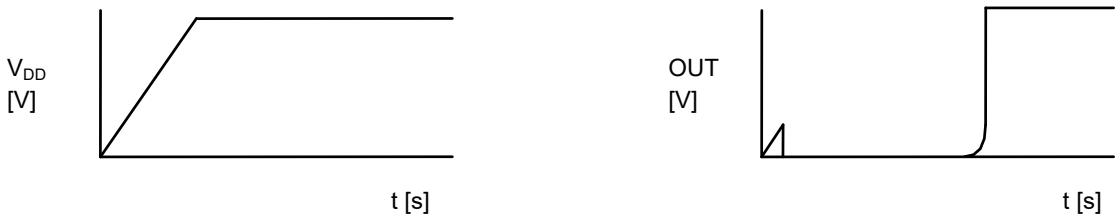


Figure 28

Remark When the power rises sharply, the output may instantaneously be set to the "H" level due to the IC's indefinite area (the output voltage is indefinite when it is the IC's minimum operation voltage or less), as seen in **Figure 29.**

Figure 29

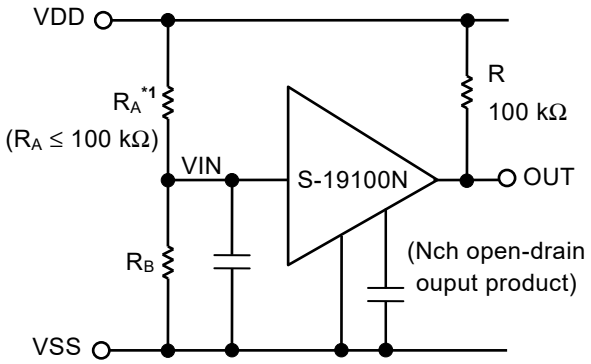
Caution 1. The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

2. Note that the hysteresis width may be larger as the following equation shows when using the above connection. Perform thorough evaluation using the actual application to set the constant.

Maximum hysteresis width = $V_{HYS} + R_A \bullet 20\ \mu A$

3. Change of detection voltage (Nch open-drain output product only)

If there is not a product with a specified detection voltage value in the S-19100NxxA Series, the detection voltage can be changed by using a resistance divider or a diode, as seen in **Figure 30** and **Figure 31**.
In **Figure 30**, the hysteresis width also changes.



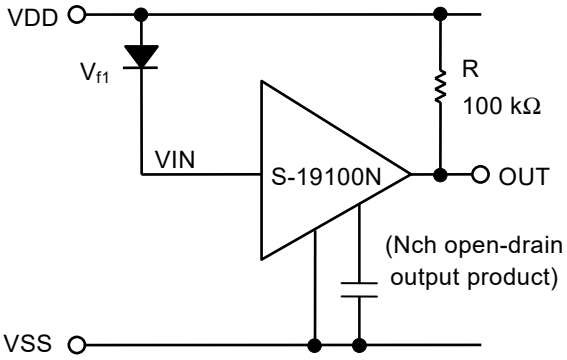
Detection voltage = $\frac{R_A + R_B}{R_B} \bullet -V_{DET}$

Hysteresis width = $\frac{R_A + R_B}{R_B} \bullet V_{HYS}$

***1.** R_A should be 100 kΩ or less to prevent oscillation.

Caution If R_A and R_B are large, the hysteresis width may also be larger than the value given by the above equation due to the feed-through current.

Figure 30



Detection voltage = $V_{f1} + (-V_{DET})$

Figure 31

Caution 1. The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

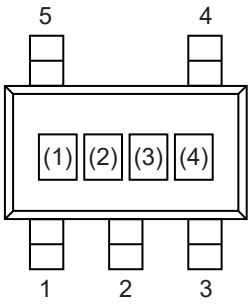
2. Note that the hysteresis width may be larger as the following equation shows when using the above connections. Perform thorough evaluation using the actual application to set the constant.

Maximum hysteresis width = $\frac{R_A + R_B}{R_B} \bullet V_{HYS} + R_A \bullet 20\ \mu A$

■ Marking Specifications

1. SOT-23-5

Top view



(1) to (3): Product code (Refer to **Product name vs. Product code**)
(4): Lot number

Product name vs. Product code

1. 1 Nch open-drain output product

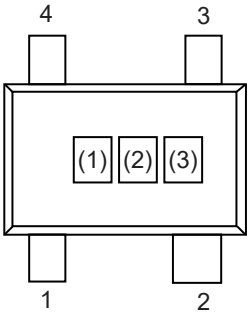
Product Name	Product Code		
	(1)	(2)	(3)
S-19100N12A-M5T2U	3	N	A
S-19100N13A-M5T2U	3	N	B
S-19100N14A-M5T2U	3	N	C
S-19100N15A-M5T2U	3	N	D
S-19100N16A-M5T2U	3	N	E
S-19100N17A-M5T2U	3	N	F
S-19100N18A-M5T2U	3	N	G
S-19100N19A-M5T2U	3	N	H
S-19100N20A-M5T2U	3	N	I
S-19100N21A-M5T2U	3	N	J
S-19100N22A-M5T2U	3	N	K
S-19100N23A-M5T2U	3	N	L
S-19100N24A-M5T2U	3	N	M
S-19100N25A-M5T2U	3	N	N
S-19100N26A-M5T2U	3	N	O
S-19100N27A-M5T2U	3	N	P
S-19100N28A-M5T2U	3	N	Q
S-19100N29A-M5T2U	3	N	R
S-19100N30A-M5T2U	3	N	S
S-19100N31A-M5T2U	3	N	T
S-19100N32A-M5T2U	3	N	U
S-19100N33A-M5T2U	3	N	V
S-19100N34A-M5T2U	3	N	W
S-19100N35A-M5T2U	3	N	X
S-19100N36A-M5T2U	3	N	Y
S-19100N37A-M5T2U	3	N	Z
S-19100N38A-M5T2U	3	N	1
S-19100N39A-M5T2U	3	N	2
S-19100N40A-M5T2U	3	N	3
S-19100N41A-M5T2U	3	N	4
S-19100N42A-M5T2U	3	N	5
S-19100N43A-M5T2U	3	N	6
S-19100N44A-M5T2U	3	N	7
S-19100N45A-M5T2U	3	N	8
S-19100N46A-M5T2U	3	N	9

1. 2 CMOS output product

Product Name	Product Code		
	(1)	(2)	(3)
S-19100C12A-M5T2U	3	M	A
S-19100C13A-M5T2U	3	M	B
S-19100C14A-M5T2U	3	M	C
S-19100C15A-M5T2U	3	M	D
S-19100C16A-M5T2U	3	M	E
S-19100C17A-M5T2U	3	M	F
S-19100C18A-M5T2U	3	M	G
S-19100C19A-M5T2U	3	M	H
S-19100C20A-M5T2U	3	M	I
S-19100C21A-M5T2U	3	M	J
S-19100C22A-M5T2U	3	M	K
S-19100C23A-M5T2U	3	M	L
S-19100C24A-M5T2U	3	M	M
S-19100C25A-M5T2U	3	M	N
S-19100C26A-M5T2U	3	M	O
S-19100C27A-M5T2U	3	M	P
S-19100C28A-M5T2U	3	M	Q
S-19100C29A-M5T2U	3	M	R
S-19100C30A-M5T2U	3	M	S
S-19100C31A-M5T2U	3	M	T
S-19100C32A-M5T2U	3	M	U
S-19100C33A-M5T2U	3	M	V
S-19100C34A-M5T2U	3	M	W
S-19100C35A-M5T2U	3	M	X
S-19100C36A-M5T2U	3	M	Y
S-19100C37A-M5T2U	3	M	Z
S-19100C38A-M5T2U	3	M	1
S-19100C39A-M5T2U	3	M	2
S-19100C40A-M5T2U	3	M	3
S-19100C41A-M5T2U	3	M	4
S-19100C42A-M5T2U	3	M	5
S-19100C43A-M5T2U	3	M	6
S-19100C44A-M5T2U	3	M	7
S-19100C45A-M5T2U	3	M	8
S-19100C46A-M5T2U	3	M	9

2. SC-82AB

Top view



(1) to (3): Product code (Refer to **Product name vs. Product code**)

Product name vs. Product code

2. 1 Nch open-drain output product

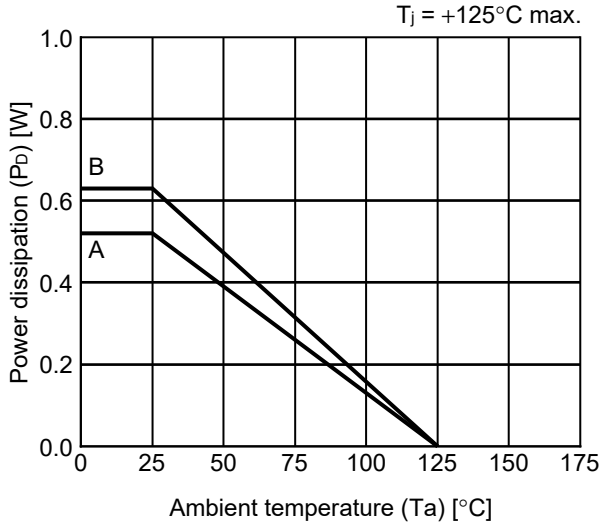
Product Name	Product Code		
	(1)	(2)	(3)
S-19100N12A-N4T2U	3	N	A
S-19100N13A-N4T2U	3	N	B
S-19100N14A-N4T2U	3	N	C
S-19100N15A-N4T2U	3	N	D
S-19100N16A-N4T2U	3	N	E
S-19100N17A-N4T2U	3	N	F
S-19100N18A-N4T2U	3	N	G
S-19100N19A-N4T2U	3	N	H
S-19100N20A-N4T2U	3	N	I
S-19100N21A-N4T2U	3	N	J
S-19100N22A-N4T2U	3	N	K
S-19100N23A-N4T2U	3	N	L
S-19100N24A-N4T2U	3	N	M
S-19100N25A-N4T2U	3	N	N
S-19100N26A-N4T2U	3	N	O
S-19100N27A-N4T2U	3	N	P
S-19100N28A-N4T2U	3	N	Q
S-19100N29A-N4T2U	3	N	R
S-19100N30A-N4T2U	3	N	S
S-19100N31A-N4T2U	3	N	T
S-19100N32A-N4T2U	3	N	U
S-19100N33A-N4T2U	3	N	V
S-19100N34A-N4T2U	3	N	W
S-19100N35A-N4T2U	3	N	X
S-19100N36A-N4T2U	3	N	Y
S-19100N37A-N4T2U	3	N	Z
S-19100N38A-N4T2U	3	N	1
S-19100N39A-N4T2U	3	N	2
S-19100N40A-N4T2U	3	N	3
S-19100N41A-N4T2U	3	N	4
S-19100N42A-N4T2U	3	N	5
S-19100N43A-N4T2U	3	N	6
S-19100N44A-N4T2U	3	N	7
S-19100N45A-N4T2U	3	N	8
S-19100N46A-N4T2U	3	N	9

2. 2 CMOS output product

Product Name	Product Code		
	(1)	(2)	(3)
S-19100C12A-N4T2U	3	M	A
S-19100C13A-N4T2U	3	M	B
S-19100C14A-N4T2U	3	M	C
S-19100C15A-N4T2U	3	M	D
S-19100C16A-N4T2U	3	M	E
S-19100C17A-N4T2U	3	M	F
S-19100C18A-N4T2U	3	M	G
S-19100C19A-N4T2U	3	M	H
S-19100C20A-N4T2U	3	M	I
S-19100C21A-N4T2U	3	M	J
S-19100C22A-N4T2U	3	M	K
S-19100C23A-N4T2U	3	M	L
S-19100C24A-N4T2U	3	M	M
S-19100C25A-N4T2U	3	M	N
S-19100C26A-N4T2U	3	M	O
S-19100C27A-N4T2U	3	M	P
S-19100C28A-N4T2U	3	M	Q
S-19100C29A-N4T2U	3	M	R
S-19100C30A-N4T2U	3	M	S
S-19100C31A-N4T2U	3	M	T
S-19100C32A-N4T2U	3	M	U
S-19100C33A-N4T2U	3	M	V
S-19100C34A-N4T2U	3	M	W
S-19100C35A-N4T2U	3	M	X
S-19100C36A-N4T2U	3	M	Y
S-191003C7A-N4T2U	3	M	Z
S-19100C38A-N4T2U	3	M	1
S-19100C39A-N4T2U	3	M	2
S-19100C40A-N4T2U	3	M	3
S-19100C41A-N4T2U	3	M	4
S-19100C42A-N4T2U	3	M	5
S-19100C43A-N4T2U	3	M	6
S-19100C44A-N4T2U	3	M	7
S-19100C45A-N4T2U	3	M	8
S-19100C46A-N4T2U	3	M	9

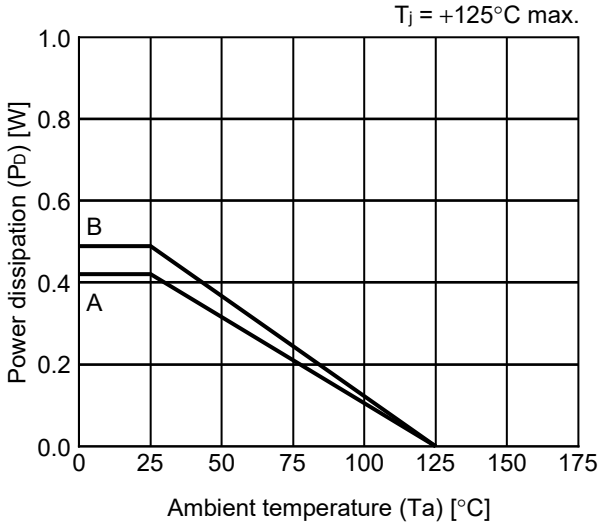
■ Power Dissipation

SOT-23-5



Board	Power Dissipation (P_D)
A	0.52 W
B	0.63 W
C	–
D	–
E	–

SC-82AB

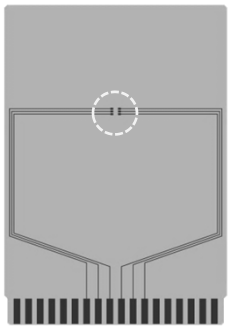


Board	Power Dissipation (P_D)
A	0.42 W
B	0.49 W
C	–
D	–
E	–

SOT-23-3/3S/5/6 Test Board

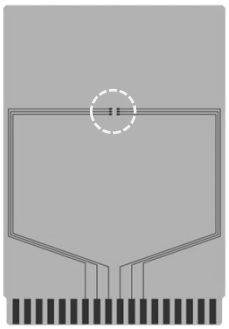
IC Mount Area

(1) Board A



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



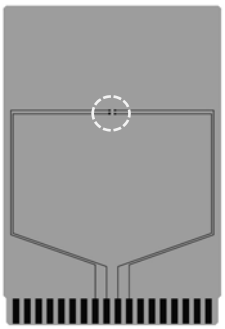
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

No. SOT23x-A-Board-SD-2.0

SC-82AB Test Board

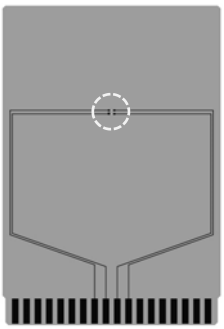
(1) Board A

IC Mount Area



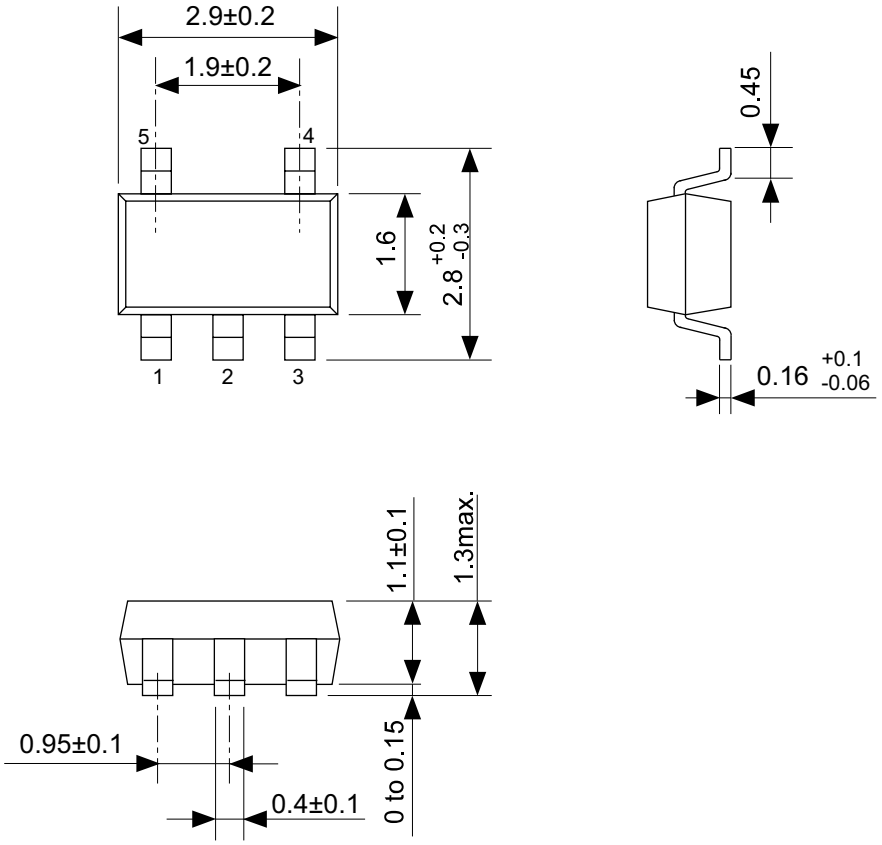
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

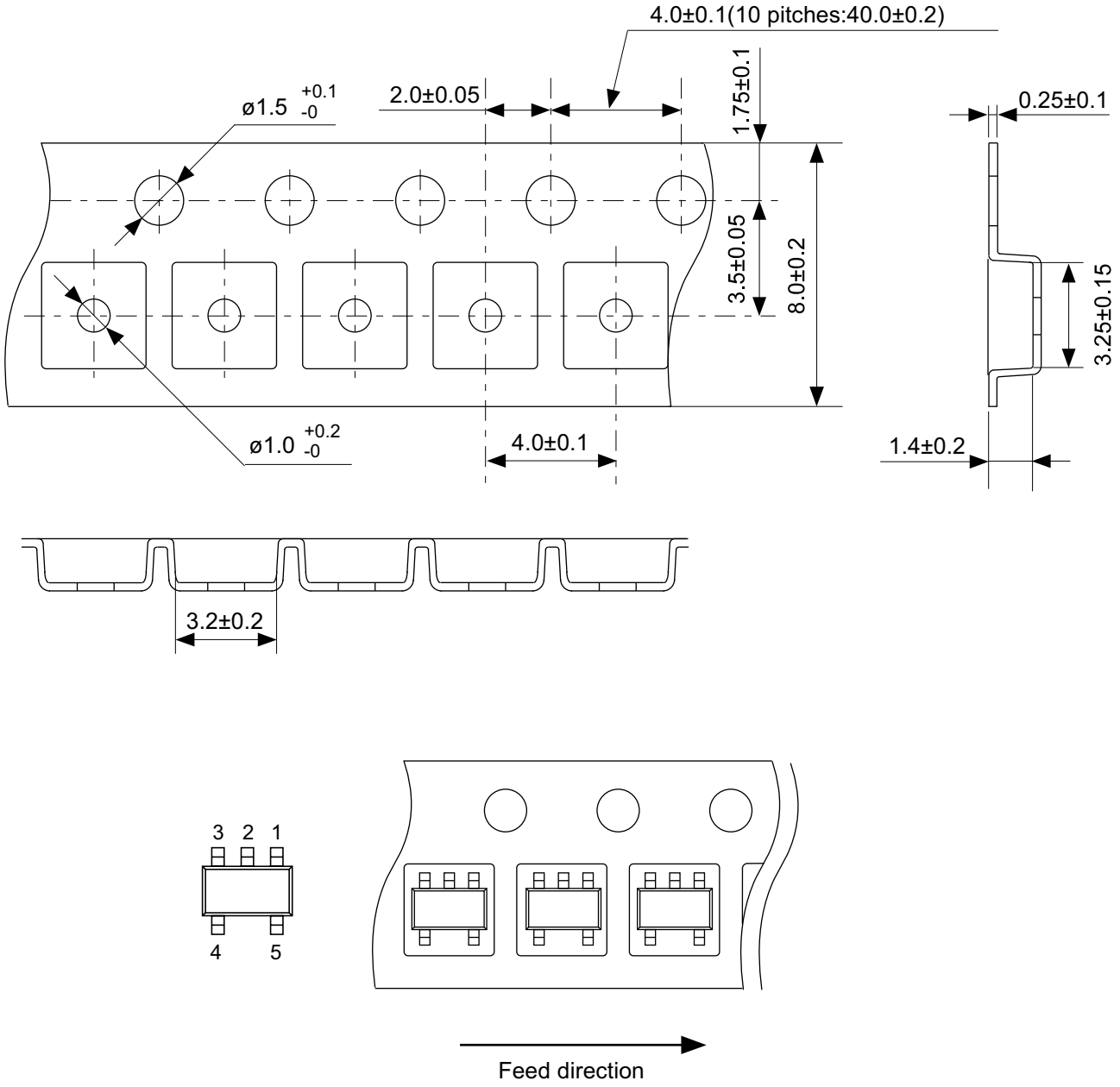
No. SC82AB-A-Board-SD-1.0



No. MP005-A-P-SD-1.3

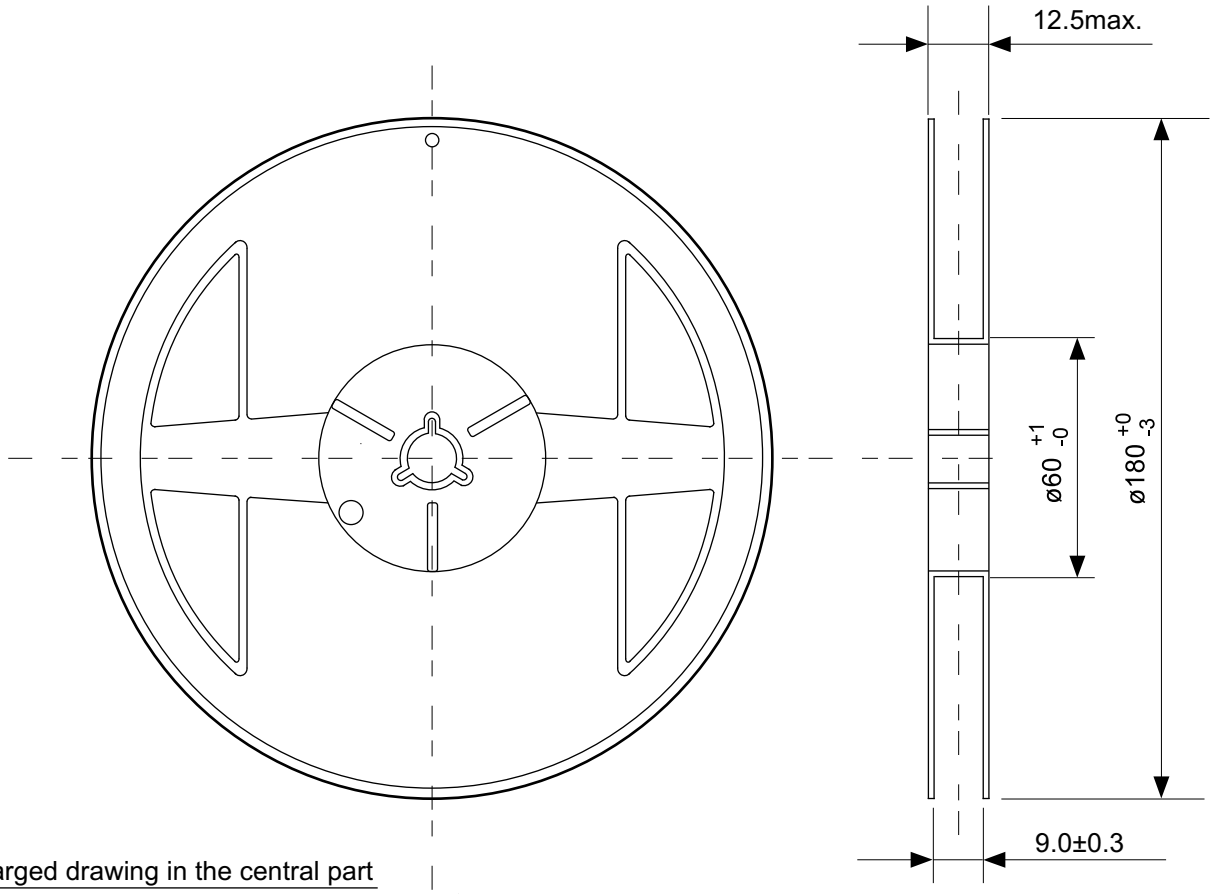
TITLE	SOT235-A-PKG Dimensions
No.	MP005-A-P-SD-1.3
ANGLE	
UNIT	mm

ABLIC Inc.

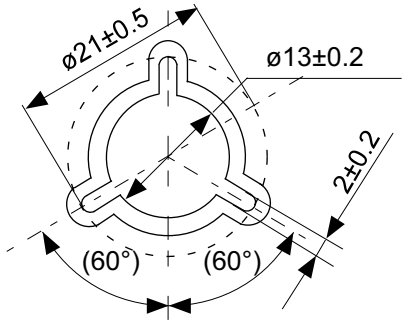


No. MP005-A-C-SD-2.1

TITLE	SOT235-A-Carrier Tape
No.	MP005-A-C-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	

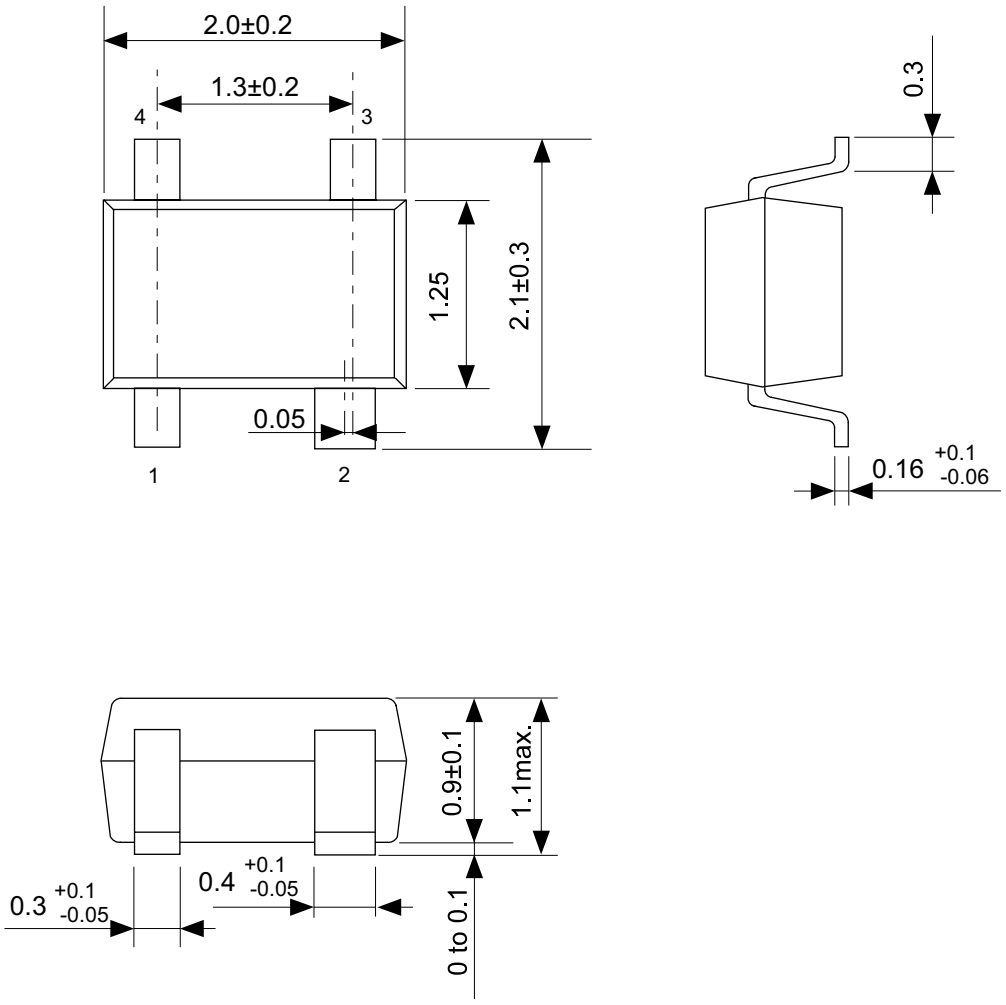


Enlarged drawing in the central part



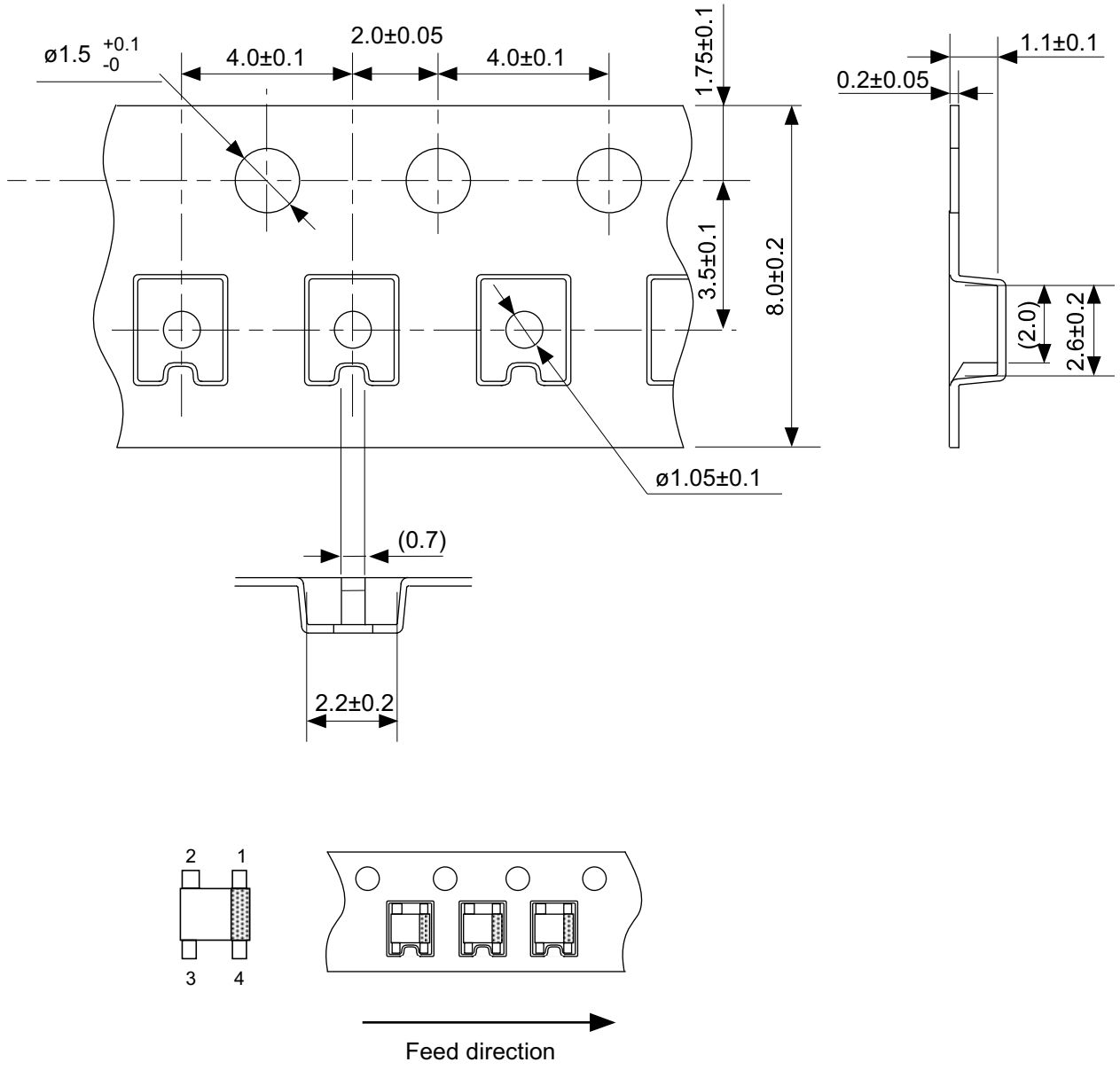
No. MP005-A-R-SD-1.1

TITLE	SOT235-A-Reel		
No.	MP005-A-R-SD-1.1		
ANGLE		QTY.	3,000
UNIT	mm		
ABLIC Inc.			



No. NP004-A-P-SD-2.0

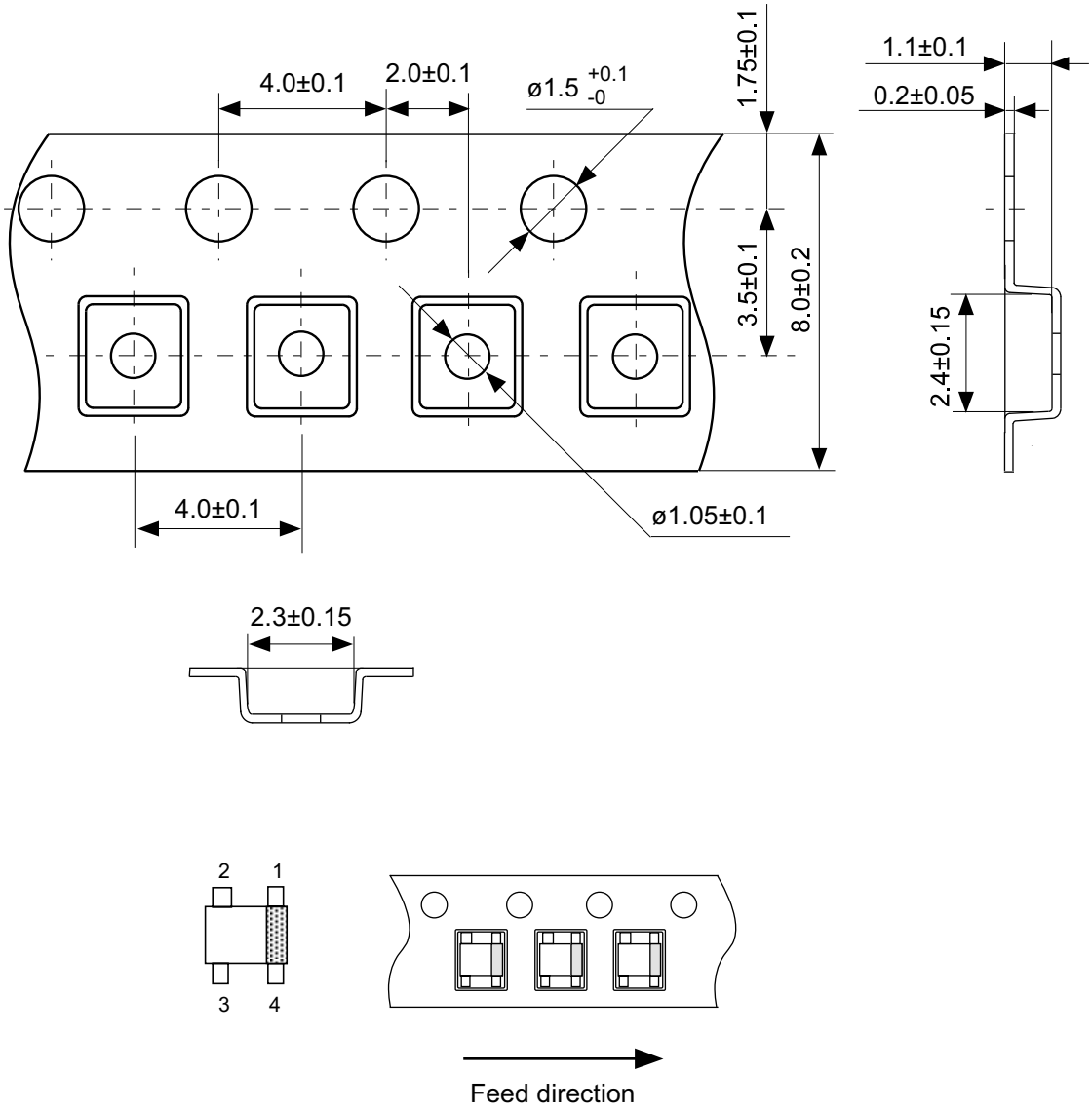
TITLE	SC82AB-A-PKG Dimensions
No.	NP004-A-P-SD-2.0
ANGLE	
UNIT	mm
	ABLIC Inc.



Feed direction

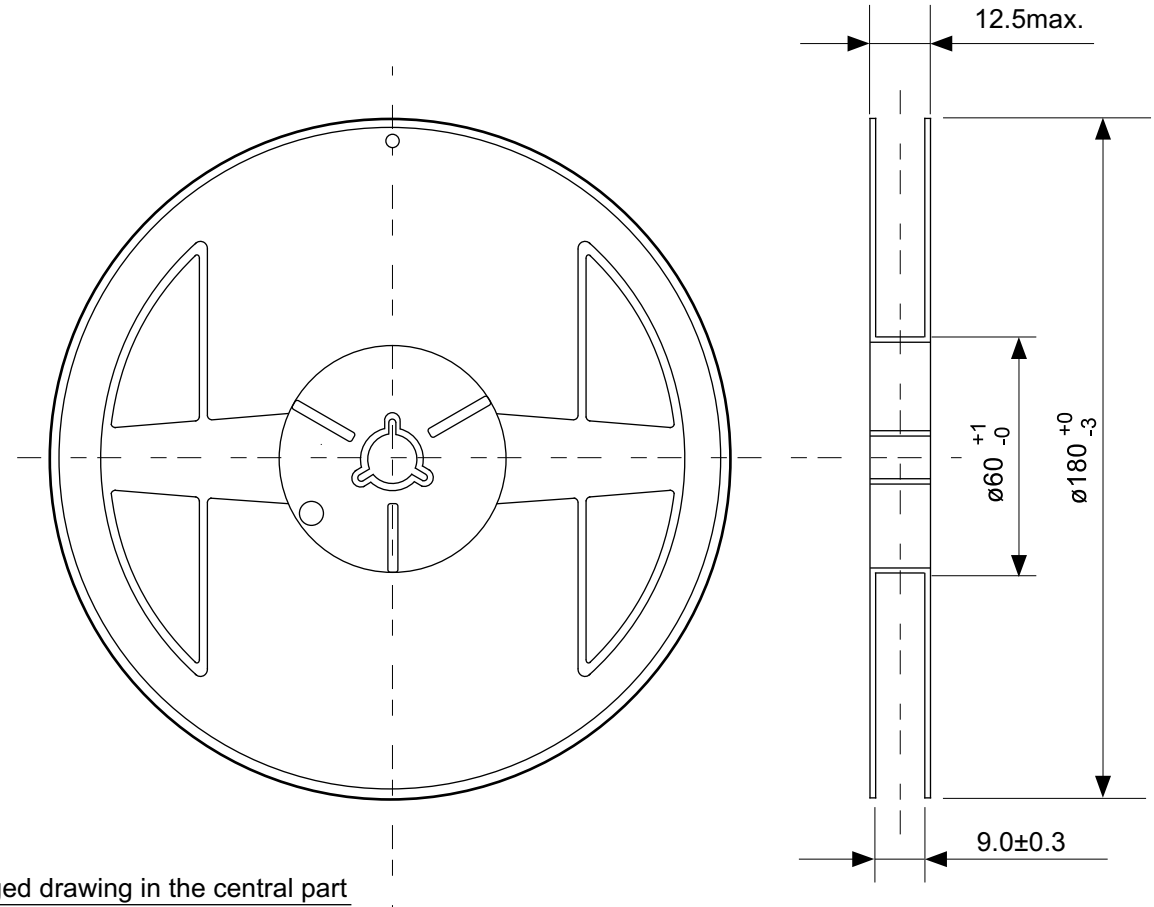
No. NP004-A-C-SD-3.0

TITLE	SC82AB-A-Carrier Tape
No.	NP004-A-C-SD-3.0
ANGLE	
UNIT	mm
	ABLIC Inc.

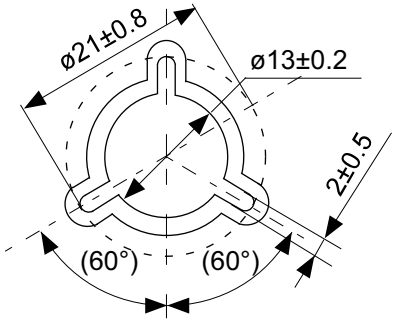


No. NP004-A-C-S1-2.0

TITLE	SC82AB-A-Carrier Tape
No.	NP004-A-C-S1-2.0
ANGLE	
UNIT	mm
	ABLIC Inc.



Enlarged drawing in the central part



No. NP004-A-R-SD-1.1

TITLE	SC82AB-A-Reel		
No.	NP004-A-R-SD-1.1		
ANGLE		QTY.	3,000
UNIT	mm		
	ABLIC Inc.		

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2.4-2019.07