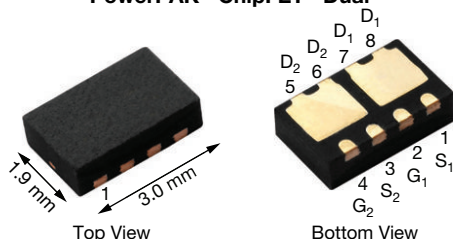


Dual N-Channel 40 V (D-S) MOSFET

PRODUCT SUMMARY

V _{DS} (V)	R _{DS(on)} (Ω) MAX.	I _D (A)	Q _g (TYP.)
40	0.082 at V _{GS} = 10 V	6 ^a	2.2 nC
	0.094 at V _{GS} = 4.5 V	6 ^a	

PowerPAK® ChipFET® Dual



Marking Code: CG

Ordering Information:

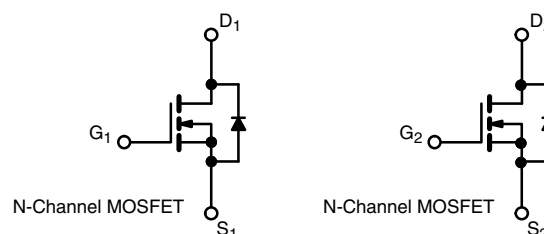
Si5948DU-T1-GE3 (lead (Pb)-free and halogen-free)

FEATURES

- TrenchFET® power MOSFET
- 100 % R_g and UIS tested
- New thermally enhanced PowerPAK® ChipFET® package
 - Small footprint area
 - Low on-resistance
 - Thin 0.8 mm profile
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- DC/DC power supply



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	40	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	I _D	6 ^a	A
		5.5	
		3.7 ^{b, c}	
		2.9 ^{b, c}	
Pulsed Drain Current (t = 100 μs)	I _{DM}	10	A
Continuous Source-Drain Diode Current	I _S	5.8	
		1.7 ^{b, c}	
Single Pulse Avalanche Current	I _{AS}	6	mJ
Avalanche Energy	E _{AS}	1.8	
Maximum Power Dissipation	P _D	7	W
		4.4	
		2 ^{b, c}	
		1.3 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum Junction-to-Ambient ^{b, f}	R _{thJA}	52	62	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	15	18	

Notes

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- t = 5 s.
- See solder profile (www.vishay.com/ppg?73257). The PowerPAK ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 105 °C/W.



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	40	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA	-	45.3	-	mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J		-	-4.1	-	
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1	-	2.5	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 40 V, V _{GS} = 0 V	-	-	-1	μA
		V _{DS} = 40 V, V _{GS} = 0 V, T _J = 55 °C	-	-	-10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	5	-	-	A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 5 A	-	0.065	0.082	Ω
		V _{GS} = 4.5 V, I _D = 3 A	-	0.074	0.094	
Forward Transconductance ^a	g _{fs}	V _{DS} = 20 V, I _D = 5 A	-	11	-	S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz	-	165	-	pF
Output Capacitance	C _{oss}		-	30	-	
Reverse Transfer Capacitance	C _{rss}		-	13	-	
Total Gate Charge	Q _g	V _{DS} = 20 V, V _{GS} = 10 V, I _D = 10 A	-	3.3	5	nC
		V _{DS} = 20 V, V _{GS} = 4.5 V, I _D = 10 A	-	1.7	2.6	
Gate-Source Charge	Q _{gs}		-	0.53	-	
Gate-Drain Charge	Q _{gd}		-	0.63	-	
Gate Resistance	R _g	f = 1 MHz	1.3	6.5	13	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 20 V, R _L = 4 Ω I _D ≅ 5 A, V _{GEN} = 10 V, R _g = 1 Ω	-	5	10	ns
Rise Time	t _r		-	25	50	
Turn-Off Delay Time	t _{d(off)}		-	7	15	
Fall Time	t _f		-	10	20	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 20 V, R _L = 4 Ω I _D ≅ 5 A, V _{GEN} = 4.5 V, R _g = 1 Ω	-	11	20	
Rise Time	t _r		-	41	80	
Turn-Off Delay Time	t _{d(off)}		-	9	20	
Fall Time	t _f		-	25	50	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	-	-	5.8	A
Pulse Diode Forward Current (t = 100 μs)	I _{SM}		-	-	10	
Body Diode Voltage	V _{SD}	I _S = 5 A, V _{GS} = 0 V	-	0.9	1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 5 A, dI/dt = 100 A/μs, T _J = 25 °C	-	15	30	ns
Body Diode Reverse Recovery Charge	Q _{rr}		-	8	15	nC
Reverse Recovery Fall Time	t _a		-	9	-	ns
Reverse Recovery Rise Time	t _b		-	6	-	

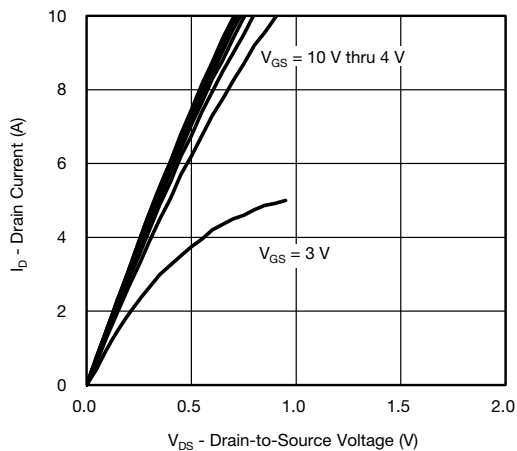
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

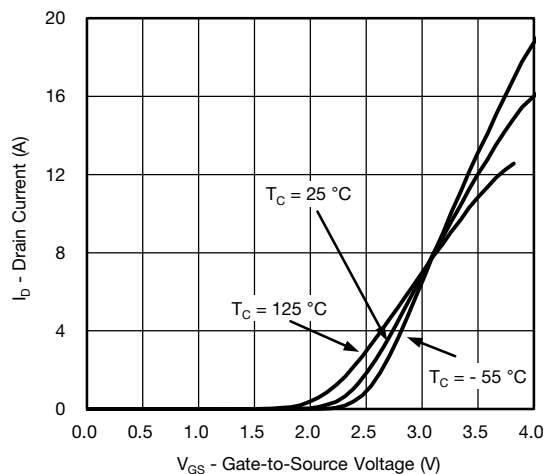
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



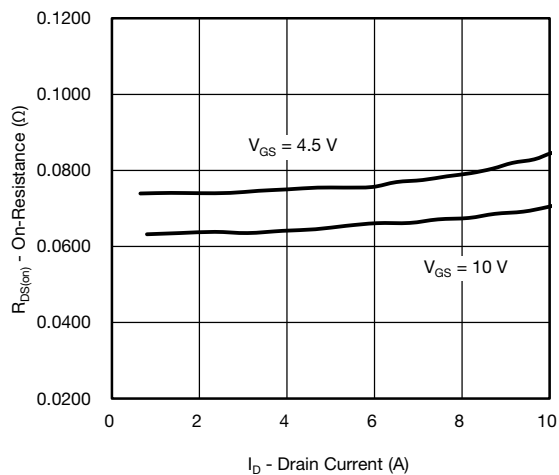
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



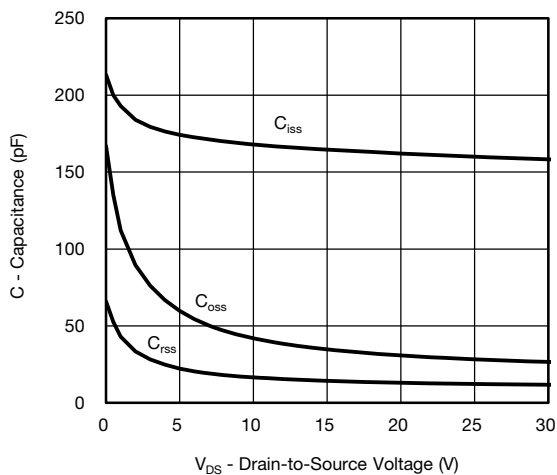
Output Characteristics



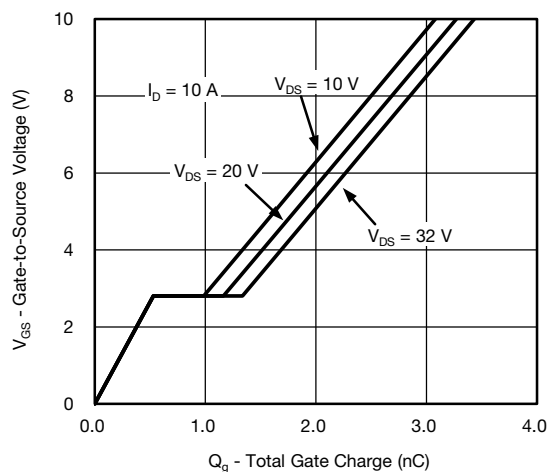
Transfer Characteristics



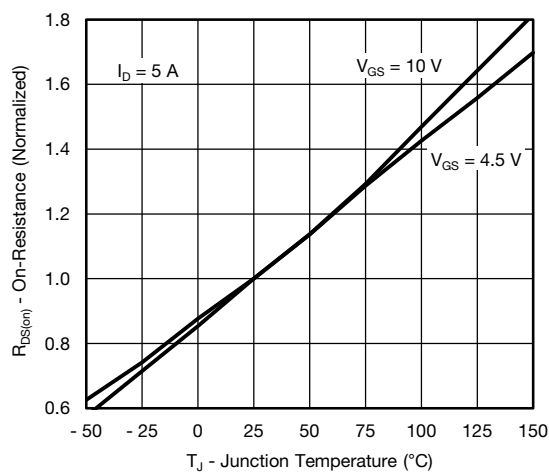
On-Resistance vs. Drain Current and Gate Voltage



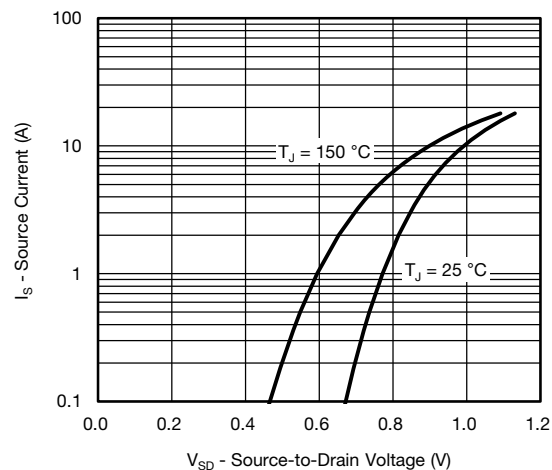
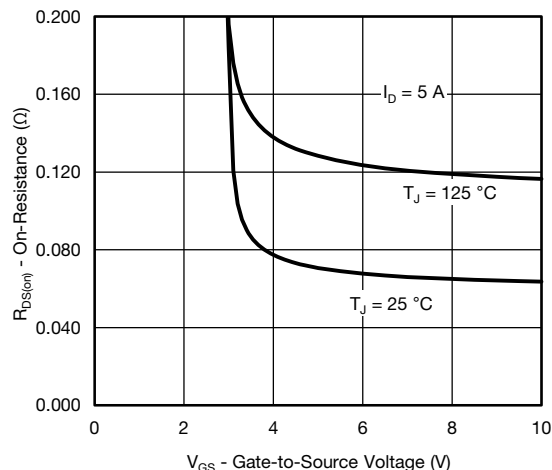
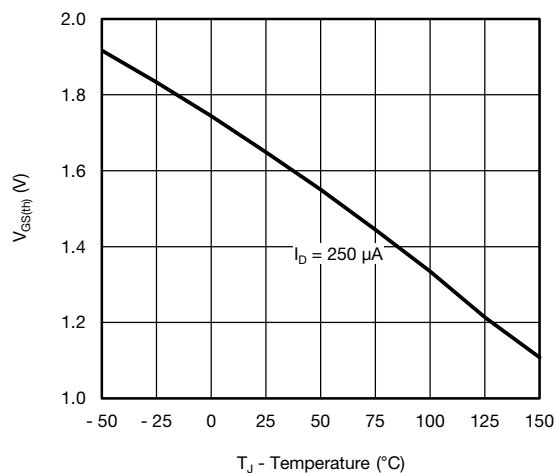
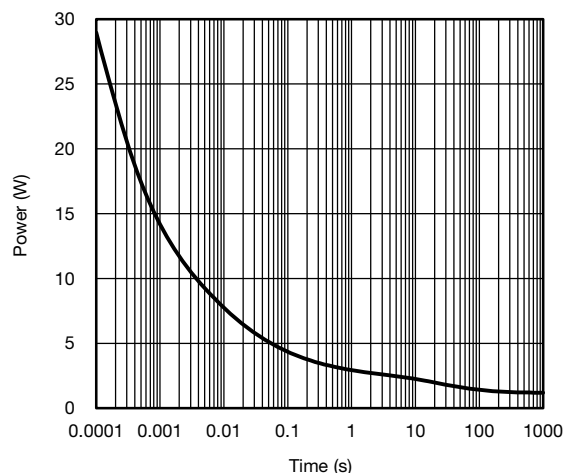
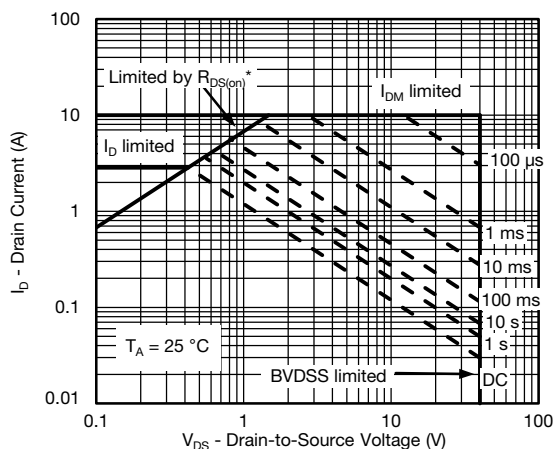
Capacitance

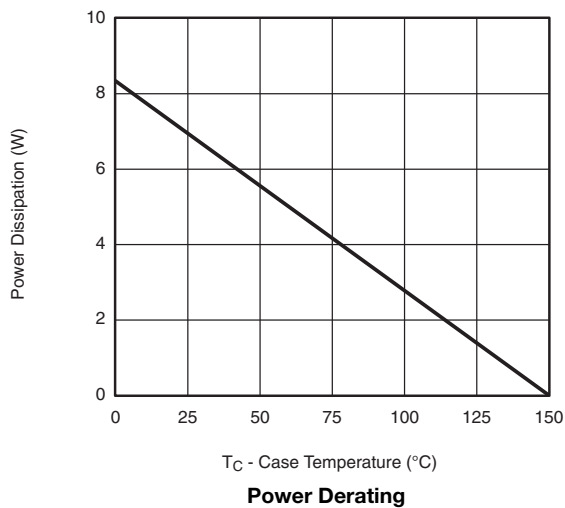
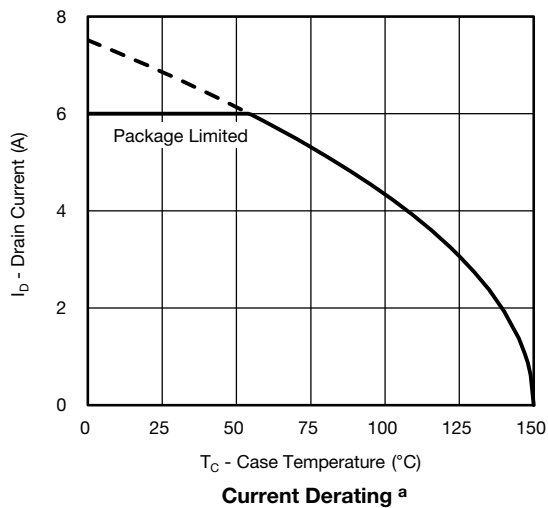


Gate Charge



On-Resistance vs. Junction Temperature

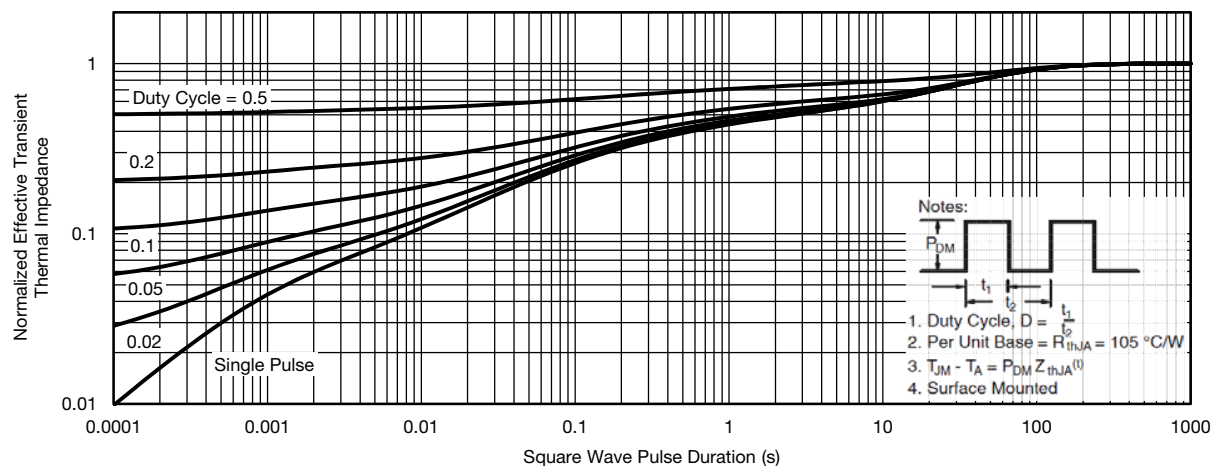
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Single Pulse Power, Junction-to-Ambient

Safe Operating Area

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Note

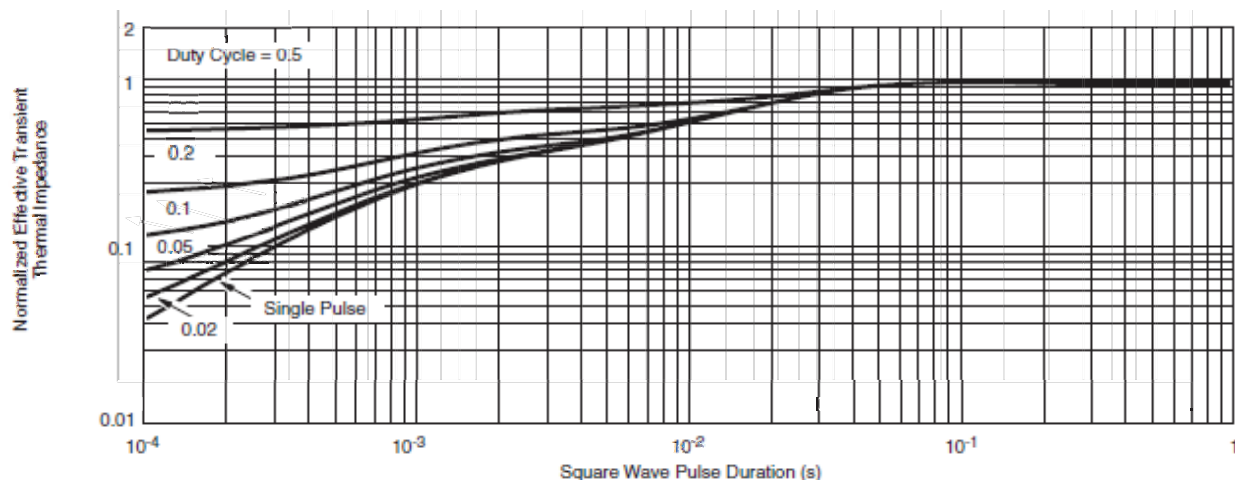
- a. The power dissipation P_D is based on T_J (max.) = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

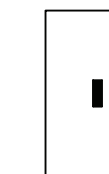
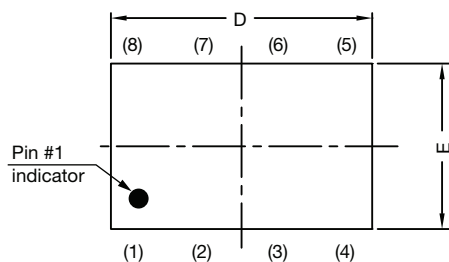


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?76424.



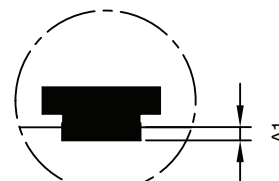
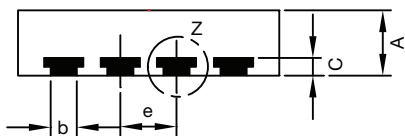
PowerPAK® ChipFET® Case Outline



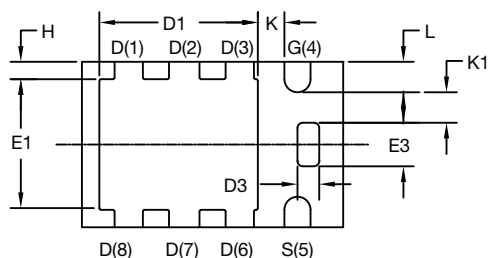
Side view of single



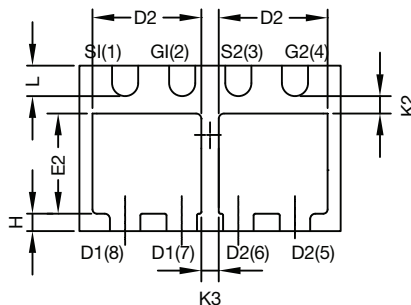
Side view of dual



Detail Z



Backside view of single pad



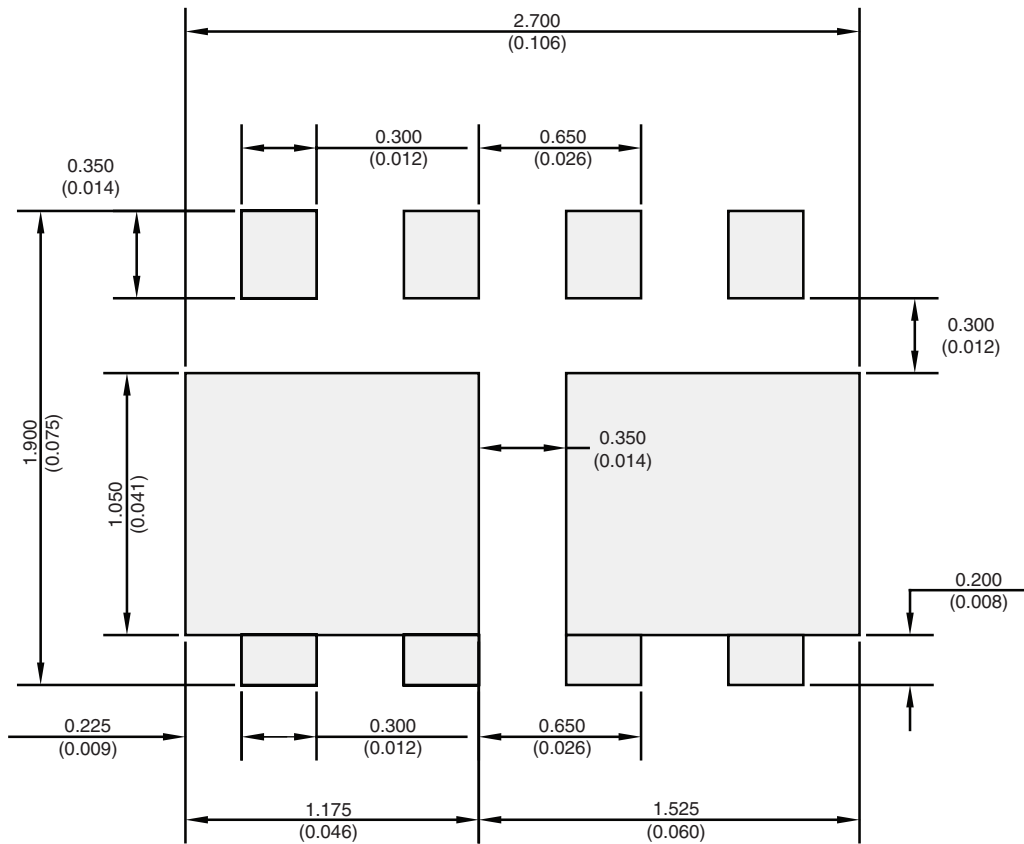
Backside view of dual pad

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.85	0.028	0.030	0.033
A1	0	-	0.05	0	-	0.002
b	0.25	0.30	0.35	0.010	0.012	0.014
C	0.15	0.20	0.25	0.006	0.008	0.010
D	2.92	3.00	3.08	0.115	0.118	0.121
D1	1.75	1.87	2.00	0.069	0.074	0.079
D2	1.07	1.20	1.32	0.042	0.047	0.052
D3	0.20	0.25	0.30	0.008	0.010	0.012
E	1.82	1.90	1.98	0.072	0.075	0.078
E1	1.38	1.50	1.63	0.054	0.059	0.064
E2	0.92	1.05	1.17	0.036	0.041	0.046
E3	0.45	0.50	0.55	0.018	0.020	0.022
e	0.65 BSC			0.026 BSC		
H	0.15	0.20	0.25	0.006	0.008	0.010
K	0.25	-	-	0.010	-	-
K1	0.30	-	-	0.012	-	-
K2	0.20	-	-	0.008	-	-
K3	0.20	-	-	0.008	-	-
L	0.30	0.35	0.40	0.012	0.014	0.016
C14-0630-Rev. E, 21-Jul-14						
DWG: 5940						

Note

- Millimeters will govern

RECOMMENDED MINIMUM PADS FOR PowerPAK® ChipFET® Dual



Recommended Minimum Pads
Dimensions in mm/(Inches)

Note: This is Flipped Mirror Image
Pin #1 Location is Top Left Corner



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