

6.5 mΩ, Bidirectional Switch in Compact WCSP

DESCRIPTION

The SiP32101, SiP32102, SiP32103, and SiP32104 are low resistance bidirectional load switches. They isolate A and B ports at off state. The parts have an ultra low 6.5 mΩ (typ. at 3.3 V) on-resistance and operate from a + 2.3 V to + 5.5 V input voltage range, making the devices ideal battery-disconnect switches for high capacity battery applications and multi-source power switches where bidirectional on/off control is required. The parts have identical A and B ports conducting current in both directions equally well.

The SiP32101, SiP32102, SiP32103, and SiP32104 have slew rate control minimizing switch on in-rush current in large load capacitor. These devices are also highly efficient, featuring low operating and shutdown currents.

The SiP32101, SiP32102, SiP32103, and SiP32104 can interface directly with a low voltage control signal. The SiP32101, SiP32103, and SiP32104 have an active low enable with different EN pull options. The SiP32102 has an active high enable. The series provides choices to minimize enable control circuit current depending on application requirement.

The SiP32101, SiP32102, SiP32103, and SiP32104 are available in an ultra compact 12-bump, 1.3 mm x 1.7 mm, 0.4 mm pitch WCSP package with top side lamination. The device operates over the temperature of -40 °C to +85 °C.

FEATURES

- Bidirectional on and off
- 7 A continuous current capability
- Ultra low R_{on} , 6.5 mΩ (typ.) at 3.3 V
- Wide input voltage, 2.3 V to 5.5 V
- Slew rate controlled turn on
- Low quiescent current: 110 nA
- High / low EN, and integrated pull options
- Compact 12-bump, 1.3 mm x 1.7 mm x 0.55 mm WCSP package
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Smartphones and tablets
- Digital still / video cameras
- Portable meters and test instruments
- Communication devices with embedded batteries
- Portable medical and healthcare systems
- Data storage
- Battery bank

TYPICAL APPLICATION CIRCUIT

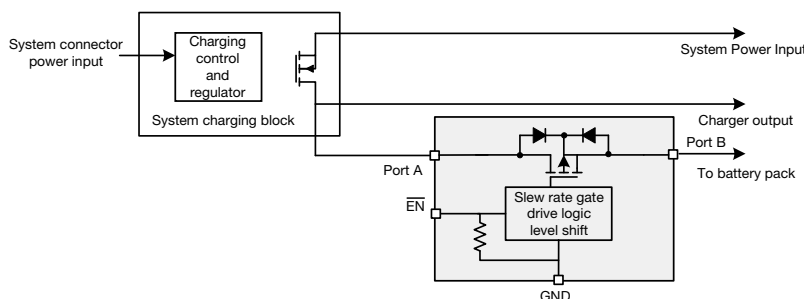


Fig. 1 - Typical Application Circuit

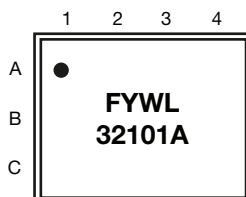
ORDERING INFORMATION					
PART NUMBER	MARKING	ENABLE	ENABLE PULL RESISTOR	PACKAGE	TEMPERATURE
SiP32101DB-T1-GE1	32101A	Low	Enable pull low	12-bump, 1.3 mm x 1.7 mm, 0.4 mm pitch WCSP package	-40 °C to +85 °C
SiP32102DB-T1-GE1	32102A	High	Enable pull low		
SiP32103DB-T1-GE1	32103A	Low	Enable pull high		
SiP32104DB-T1-GE1	32104A	Low	No pull		
SiP32101EVB	-	-	-	Evaluation board	-
SiP32102EVB	-	-	-		-
SiP32103EVB	-	-	-		-
SiP32104EVB	-	-	-		-

Note

- GE1 denotes halogen-free and RoHS-compliant



MARKING FORMAT



ABSOLUTE MAXIMUM RATINGS			
PARAMETER	CONDITIONS	LIMIT	UNIT
V_{PA}, V_{PB}	Reference to GND	-0.3 to +6	V
	Pulse at 1 ms reference to GND ^a	-1.6	
V_{EN}	Reference to GND	-0.3 to +6	
Maximum continuous switch current		7	A
Maximum pulse current	100 μ s pulse	15	
ESD (HBM)		8000	V
Operating temperature		-40 to +85	$^{\circ}$ C
Operating junction temperature		125	
Storage temperature		-65 to +150	
Thermal resistance (θ_{JA}) ^b		73	$^{\circ}$ C/W
Power dissipation (P_D) ^{b, c}	$T_A = 70^{\circ}$ C	1096	mW

Notes

- a. Negative current injection up to 300 mA
b. All bumps soldered to 1" x 1", 2 oz. copper, 4 layers PC board
c. Derate 13.7 mW/ $^{\circ}$ C above $T_A = 70^{\circ}$ C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

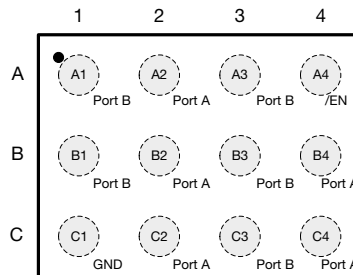
SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS SPECIFIED $V_{IN} = V_{PA}/V_{PB} = 2.3\text{ V to }5.5\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }85\text{ }^{\circ}\text{C}$ (Typical values are at V_{PA} , $V_{PB} = 4.2\text{ V}$, C_{PA} , $C_{PB} = 0.1\text{ }\mu\text{F}$, $T_A = 25\text{ }^{\circ}\text{C}$)	LIMITS			UNIT
			MIN. ^a	TYP. ^b	MAX. ^a	
Power Supply						
Operating voltage ^c	$V_{PA/PB}$		2.3	-	5.5	V
Quiescent current	I_Q	$V_{\overline{EN}} = 0\text{ V}$ (for SiP32101 and SiP32104), $V_{\overline{EN}} = V_{IN}$ (for SiP32102), no load	-	110	140	nA
		$V_{\overline{EN}} = 0\text{ V}$ (for SiP32103), no load	-	8.2	15	μA
Shutdown current	I_{SHDN}	$V_{\overline{EN}} = V_{IN}$ (for SiP32101, SiP32103, and SiP32104), $V_{\overline{EN}} = 0\text{ V}$ (for SiP32102), no load	-	110	140	nA
Internal FET						
On-resistance	$R_{DS(on)}$	$V_{PA}/V_{PB} = 2.3\text{ V}$, $I_L = 500\text{ mA}$, $T_A = 25\text{ }^{\circ}\text{C}$	-	8	13	$\text{m}\Omega$
		$V_{PA}/V_{PB} = 3.3\text{ V}$, $I_L = 500\text{ mA}$, $T_A = 25\text{ }^{\circ}\text{C}$	-	6.5	10	
Control						
$\overline{\text{EN}}$ input logic-low voltage ^c	V_{IL}		-	-	0.4	V
$\overline{\text{EN}}$ input logic-high voltage ^c	V_{IH}		1.4	-	-	
$\overline{\text{EN}}$ input logic hysteresis	$V_{I(HYS)}$		-	> 200	-	mV
$\overline{\text{EN}}$ pull resistor	$R_{\overline{\text{EN}}}$	$V_{PA}/V_{PB} = 5.5\text{ V}$, $V_{\overline{\text{EN}}}$ (or $V_{\text{EN}}) = 2.3\text{ V}$	350	500	700	k Ω

SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS SPECIFIED $V_{IN} = V_{PA}/V_{PB} = 2.3 \text{ V to } 5.5 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } 85 \text{ }^{\circ}\text{C}$ (Typical values are at V_{PA} , $V_{PB} = 4.2 \text{ V}$, C_{PA} , $C_{PB} = 0.1 \text{ }\mu\text{F}$, $T_A = 25 \text{ }^{\circ}\text{C}$)	LIMITS			UNIT
			MIN. ^a	TYP. ^b	MAX. ^a	
Timing						
Output turn-on delay time	$t_{d(on)}$	$V_{IN} = 4.2 \text{ V}$, $R_L = 100 \text{ }\Omega$, $C_L = 0.1 \text{ }\mu\text{F}$, $T_A = 25 \text{ }^{\circ}\text{C}$	-	0.8	-	ms
Output turn-on rise time	t_r		-	1	-	
Output turn-off delay time	$t_{d(off)}$		-	0.12	-	
Output turn-off fall time	t_f		-	0.1	-	

Notes

- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing
- For V_{IN} outside this range consult typical $\overline{\text{EN}}$, EN threshold curve

BUMP CONFIGURATION



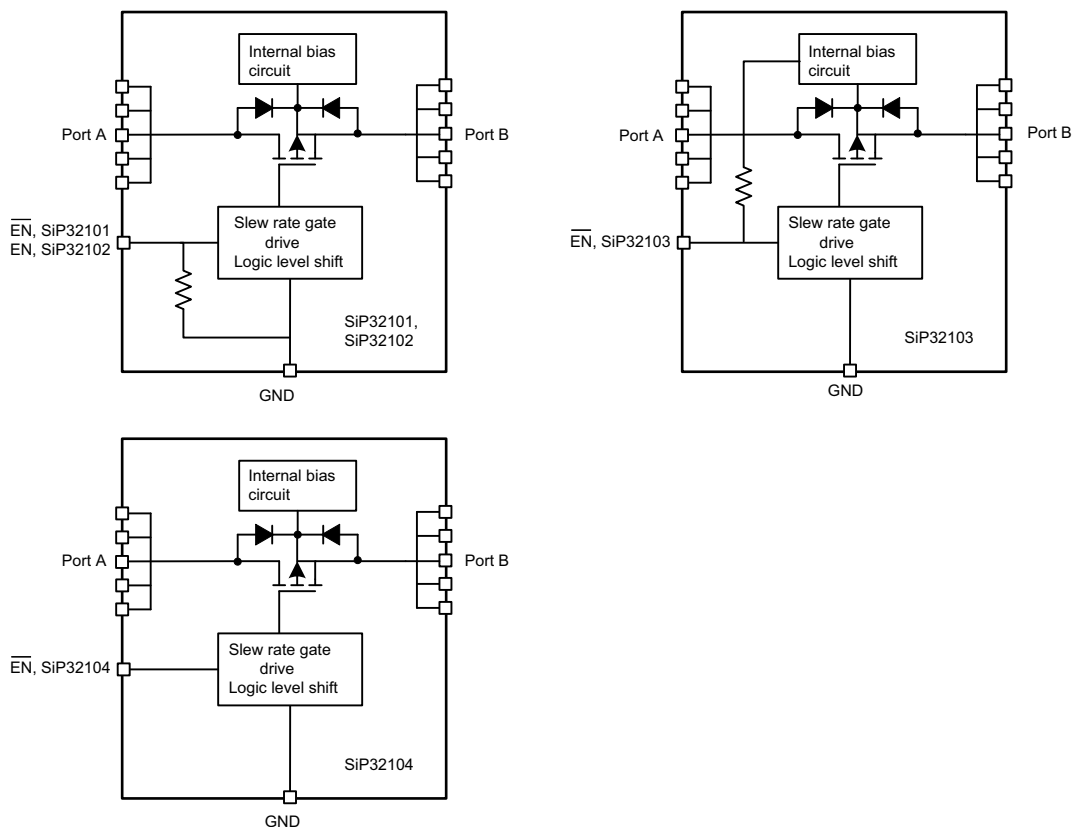
Top view
(solder bumps on bottom)

Fig. 2 - WCSP12, 1.3 mm x 1.7 mm

BUMP DESCRIPTION		
BUMP NUMBER	NAME	FUNCTION
A1, B1, A3, B3, C3	PB	Power port B
C1	GND	Ground
A2, B2, C2, B4, C4	PA	Power port A
A4	$\overline{\text{EN}}$	Switch enable input, active low



FUNCTIONAL BLOCK DIAGRAM





TYPICAL CHARACTERISTICS (internally regulated 25 °C, unless otherwise noted)

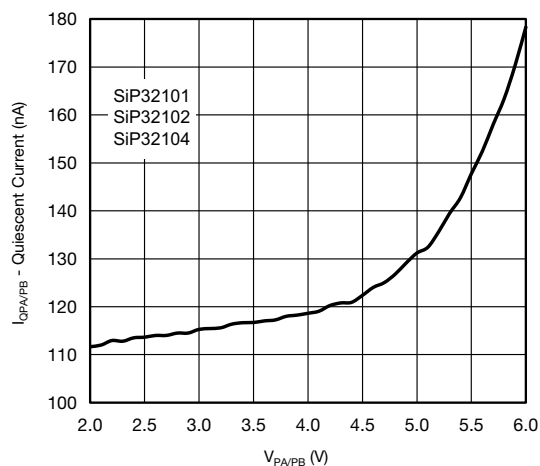


Fig. 3 - Quiescent vs. Input Voltage

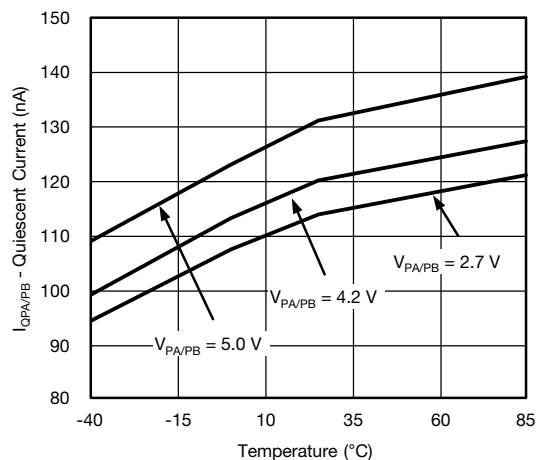


Fig. 6 - Quiescent vs. Temperature

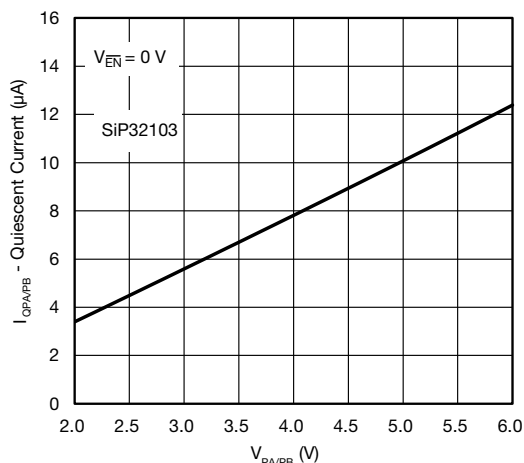


Fig. 4 - Quiescent vs. Input Voltage

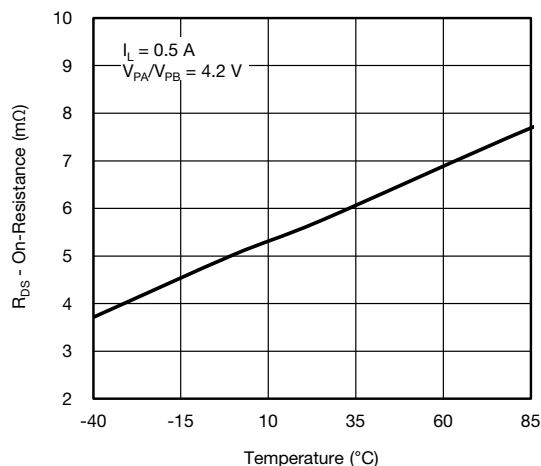


Fig. 7 - On Resistance vs. Temperature

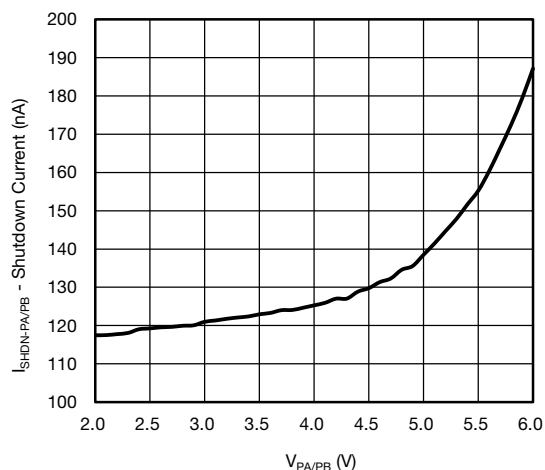


Fig. 5 - Shutdown Current vs. Input Voltage

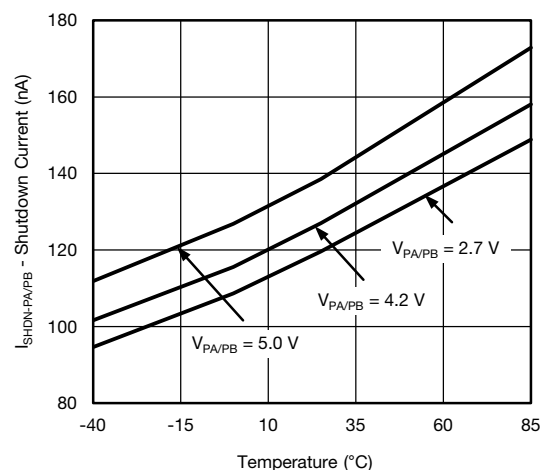


Fig. 8 - Shutdown Current vs. Temperature



TYPICAL CHARACTERISTICS (internally regulated 25 °C, unless otherwise noted)

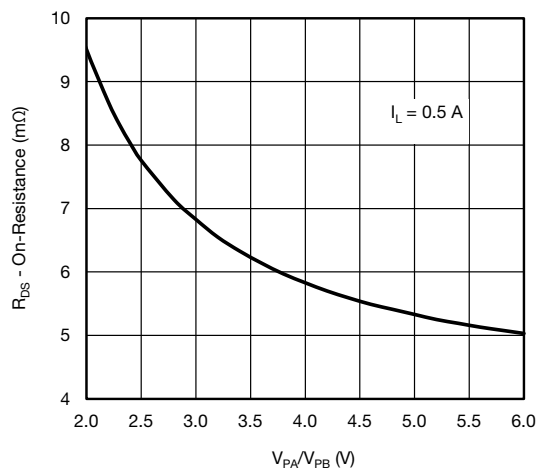


Fig. 9 - On Resistance vs. Input Voltage

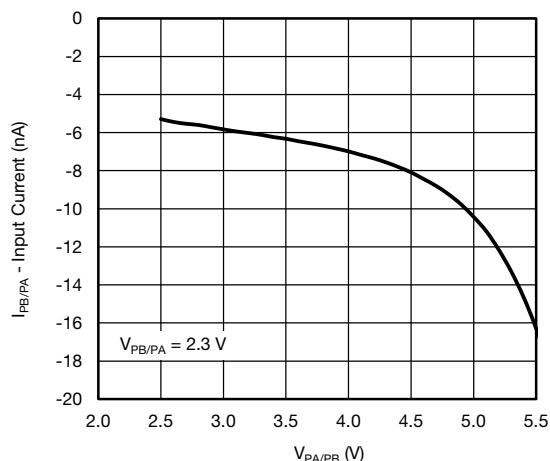


Fig. 12 - Reverse Blocking Current (I_{RB}) vs. Output Voltage

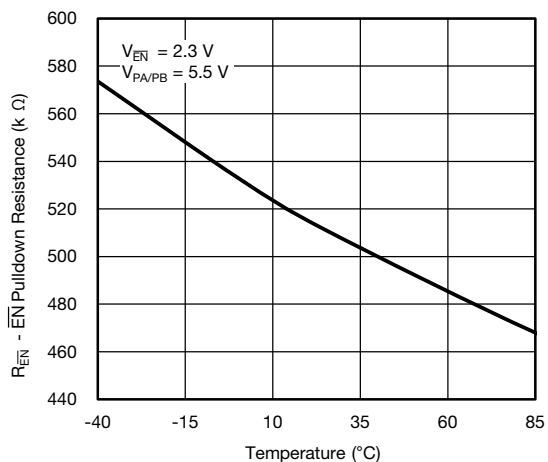


Fig. 10 - EN Pull Down Resistance vs. Temperature

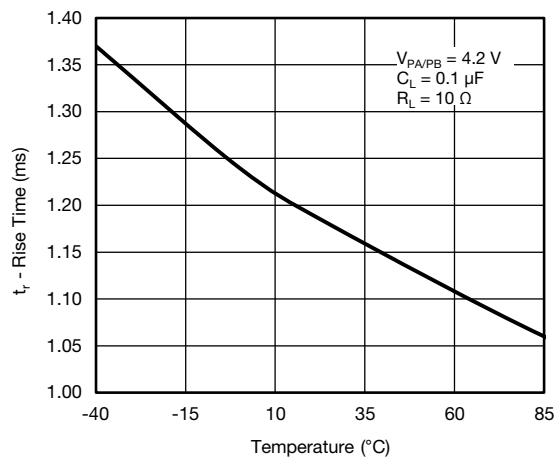


Fig. 13 - Rise Time vs. Temperature

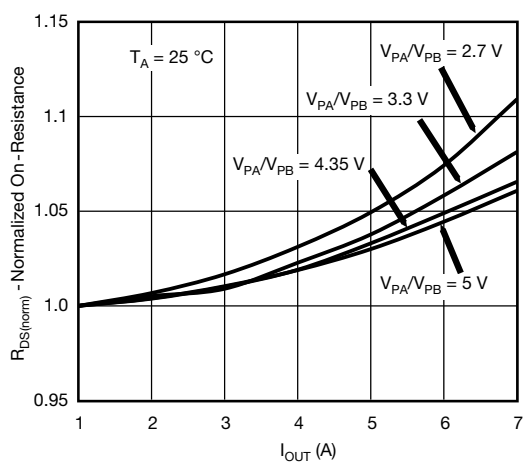


Fig. 11 - Normalized On Resistance vs. Load Current

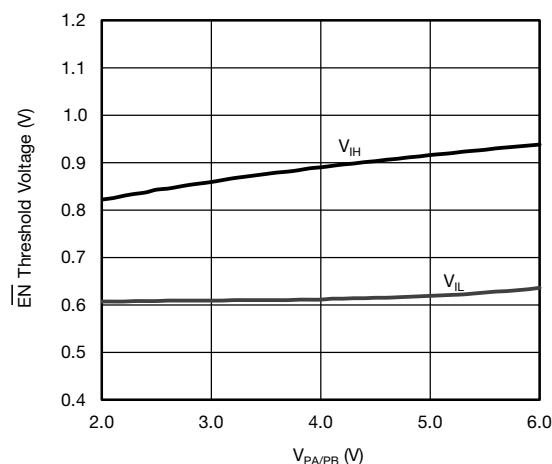


Fig. 14 - EN Threshold Voltage vs. Input Voltage



TYPICAL CHARACTERISTICS (internally regulated 25 °C, unless otherwise noted)

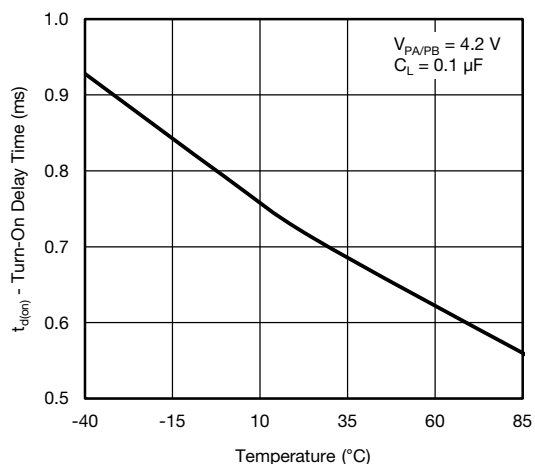


Fig. 15 - Turn-on Delay Time vs. Temperature

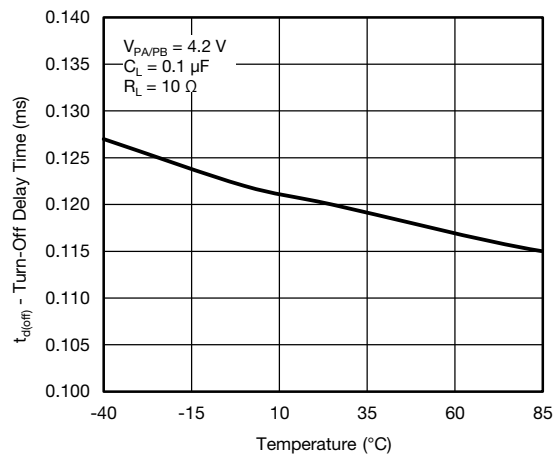


Fig. 16 - Turn-off Delay Time vs. Temperature

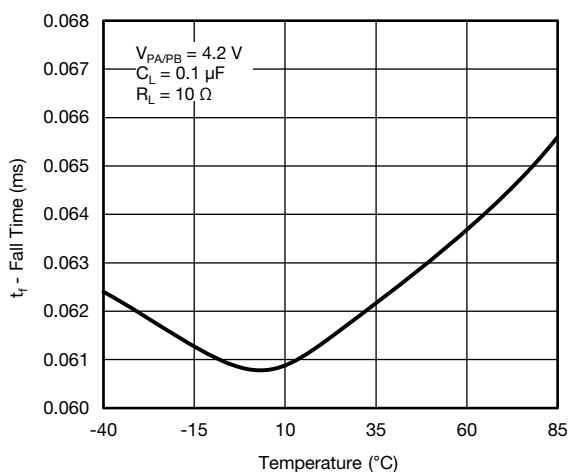


Fig. 17 - Fall Time vs. Temperature

DETAILED DESCRIPTION

The SiP32101 bidirectional switch features reverse blocking capability to isolate the battery from the system. The internal switch has an ultra low 6.5 m Ω (typ. at 3.3 V) on-resistance and operates from a +2.3 V to +5.5 V input voltage range, making the device ideal battery disconnect-switch for high capacity battery applications. The parts can handle 7 A continuous current at both directions.

The SiP32101 has slew rate control, making it ideal in large load capacitor as well as high current load switching applications.

The SiP32101 is available in an ultra compact 12-bump, 1.3 mm x 1.7 mm, 0.4 mm pitch WCSP package with top side lamination. The device operates over the temperature of -40 °C to +85 °C.

REVERSE CURRENT BLOCKING

The SiP32101 is a bidirectional switch that prevent current flowing from either port to the other when the device is disabled.

EN INPUT

SiP32101 has an active-low enable pin which can interface with low voltage GPIO directly. The switch is on when EN is low and off when EN is high. The SiP32101 has an integrated pull down resistor at $\overline{\text{EN}}$ pin.

SWITCH ON AND OFF PERFORMANCE

The SiP32101 has a slew rate control. This minimizes the inrush current and provides a soft turn on.

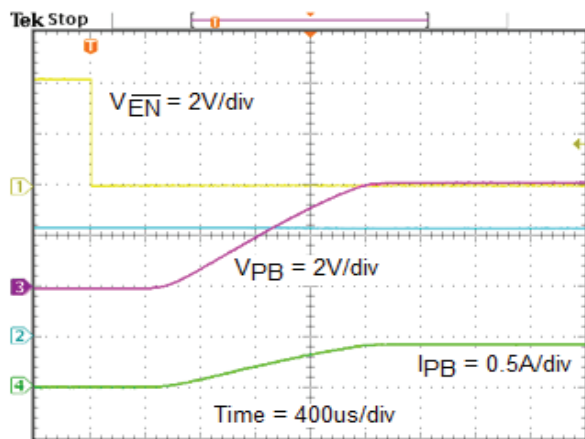


Fig. 18 - Port B Turn-On Time
($V_{PA} = 4.2 \text{ V}$, $R_L = 10 \Omega$, $C_L = 0.1 \mu\text{F}$)

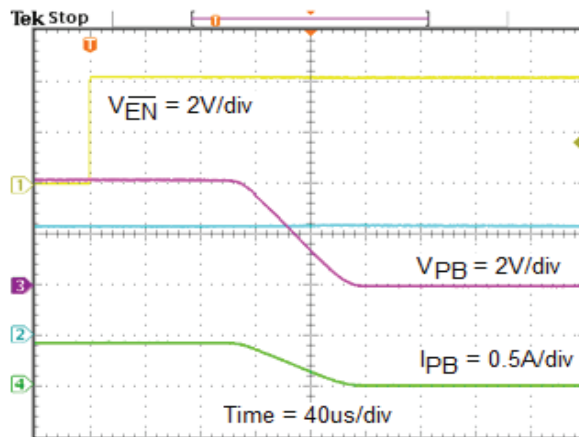


Fig. 19 - Port B Turn-Off Time
($V_{PA} = 4.2 \text{ V}$, $R_L = 10 \Omega$, $C_L = 0.1 \mu\text{F}$)

DEVICE PIN OUT

Device pin out is designed for ease of layout.

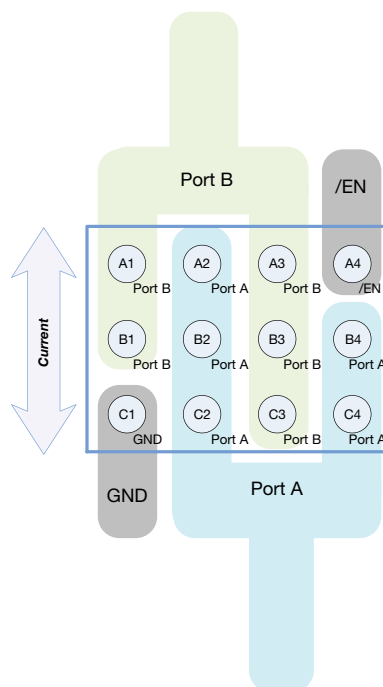


Fig. 20 - Proposed Layout

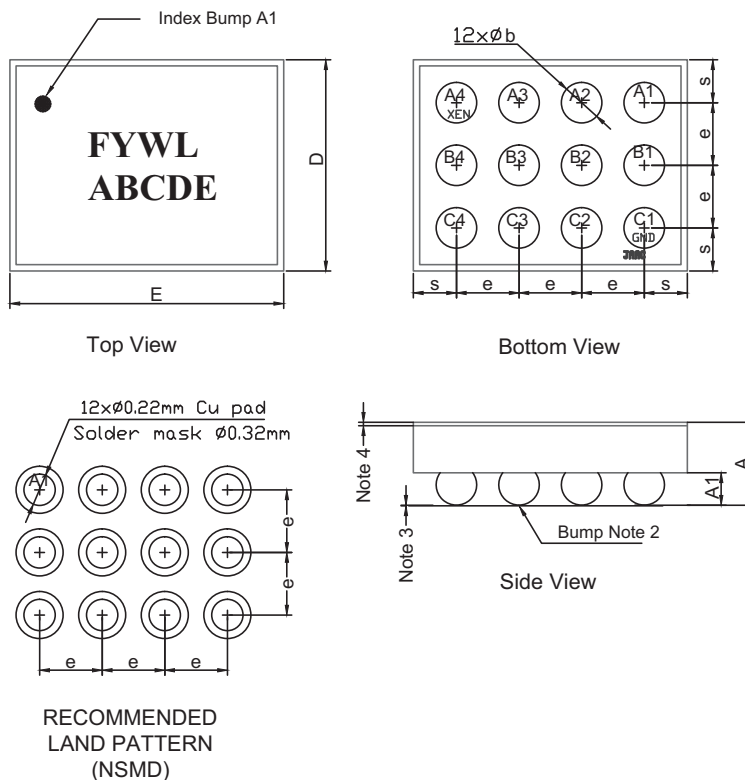


PRODUCT SUMMARY				
Part number	SiP32101	SiP32102	SiP32103	SiP32104
Description	2.3 V to 5.5 V, 6.5 mΩ, 7 A, bidirectional switch, EN active low with internal pull-down resistor	2.3 V to 5.5 V, 6.5 mΩ, 7 A, bidirectional switch, EN active high with internal pull-down resistor	2.3 V to 5.5 V, 6.5 mΩ, 7 A, bidirectional switch, EN active low with internal pull-up resistor	2.3 V to 5.5 V, 6.5 mΩ, 7 A, bidirectional switch, EN active low
Configuration	Single	Single	Single	Single
Slew rate time (μs)	1 000	1 000	1 000	1 000
On delay time (μs)	500	500	800	800
Input voltage min. (V)	2.3	2.3	2.3	2.3
Input voltage max. (V)	5.5	5.5	5.5	5.5
On-resistance at input voltage min. (mΩ)	8	8	8	8
On-resistance at input voltage max. (mΩ)	5.1	5.1	5.1	5.1
Quiescent current at input voltage min. (μA)	0.11	0.11	4	0.11
Quiescent current at input voltage max. (μA)	0.14	0.14	8.2	0.14
Output discharge (yes / no)	No	No	No	No
Reverse blocking (yes / no)	Yes	Yes	Yes	Yes
Continuous current (A)	7	7	7	7
Package type	WCSP12	WCSP12	WCSP12	WCSP12
Package size (W, L, H) (mm)	1.3 x 1.7 x 0.5	1.3 x 1.7 x 0.5	1.3 x 1.7 x 0.5	1.3 x 1.7 x 0.5
Status code	2	2	2	2
Product type	Slew rate, true bidirectional	Slew rate, true bidirectional	Slew rate, true bidirectional	Slew rate, true bidirectional
Applications	Computers, consumer, industrial, healthcare, portable	Computers, consumer, industrial, healthcare, portable	Computers, consumer, industrial, healthcare, portable	Computers, consumer, industrial, healthcare, portable

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WCSP12: 12 Bumps

(3 x 4, 0.4 mm pitch, 208 µm bump height, 1.71 mm x 1.31 mm die size)



DIMENSION	MILLIMETERS ⁽⁵⁾			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.515	0.530	0.545	0.0203	0.0209	0.0215
A1	0.183	0.208	0.233	0.0072	0.0082	0.0092
b	0.234	0.260	0.312	0.0092	0.0102	0.0123
e	0.400			0.0157		
s	0.235	0.255	0.275	0.0093	0.0100	0.0108
D	1.270	1.310	1.350	0.0500	0.0516	0.0531
E	1.670	1.710	1.750	0.0657	0.0673	0.0689

Notes (unless otherwise specified)

- (1) Laser mark on the silicon die back coated with an epoxy film.
- (2) Bumps are SAC396.
- (3) 0.050 max. co-planarity.
- (4) Laminate tape thickness is 0.022 mm.
- (5) Use millimeters as the primary measurement.

ECN: S13-2510-Rev. B, 16-Dec-13
DWG: 6017



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