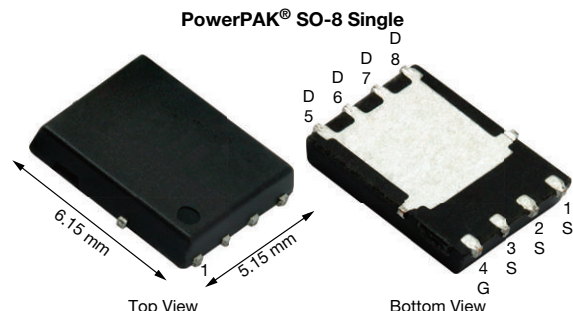


N-Channel 30 V (D-S) MOSFET



PRODUCT SUMMARY	
V_{DS} (V)	30
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.00122
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V	0.00195
Q_g typ. (nC)	20.8
I_D (A)	191 ^a
Configuration	Single

FEATURES

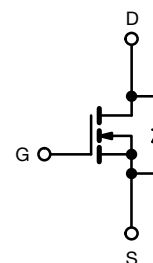
- TrenchFET® Gen IV power MOSFET
- 100 % R_g and UIS tested
- Excellent $R_{DS} - Q_g$ Figure-of-Merit (FOM) for switch-mode power supplies
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- High power density DC/DC
- Synchronous rectification
- Load switch
- OR-ing



N-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK® SO-8
Lead (Pb)-free, halogen-free, BLR and IOL	SiRA62DDP-T1-UE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	30	V
Gate-source voltage		V_{GS}	+20, -16	
Continuous drain current ($T_J = 150$ °C)	$T_C = 25$ °C	I_D	191	A
	$T_C = 70$ °C		153	
	$T_A = 25$ °C		51 ^{b, c}	
	$T_A = 70$ °C		40 ^{b, c}	
Pulsed drain current ($t = 100$ μ s)		I_{DM}	400	
Continuous source-drain diode current	$T_C = 25$ °C	I_S	65	
	$T_A = 25$ °C		4.6 ^{b, c}	
Single pulse avalanche current		I_{AS}	45	mJ
Single pulse avalanche energy		E_{AS}	102	
Maximum power dissipation	$T_C = 25$ °C	P_D	71	W
	$T_C = 70$ °C		46	
	$T_A = 25$ °C		5 ^{b, c}	
	$T_A = 70$ °C		3.2 ^{b, c}	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^{d, e}			260	

THERMAL RESISTANCE RATINGS					
PARAMETER		SMYBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^{b, f}	$t \leq 10$ s	R_{thJA}	20	25	°C/W
	Steady state	R_{thJC}	1.4	1.75	

Notes

- Based on $T_C = 25$ °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Reflow conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 70 °C/W



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	30	-	-	V
Drain-source breakdown voltage ^(c) (transient)	V _{DSt}	V _{GS} = 0 V, I _{D(aval)} = 70 A, t _{transcient} ≤ 50 ns	36	-	-	
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = 10 mA	-	20	-	mV/°C
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	-	-4.9	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1	-	2.2	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = +20, -16 V	-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C	-	-	10	
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 15 A	-	0.0010	0.00122	Ω
		V _{GS} = 4.5 V, I _D = 10 A	-	0.0018	0.00195	
Forward transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 40 A	-	135	-	S
Dynamic ^b						
Input capacitance	C _{iSS}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	-	4344	-	pF
Output capacitance	C _{oss}		-	1680	-	
Reverse transfer capacitance	C _{rSS}		-	67	-	
C _{rSS} /C _{iSS} ratio			-	0.0016	0.0032	
Total gate charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 10 A	-	46.3	70	nC
		V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 10 A	-	20.8	32	
Gate-source charge	Q _{gs}		-	11.4	-	
Gate-drain charge	Q _{gd}		-	2.4	-	
Output charge	Q _{oss}	V _{DS} = 15 V, V _{GS} = 0 V	-	50	-	
Gate resistance	R _g	f = 1 MHz	0.24	1.2	2.4	Ω
Turn-on delay time	t _{d(on)}	V _{DD} = 15 V, R _L = 1.5 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω	-	15	30	ns
Rise time	t _r		-	5	10	
Turn-off delay time	t _{d(off)}		-	30	60	
Fall time	t _f		-	5	10	
Turn-on delay time	t _{d(on)}	V _{DD} = 15 V, R _L = 1.5 Ω I _D ≅ 10 A, V _{GEN} = 4.5 V, R _g = 1 Ω	-	30	60	
Rise time	t _r		-	60	120	
Turn-off delay time	t _{d(off)}		-	30	60	
Fall time	t _f		-	10	20	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	65	A
Pulse diode forward current ^a	I _{SM}		-	-	400	
Body diode voltage	V _{SD}	I _S = 10 A	-	0.75	1.1	V
Body diode reverse recovery time	t _{rr}	I _F = 10 A, di/dt = 100 A/μs, T _J = 25 °C	-	45	90	ns
Body diode reverse recovery charge	Q _{rr}		-	45	90	nC
Reverse recovery fall time	t _a		-	24.5	-	ns
Reverse recovery rise time	t _b		-	20.5	-	

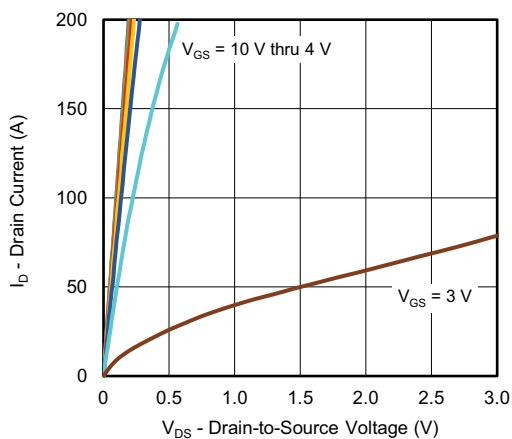
Notes

- a. Pulse test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing
c. Based on characterization, not subject to production testing

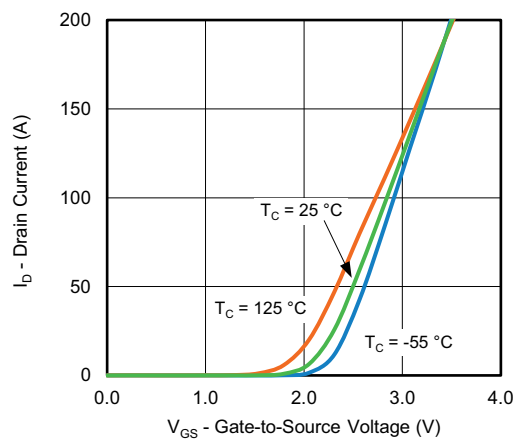
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



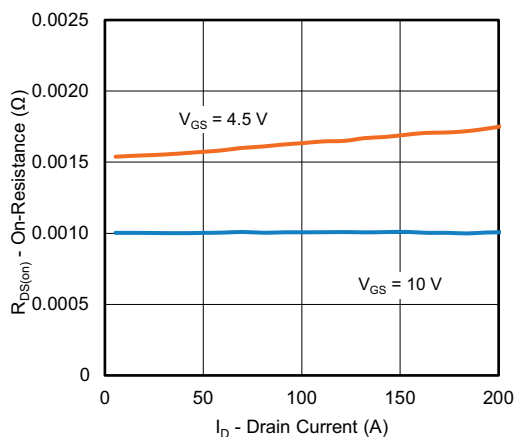
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



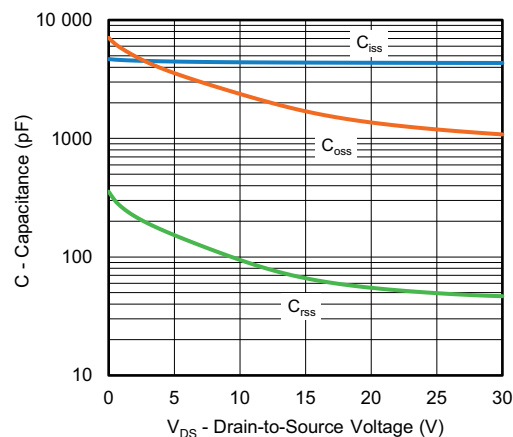
Output Characteristics



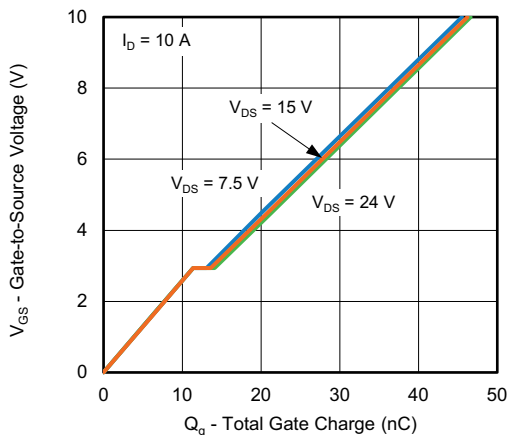
Transfer Characteristics



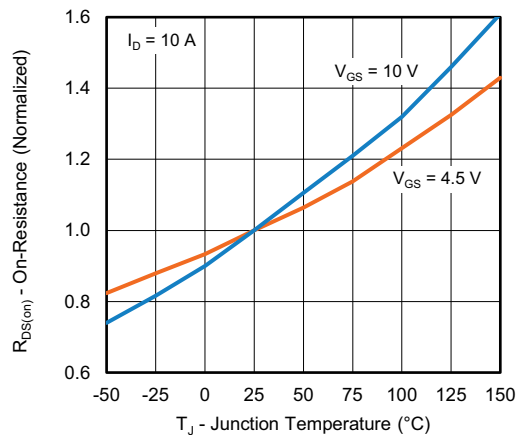
On-Resistance vs. Drain Current



Capacitance



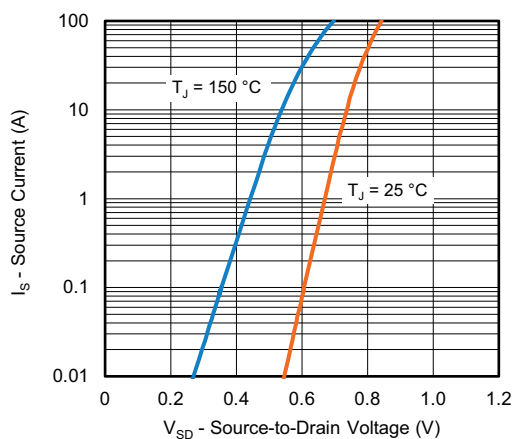
Gate Charge



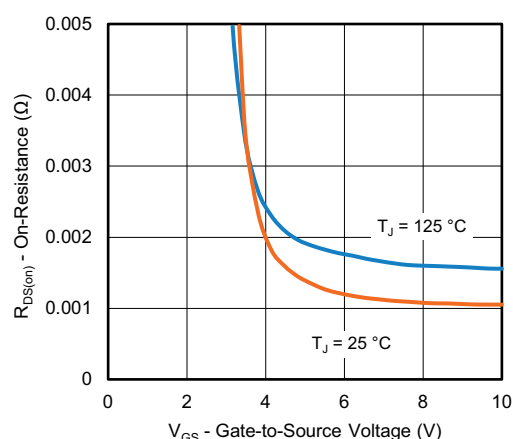
On-Resistance vs. Junction Temperature



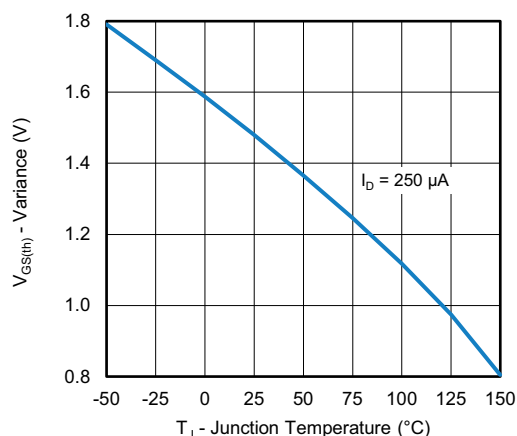
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



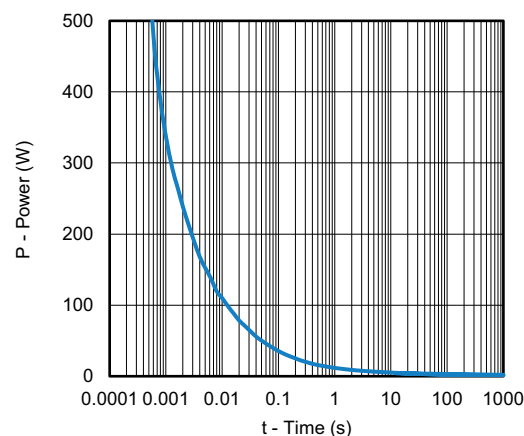
Source-Drain Diode Forward Voltage



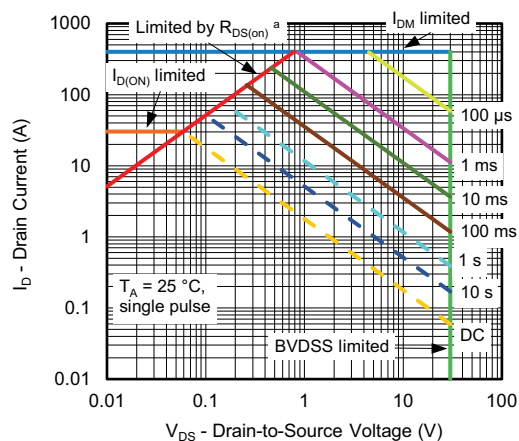
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient



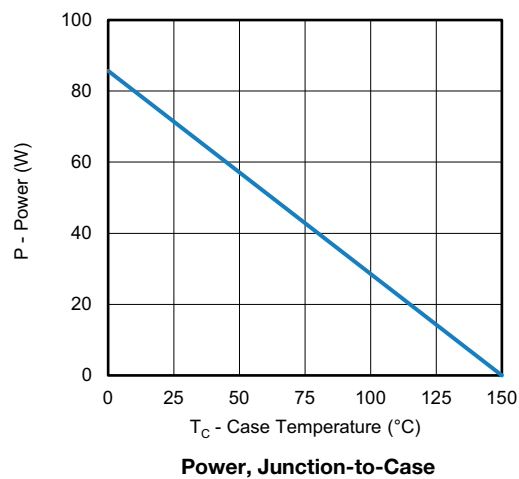
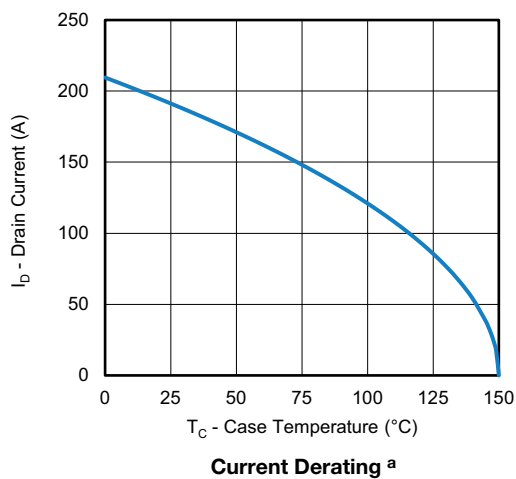
Safe Operating Area

Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

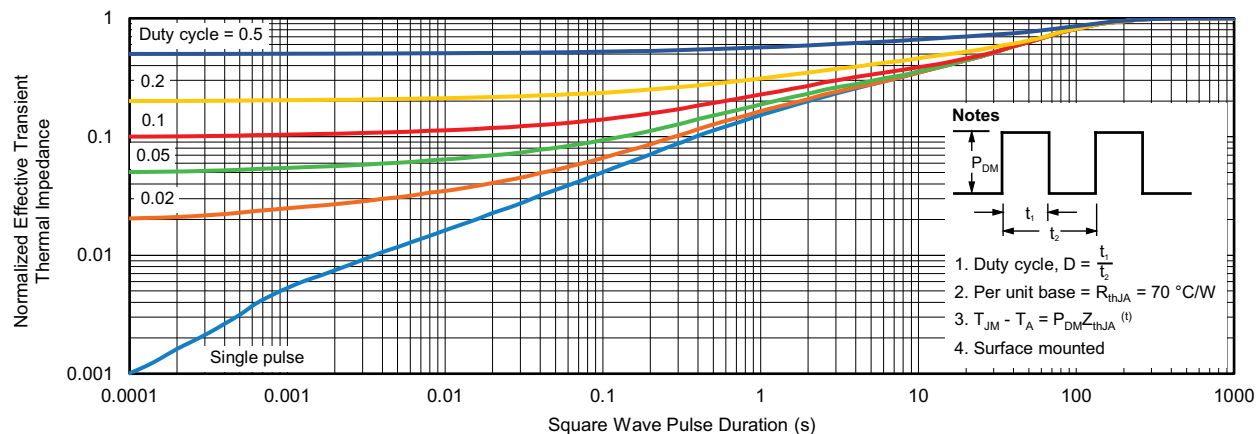


Note

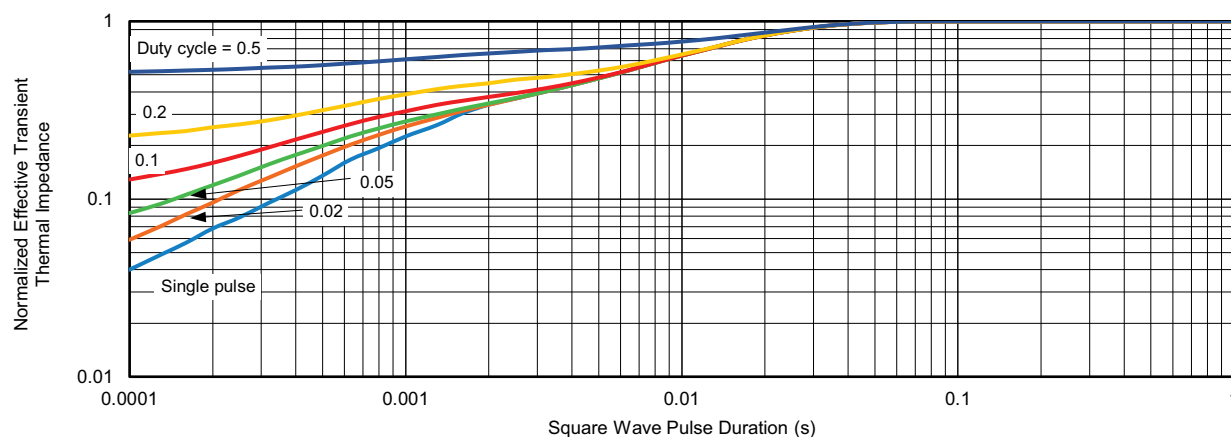
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62491.

PowerPAK® SO-8, (Single/Dual)



Notes

1. Inch will govern.
2. Dimensions exclusive of mold gate burrs.
3. Dimensions exclusive of mold flash and cutting burrs.

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1		-	0.05	0	-	0.002
b	0.33	0.41	0.51	0.013	0.016	0.020
c	0.23	0.28	0.33	0.009	0.011	0.013
D	5.05	5.15	5.26	0.199	0.203	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.56	3.76	3.91	0.140	0.148	0.154
D3	1.32	1.50	1.68	0.052	0.059	0.066
D4	0.57 typ.			0.0225 typ.		
D5	3.98 typ.			0.157 typ.		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	5.79	5.89	5.99	0.228	0.232	0.236
E2	3.48	3.66	3.84	0.137	0.144	0.151
E3	3.68	3.78	3.91	0.145	0.149	0.154
E4	0.75 typ.			0.030 typ.		
e	1.27 BSC			0.050 BSC		
K	1.27 typ.			0.050 typ.		
K1	0.56	-	-	0.022	-	-
H	0.51	0.61	0.71	0.020	0.024	0.028
L	0.51	0.61	0.71	0.020	0.024	0.028
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 typ.			0.005 typ.		
ECN: S17-0173-Rev. L, 13-Feb-17						
DWG: 5881						

RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single



Recommended Minimum Pads
Dimensions in Inches/(mm)

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