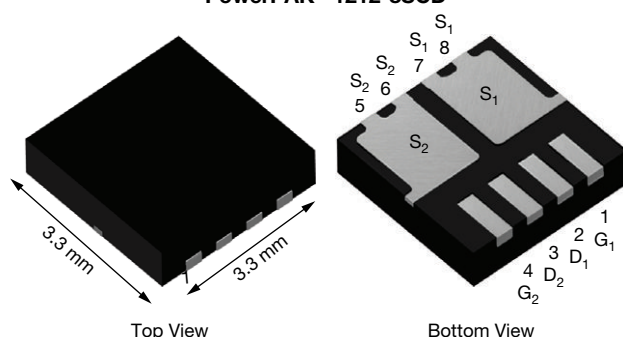


Common Drain Dual N-Channel 30 V (S1-S2) MOSFET

PowerPAK® 1212-8SCD


PRODUCT SUMMARY	
V _{S1S2} (V)	30
R _{S1S2(on)} max. (Ω) at V _{GS} = 10 V	0.00450
R _{S1S2(on)} max. (Ω) at V _{GS} = 4.5 V	0.00695
Q _g typ. (nC) ^g	14
I _{S1S2} (A) ^a	101
Configuration	Common drain

ORDERING INFORMATION

Package	PowerPAK 1212-8SCD
Lead (Pb)-free and halogen-free	SiSF06DN-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V _{S1S2}	30	V
Gate-source voltage	V _{GS}	+20 / -16	
Continuous drain current (T _J = 150 °C)	I _{S1S2}	101	A
		81	
		28 ^{b, c}	
		22 ^{b, c}	
Pulsed drain current (t = 100 μs)	I _{S1S2M}	190	
Maximum power dissipation	P _D	69.4	W
		44.4	
		5.2 ^{b, c}	
		3.3 ^{b, c}	
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^c		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^b	R _{thJA}	19	24	°C/W
Maximum junction-to-case (drain)	R _{thJC}	1.4	1.8	

Notes

- T_C = 25 °C
- Surface mounted on 1" x 1" FR4 board
- t = 10 s
- See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8SCD is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 63 °C/W
- Single MOSFET

FEATURES

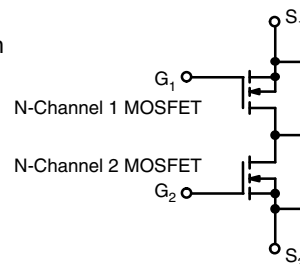
- TrenchFET® Gen IV power MOSFET
- Very low source-to-source on resistance
- Integrated common-drain n-channel MOSFETs in a compact and thermally enhanced package
- 100 % R_g and UIS tested
- Optimizes circuit layout for bi-directional current flow
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Battery protection switch
- Bi-directional switch
- Load switch





SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	30	-	-	V
Gate-source threshold voltage	V _{GS(th)}	V _{S1S2} = V _{GS} , I _D = 250 μA	1	-	2.3	
Gate-source leakage	I _{GSS}	V _{S1S2} = 0 V, V _{GS} = +20 V / -16 V	-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{S1S2} = 30 V, V _{GS} = 0 V	-	-	1	μA
		V _{S1S2} = 30 V, V _{GS} = 0 V, T _J = 70 °C	-	-	15	
On-state drain current ^a	I _{S1S2(on)}	V _{S1S2} ≥ 10 V, V _{GS} = 10 V	20	-	-	A
Drain-source on-state resistance ^a	R _{S1S2(on)}	V _{GS} = 10 V, I _{S1S2} = 7 A	-	0.00344	0.00450	Ω
		V _{GS} = 4.5 V, I _{S1S2} = 5 A	-	0.00536	0.00695	
Forward transconductance ^a	g _{fs}	V _{S1S2} = 10 V, I _{S1S2} = 35 A	-	115	-	S
Dynamic ^{b, c}						
Input capacitance	C _{iss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	-	2050	-	pF
Output capacitance	C _{oss}		-	855	-	
Reverse transfer capacitance	C _{rss}		-	40	-	
Total gate charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D =5 A	-	30	45	nC
Gate-source charge	Q _{gs}	V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 5 A	-	14	21	
Gate-drain charge	Q _{gd}		-	2.8	-	
Gate resistance	R _g	f = 1 MHz	0.2	1.1	2.2	
Turn-on delay time	t _{d(on)}	V _{DD} = 15 V, R _L = 3 Ω, I _{S1S2} ≅ 5 A, V _{GEN} = 10 V, R _g = 1 Ω	-	18	36	ns
Rise time	t _r		-	10	20	
Turn-off delay time	t _{d(off)}		-	35	70	
Fall time	t _f		-	10	20	
Turn-on delay time	t _{d(on)}	V _{DD} = 15 V, R _L = 3 Ω, I _D ≅ 5 A, V _{GEN} = 4.5 V, R _g = 1 Ω	-	30	60	
Rise time	t _r		-	60	120	
Turn-off delay time	t _{d(off)}		-	35	70	
Fall time	t _f		-	20	40	
Drain-Source Body Diode Characteristics ^c						
Continuous source-drain diode current	I _{S1S2}	T _C = 25 °C	-	-	60	A
Pulse diode forward current	I _{S1S2M}		-	-	190	
Body diode reverse recovery time	t _{rr}	I _F = 5 A, di/dt = 100 A/μs, T _J = 25 °C	-	34	51	ns
Body diode reverse recovery charge	Q _{rr}		-	25	50	nC
Reverse recovery fall time	t _a		-	17	-	ns
Reverse recovery rise time	t _b		-	17	-	

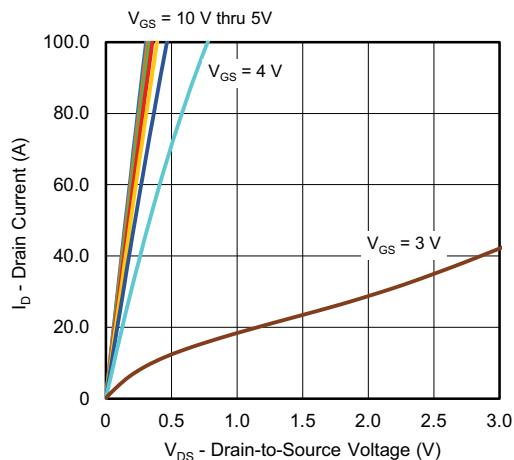
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing
c. On single MOSFET

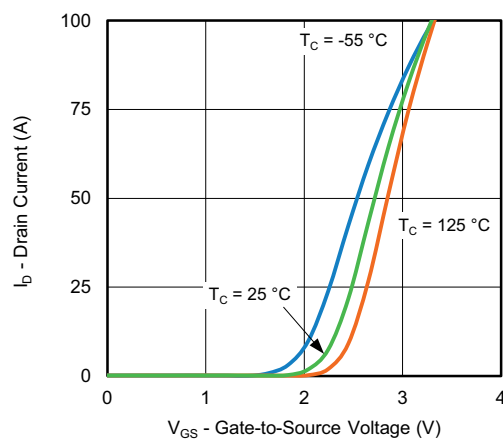
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



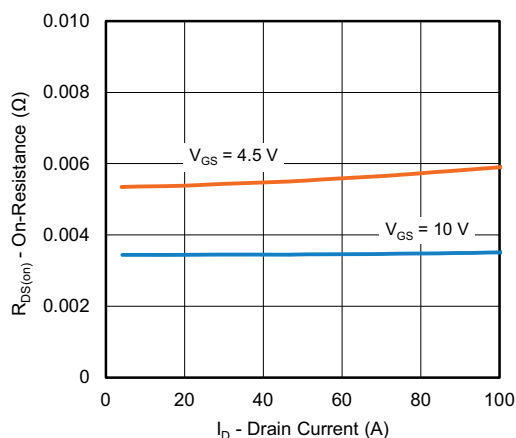
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



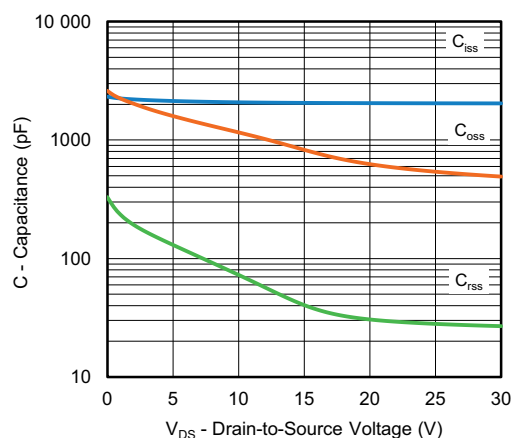
Output Characteristics



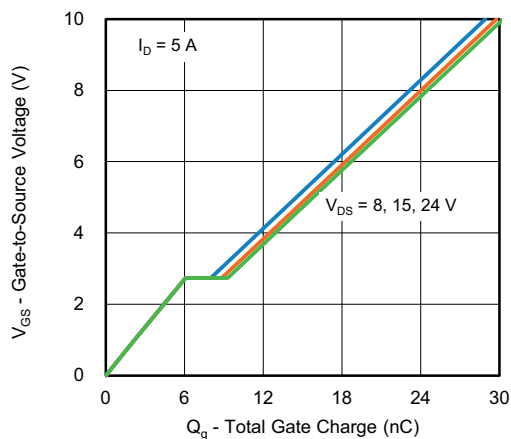
Transfer Characteristics



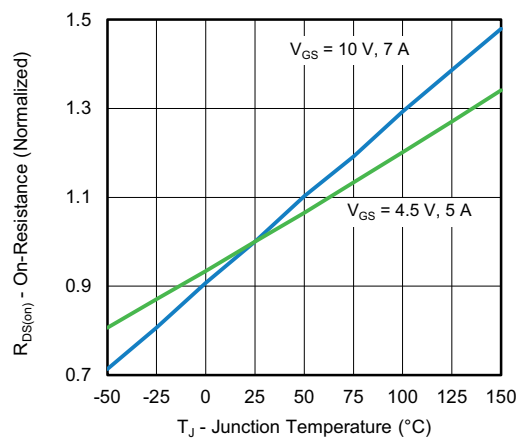
On-Resistance vs. Source Current and Gate Voltage



Capacitance



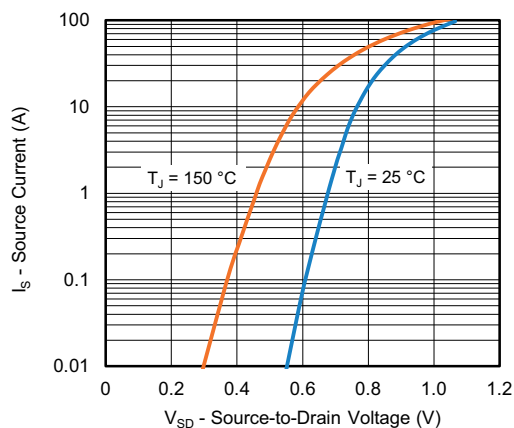
Gate Charge



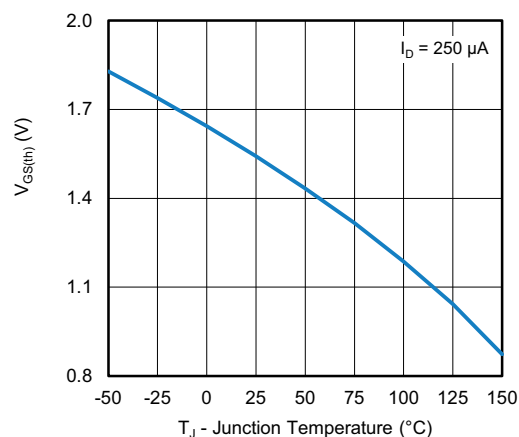
On-Resistance vs. Junction Temperature



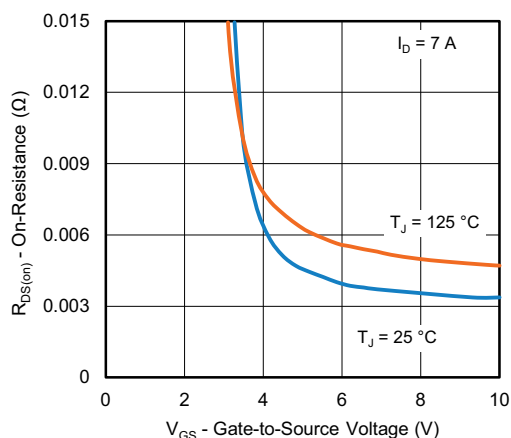
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



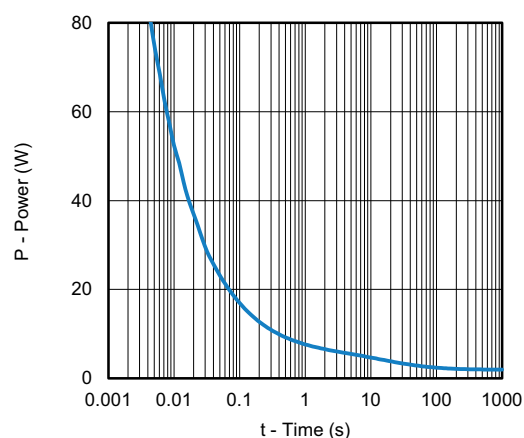
Source-Drain Diode Forward Voltage



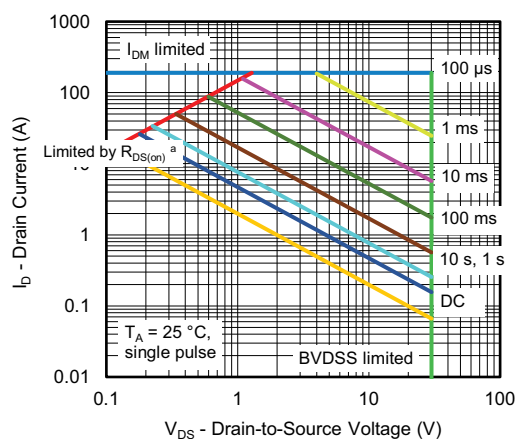
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



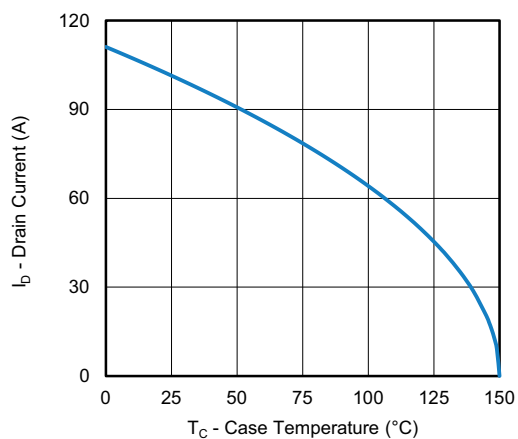
Safe Operating Area, Junction-to-Ambient

Notes

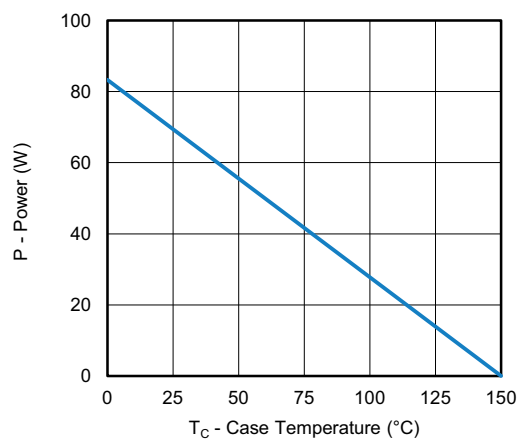
- a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



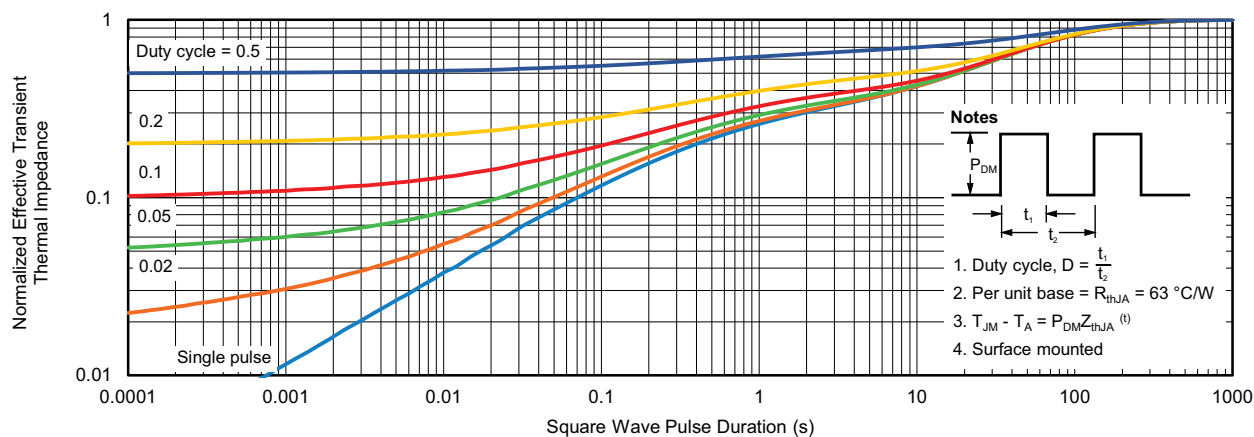
Power, Junction-to-Case

Notes

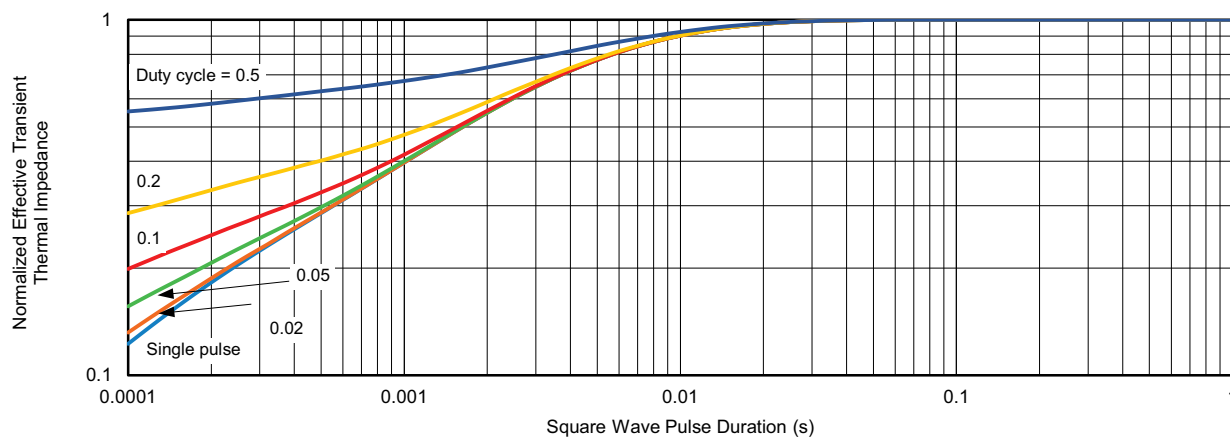
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

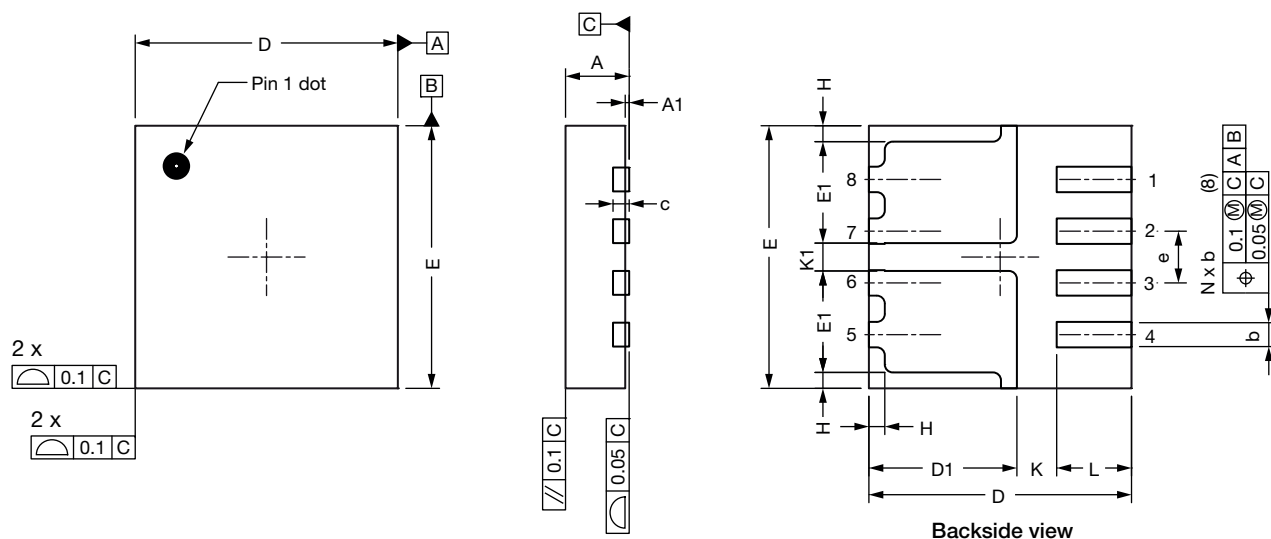


Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?77407.

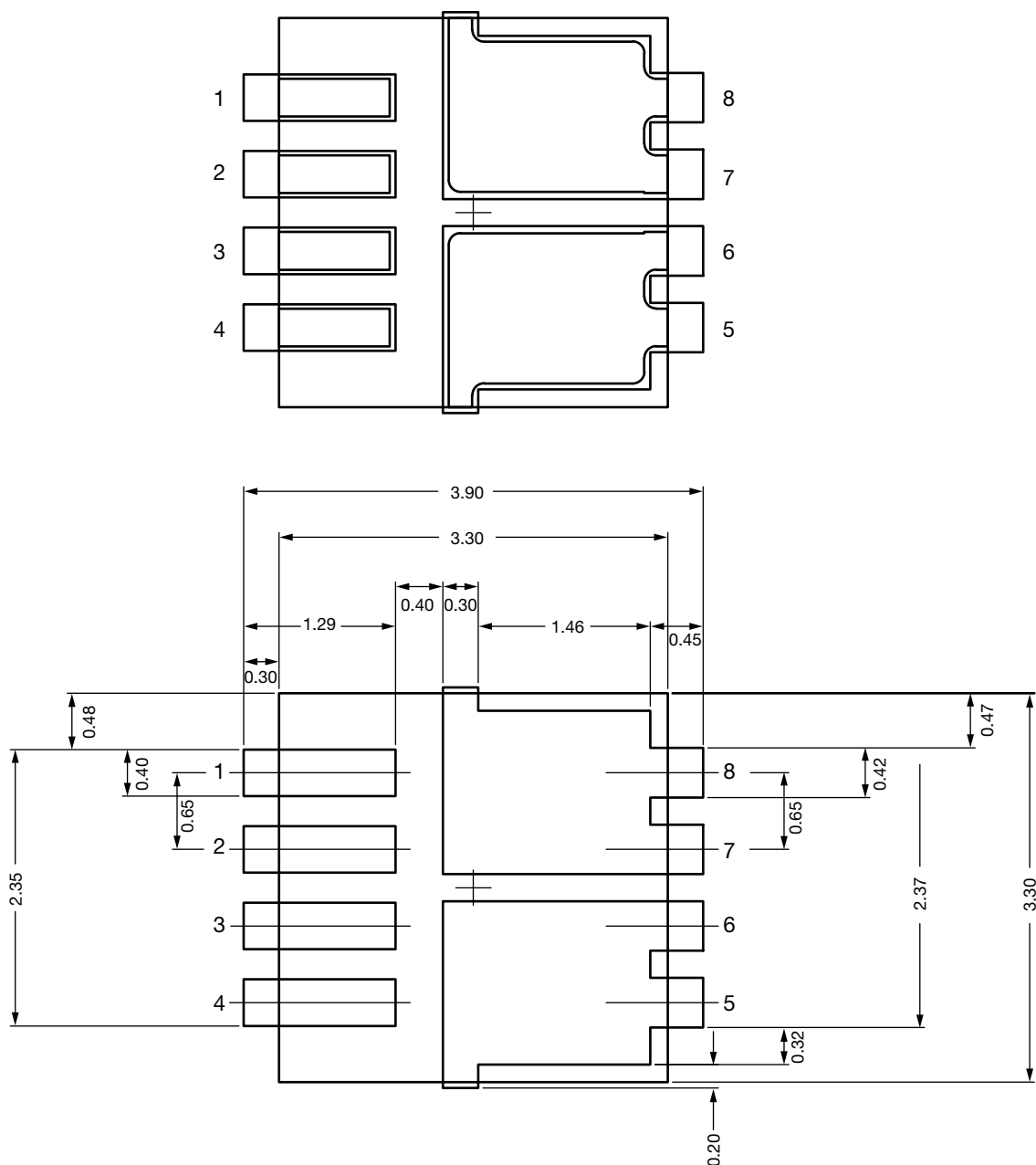

PowerPAK® 1212-8S CD with Flip Chip


DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.027	0.029	0.031
A1	0	0.02	0.05	0	0.001	0.002
b	0.27	0.32	0.37	0.011	0.013	0.015
c	-	0.20 ref.	-	-	0.008 ref.	-
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	1.76	1.86	1.96	0.069	0.073	0.077
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	1.18	1.28	1.38	0.046	0.050	0.054
e	0.60	0.65	0.70	0.024	0.026	0.028
K	0.50 typ.			0.020 typ.		
K1	0.35 typ.			0.014 typ.		
H	0.10	0.20	0.30	0.006	0.008	0.010
L	0.84	0.94	1.04	0.033	0.037	0.041

ECN: C17-1732-Rev. A, 18-Dec-17

DWG: 6061

Recommended Land Pattern





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