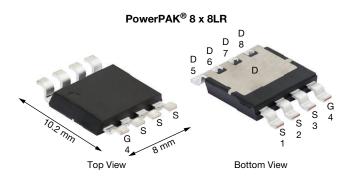


Vishay Siliconix

Automotive N-Channel 40 V (D-S) 175 °C MOSFET

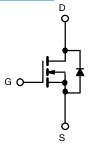


| PRODUCT SUMMARY | | | | |
|--|--------|--|--|--|
| V _{DS} (V) | 40 | | | |
| $R_{DS(on)}$ (Ω) at $V_{GS} = 10 \text{ V}$ | 0.0015 | | | |
| I _D (A) | 372 | | | |
| Configuration | Single | | | |

FEATURES

- TrenchFET® Gen IV power MOSFET
- AEC-Q101 qualified
- 100 % R_a and UIS tested
- Thin 1.6 mm package
- · Very low thermal resistance
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>





N-Channel MOSFET

| ORDERING INFORMATION | |
|---------------------------------|---|
| Package | PowerPAK 8 x 8LR |
| Lead (Pb)-free and halogen-free | SQJQ148ER (for detailed order number please see www.vishay.com/doc?79776) |

| ABSOLUTE MAXIMUM RATING | S (T _C = 25 °C, unles | s otherwise noted | l) | | |
|---|----------------------------------|-----------------------------------|-------------|----|--|
| PARAMETER | SYMBOL | LIMIT | UNIT | | |
| Drain-source voltage | | V_{DS} | 40 | V | |
| Gate-source voltage | | V_{GS} | ± 20 | V | |
| Continuous drain current | T _C = 25 °C | - I _D | 372 | | |
| | T _C = 125 °C | | 214 | | |
| Continuous source current (diode conduction) | | I _S | 360 | Α | |
| Pulsed drain current ^b | | I _{DM} | 670 | | |
| Single pulse avalanche current | L = 0.1 mH | I _{AS} | 46 | | |
| Single pulse avalanche energy | L = 0.1 IIII | E _{AS} | 105 | mJ | |
| Maximum power dissipation | T _C = 25 °C | D | 394 | W | |
| | T _C = 125 °C | P _D | 131 | VV | |
| Operating junction and storage temperature range | | T _J , T _{stg} | -55 to +175 | °C | |
| Soldering recommendations (peak temperature) ^d | | | 260 | | |

| THERMAL RESISTANCE RATINGS | | | | | |
|----------------------------|------------|------------|-------|------|--|
| PARAMETER | | SYMBOL | LIMIT | UNIT | |
| Junction-to-ambient P | CB mount c | R_{thJA} | 44 | °C/W | |
| Junction-to-case (drain) | | R_{thJC} | 0.38 | | |

Notes

- a. Package limited
- b. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %
- c. When mounted on 1" square PCB (FR4 material)
- d. See solder profile (www.vishay.com/doc?73257). The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection



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| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|----------------------------|---|---|------|---------|--------|------|
| Static | | | | | • | | |
| Drain-source breakdown voltage | V _{DS} | $V_{GS} = 0, I_D = 250 \mu A$ | | 40 | - | - | - V |
| Gate-source threshold voltage | V _{GS(th)} | $V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$ | | 2 | 3 | 3.5 | |
| Gate-source leakage | I _{GSS} | $V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$ | | - | - | ± 100 | nA |
| Zero gate voltage drain current | | $V_{GS} = 0 V$ | V _{DS} = 40 V | - | - | 1 | |
| | I _{DSS} | $V_{GS} = 0 V$ | V _{DS} = 40 V, T _J = 125 °C | - | - | 50 | μA |
| | | V _{GS} = 0 V | V _{DS} = 40 V, T _J = 175 °C | - | - | 200 | |
| On-state drain current ^a | I _{D(on)} | V _{GS} = 10 V | $V_{DS} \ge 5 \text{ V}$ | 100 | - | =. | Α |
| Drain-source on-state resistance ^a | | V _{GS} = 10 V | I _D = 20 A | - | 0.00125 | 0.0015 | Ω |
| | R _{DS(on)} | V _{GS} = 10 V | I _D = 20 A, T _J = 125 °C | - | - | 0.0025 | |
| | | V _{GS} = 10 V | I _D = 20 A, T _J = 175 °C | - | - | 0.0031 | |
| Forward transconductance b | 9 _{fs} | V _{DS} = 15 V, I _D = 60 A | | - | 120 | =. | S |
| Dynamic ^b | | | | | | | |
| Input capacitance | C _{iss} | V _{GS} = 0 V | V _{GS} = 0 V V _{DS} = 25 V, f = 1 MHz | - | 4170 | 5750 | pF |
| Output capacitance | C _{oss} | | | - | 1566 | 2193 | |
| Reverse transfer capacitance | C _{rss} |] | | - | 131 | 184 | |
| Total gate charge ^c | Qg | | 0 V V _{DS} = 20 V, I _D = 20 A | - | 68 | 102 | nC |
| Gate-source charge c | Q _{gs} | $V_{GS} = 10 \text{ V}$ | | - | 20 | - | |
| Gate-drain charge ^c | Q _{gd} | | | - | 15 | - | 1 |
| Gate resistance | R_g | f = 1 MHz | | 0.8 | 1.6 | 2.4 | Ω |
| Turn-on delay time ^c | t _{d(on)} | $V_{DD} = 20 \text{ V, } R_L = 1 \Omega$ $I_D \cong 20 \text{ A, } V_{GEN} = 10 \text{ V, } R_g = 1 \Omega$ | | - | 17 | 26 | |
| Rise time ^c | t _r | | | - | 88 | 132 | ns |
| Turn-off delay time ^c | t _{d(off)} | | | - | 30 | 45 | |
| Fall time ^c | t _f | | | - | 12 | 18 | |
| Source-Drain Diode Ratings and Cha | aracteristics ^b | | | | | | |
| Reverse recovery time | t _{rr} | V _{DD} = 32 V, I _{FM} = 15 A, di/dt = 100 A/μs | | - | 47 | 94 | ns |
| Reverse recovery charge | Q _{rr} | | | - | 47 | 94 | nC |
| Reverse recovery current | I _{RM} | | | - | - | 1.8 | Α |
| Pulsed current ^a | I _{SM} | | | - | - | 1600 | Α |
| Forward voltage | V _{SD} | $I_F = 50 \text{ A}, V_{GS} = 0$ | | - | 0.8 | 1.1 | V |

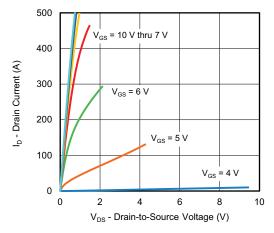
Notes

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

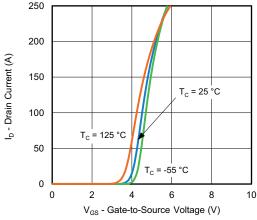
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



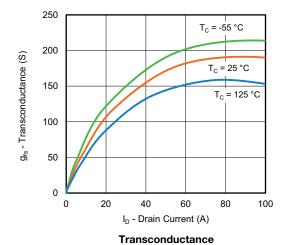
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)

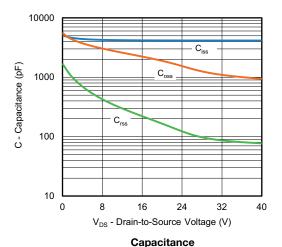


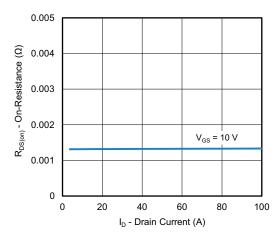
Output Characteristics



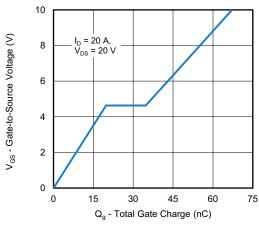
Transfer Characteristics





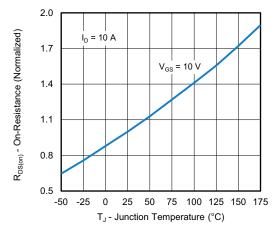


On-Resistance vs. Drain Current

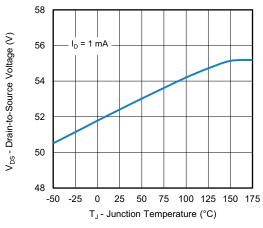




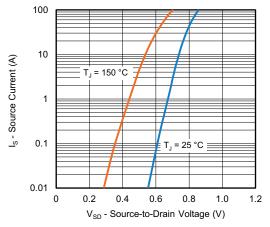
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



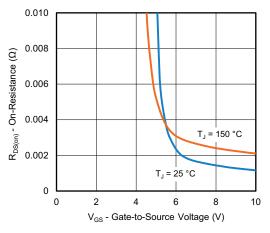
On-Resistance vs. Junction Temperature



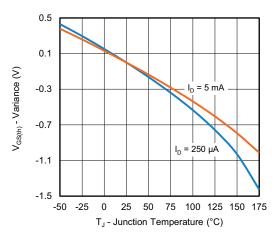
Drain Source Breakdown vs. Junction Temperature



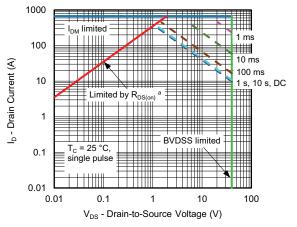
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Safe Operating Area

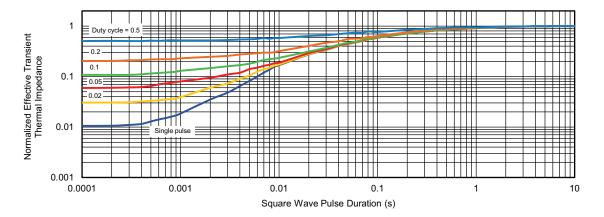
Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

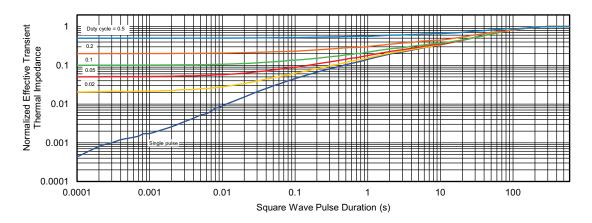
For technical questions, contact: automostech



THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

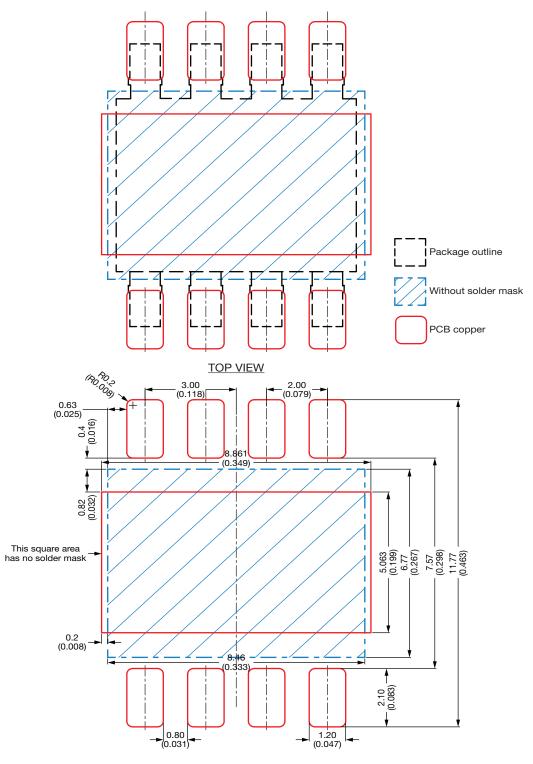


Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?66839.



Recommended Land Pattern PowerPAK® 8 x 8LR



Notes

- This land pattern is for reference
- Proposed stencil thickness 200 µm All dimensions are in millimeter (inches)

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DWG: 3002

Revision: 17-Apr-2023

Document Number: 63166



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