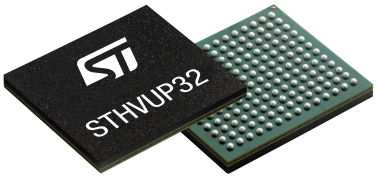
STHVUP32

Databrief

32-channel ±100 V, ±0.8/0.4 A, 3/5-level RTZ, T/R switch, high-speed ultrasound pulser with integrated transmit beamformer



Product status link
STHVUP32

Product summary	
Order code	STHVUP32
Package	FCBGA168 11.5x10.5x1.35
Packing	Tray

Product label
SUSTAINABLE TECHNOLOGY

Features

- Pulsed wave (PW) and continuous wave (CW) mode operations:
  - 3- or 5-level ±100 V output waveform
  - Programmable ±200 mA or ±400 mA or ±600 mA or ±800 mA source and sink current in 3-level configuration (±400 mA or ±200 mA in 5-level configuration)
- Fully integrated 23 Ω resistance real clamping-to-ground function
- Fully integrated 23 Ω resistance transmitting/receiving switches (TR_SW)
  - Compliant with receiver multiplexing function
- Auxiliary integrated circuits
  - Noise-blocking diodes
  - Thermal protection
  - Undervoltage protection and bias supply checks
- Programmable power management to optimize the performances for ultra-portable applications
- Beamforming in transmission mode
  - Programmable single-channel delay for beam steering and focusing
  - Clock frequency up to 200 MHz
  - 5 ns delay resolution
  - From 5 ns to 20 us delay range @ 200 MHz
  - 3 us minimum delay table writing time
- Embedded memory to store transmission patterns
  - 32 states for waveform definition, with waveform compression algorithm
  - Up to 4 different waveforms for each channel
- Easy driving control
  - Control through standard Quad Serial Peripheral Interface (QSPI)
  - Few input signals to drive several devices
  - Single interrupt as alert signal
  - Single trigger to manage transmitting (TX) and receiving (RX) phases, fully automatic and programmable
  - Anti-glitch on TRIGGER signal during TX phase
- Checksum control
- Very low package thermal resistance
- Latch-up free due to HV SOI technology
- Just a few passive components needed
- Small package: BGA 11.5 mm x 10.5 mm x 1.35 mm with 168 balls and 0.8 mm pitch

Application

- Medical ultrasound imaging
- Pulse waveform generators
- Ultra-portable ultrasound imaging
- Piezoelectric transducer drivers

Description

The STHVUP32 is a 32 channels monolithic high-voltage and high-speed pulser with an integrated beam-former. It is specifically designed for pulse generation in multi-channel low power ultra-portable medical ultrasound applications.

The waveforms generated by STHVUP32 are described with sequences of up to 32 states stored in the device memory. With each state it is possible to configure each individual output channel to be connected to high voltage supplies (positive or negative), clamped to ground or left in high impedance.

A pure analog section provides each channel four half-bridges (four high-voltage P-channel and four high-voltage N-channel MOSFETs), a clamping-to-ground circuit and a transmitting/receiving switch structure which guarantees an effective isolation during the transmission phase. Each channel features also integrated high-voltage level translators and noise-blocking diodes.

Through a dedicated bit, channels can be programmed as a 3-level output or as a 5-level output. In 3-level mode, the four half-bridges are driven in parallel to provide a default peak current of 800 mA. However, it is also possible to program a low-consumption and low output current modes to decrease the overall power consumption: in this case, it is possible to use only one, two or three half-bridges, therefore the peak current can be reduced to 200, 400 or 600 mA respectively. In 5-level mode, the four half-bridges can be driven independently, and each half-bridge has a current capability of 200 mA. The clamp circuit, used to force the XDCR<31:0> output pins down to ground, has a resistance of 23 Ω and a peak current capability of 0.64 A. The 32 independent T/R switches can be used in a multiplexing configuration.

The STHVUP32 also includes some global blocks: thermal protection circuits, undervoltage checks on VDDP3V3, VDDM3V3 and DVDD, a power-on-reset (POR) on DVDD and a global self-biased supply for the drivers of the high-voltage MOSFET.

All functions are managed by a digital core working at a maximum clock frequency of 200 MHz. This block manages the delay profiles used in the beamformer, the waveform generation and the various global settings and grants that all the device operations are performed in the correct sequence.

Revision history

Table 1. **Document revision history**

Date	Version	Changes
04-Aug-2022	1	Initial release.
03-Feb-2023	2	Updated Features and title.
14-Mar-2023	3	Update the number of balls and pitch in the Features chapter.

Contents

Revision history 3