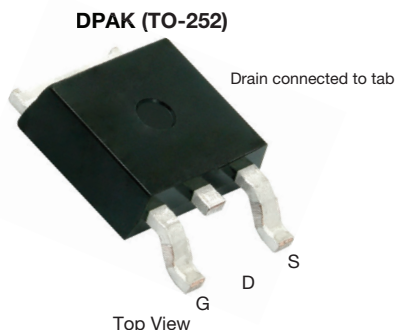
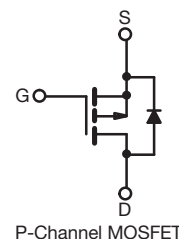


P-Channel 100 V (D-S) 175 °C MOSFET



FEATURES

- TrenchFET® Power MOSFET
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT


P-Channel MOSFET

PRODUCT SUMMARY

V_{DS} (V)	-100
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -10$ V	0.043
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -4.5$ V	0.048
Q_g typ. (nC)	54
I_D (A) ^a	-37
Configuration	Single

ORDERING INFORMATION

Package	DPAK (TO-252)
Lead (Pb)-free and halogen-free	SUD50P10-43L-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	-100	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current ($T_J = 175$ °C) ^b	I_D	$T_C = 25$ °C	-37.1 ^a
		$T_C = 125$ °C	-31 ^a
		$T_A = 25$ °C	-9.2 ^{b, c}
		$T_A = 125$ °C	-7.7 ^{b, c}
Pulsed drain current	I_{DM}	-40	A
Continuous source current (diode conduction)	I_S	$T_C = 25$ °C	-50 ^a
		$T_A = 25$ °C	-6.9 ^{b, c}
Avalanche current	I_{AS}	-35	
Single pulse avalanche energy	E_{AS}	61	mJ
Maximum power dissipation	P_D	$T_C = 25$ °C	136
		$T_C = 70$ °C	95
		$T_A = 25$ °C	8.3 ^{b, c}
		$T_A = 70$ °C	5.8 ^{b, c}
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +175	°C

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-ambient ^a	R_{thJA}	15	18	°C/W
		40	50	
Junction-to-case (drain)	R_{thJC}	0.85	1.1	

Note

- Package limited
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- Maximum under steady state conditions is 40 °C/W



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = -250 μA	-100	-	-	V	
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = -250 μA		-109	-	mV/°C	
V _{GS} (th) temperature coefficient	ΔV _{GS} (th)/T _J		-	5.9	-		
Gate-source threshold voltage	V _{GS} (th)	V _{DS} = V _{GS} , I _D = -250 μA	-1	-	- 3	V	
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	-	-	± 100	nA	
Zero gate voltage drain current	I _{DSS}	V _{DS} = -100 V, V _{GS} = 0 V	-	-	-1	μA	
		V _{DS} = -100 V, V _{GS} = 0 V, T _J = 55 °C	-	-	-10		
On-state drain current ^a	I _D (on)	V _{DS} ≥ 5 V, V _{GS} = -10 V	-40	-	-	A	
Drain-source on-state resistance ^a	R _{DS} (on)	V _{GS} = -10 V, I _D = -9.2 A	-	0.036	0.043	Ω	
		V _{GS} = -4.5 V, I _D = -7.7 A	-	0.040	0.048		
Forward transconductance ^a	g _{fs}	V _{DS} = -15 V, I _D = -9.2 A	-	38	-	S	
Dynamic ^b							
Input capacitance	C _{iss}	V _{DS} = -50 V, V _{GS} = 0 V, f = 1 MHz	-	4600	-	pF	
Output capacitance	C _{oss}		-	230	-		
Reverse transfer capacitance	C _{rss}		-	175	-		
Total gate charge	Q _g	V _{DS} = -50 V, V _{GS} = -10 V, I _D = -9.2 A	-	106	160	nC	
Gate-source charge	Q _{gs}	V _{DS} = -50 V, V _{GS} = -4.5 V, I _D = -9.2 A	-	54	81		
Gate-drain charge	Q _{gd}		-	14	-		
Gate resistance	R _g		-	26	-		
Turn-on delay time	t _d (on)	f = 1 MHz	-	4	-	Ω	
Rise time	t _r		V _{DD} = -50 V, R _L = 6.5 Ω I _D ≅ -7.7 A, V _{GEN} = - 10 V, R _g = 1 Ω	-	15	25	ns
Turn-off delay time	t _d (off)			-	20	30	
Fall time	t _f			-	110	165	
Turn-on delay time	t _d (on)	V _{DD} = -50 V, R _L = 6.5 Ω I _D ≅ -7.7 A, V _{GEN} = -4.5 V, R _g = 1 Ω		-	100	150	
Rise time	t _r		-	42	65		
Turn-off delay time	t _d (off)		-	160	240		
Fall time	t _f		-	100	150		
Drain-source body diode characteristics							
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	-50	A	
Pulse diode forward current ^a	I _{SM}		-	-	-40		
Body diode voltage	V _{SD}	I _S = - 7.7 A	-	-0.8	-1.2	V	
Body diode reverse recovery time	t _{rr}	I _F = -7.7 A, dI/dt = 100 A/μs, T _J = 25 °C	-	60	90	ns	
Body diode reverse recovery charge	Q _{rr}		-	150	225	nC	
Reverse recovery fall time	t _a		-	46	-	ns	
Reverse recovery rise time	t _b		-	14	-		

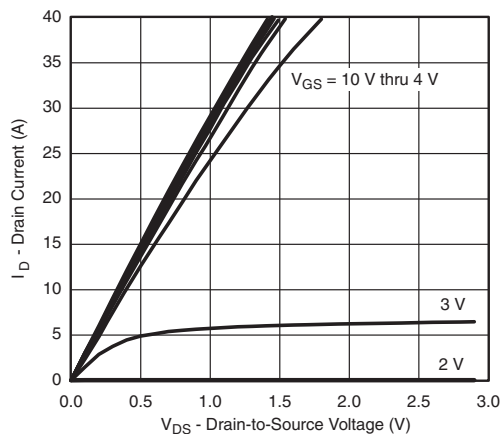
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing

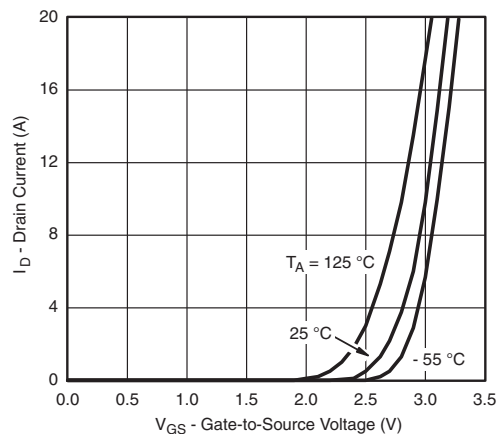
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



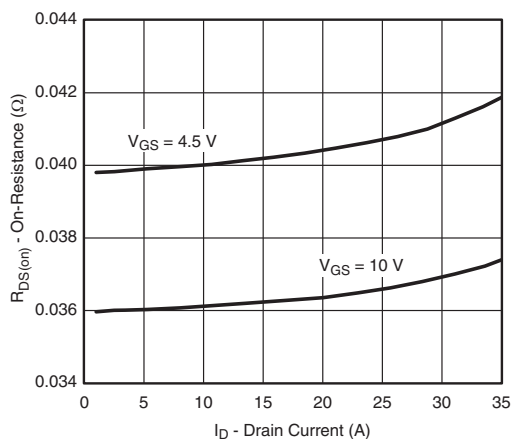
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



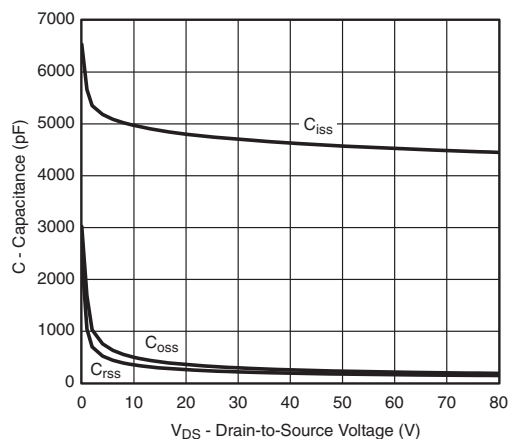
Output Characteristics



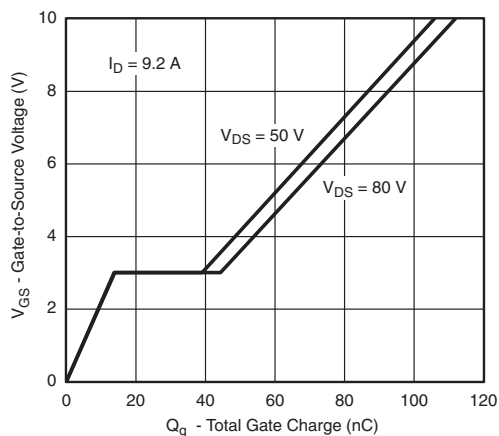
Transfer Characteristics



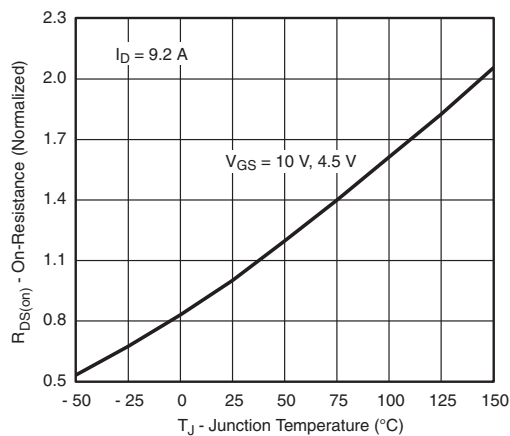
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



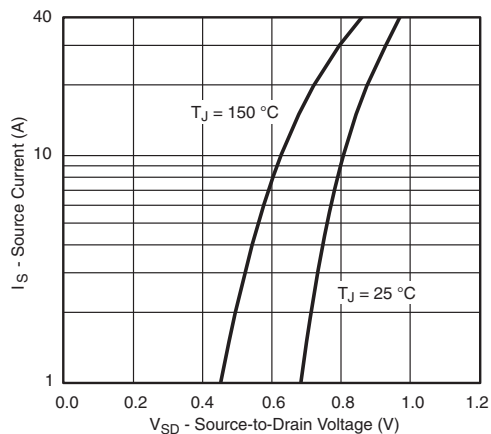
Gate Charge



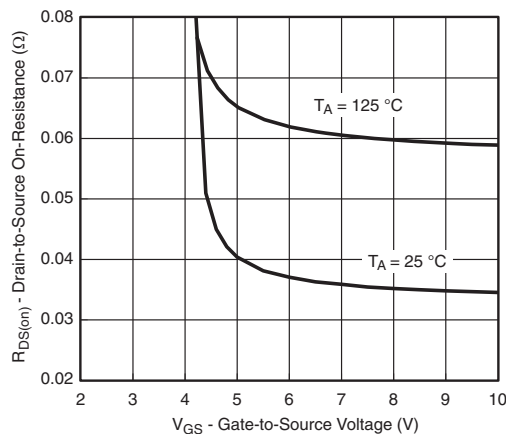
On-Resistance vs. Junction Temperature



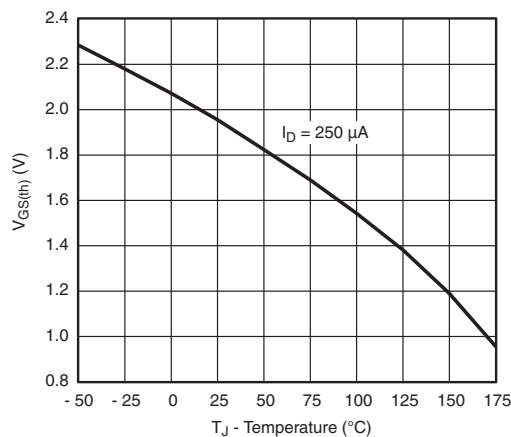
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



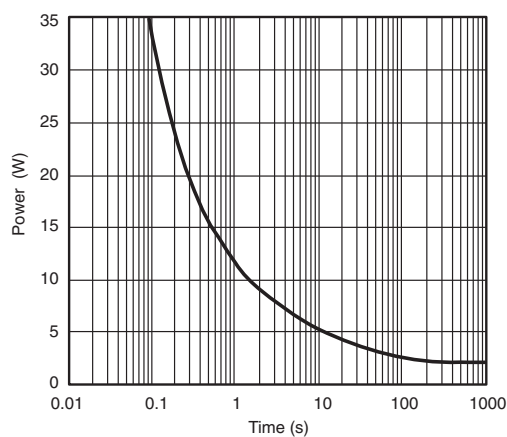
Source-Drain Diode Forward Voltage



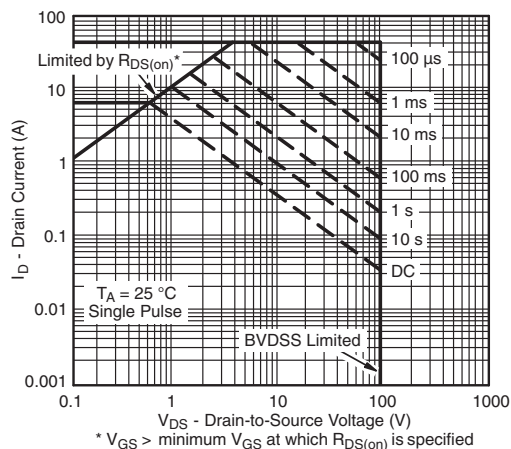
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



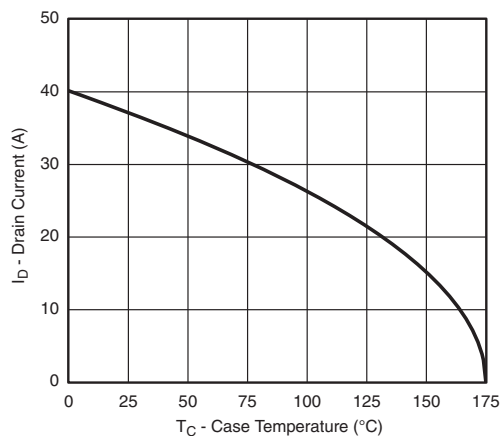
Single Pulse Power, Junction-to-Ambient



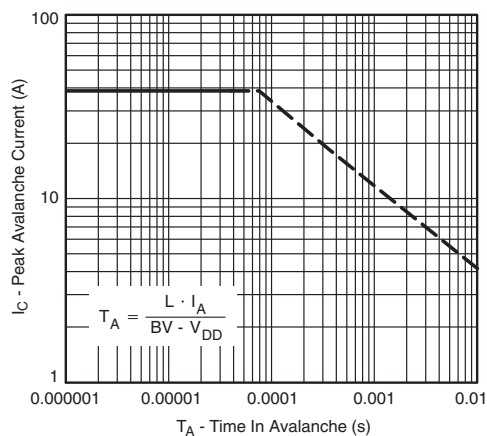
Safe Operating Area, Junction-to-Ambient



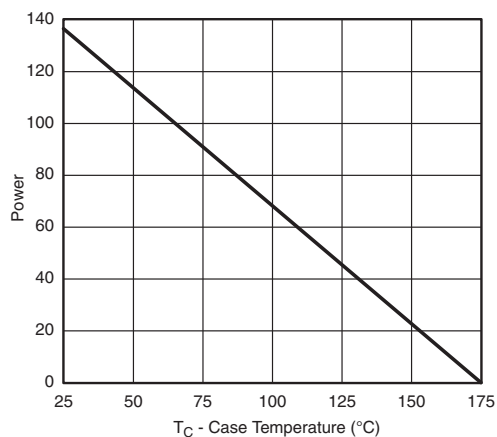
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



Single Pulse Avalanche Capability



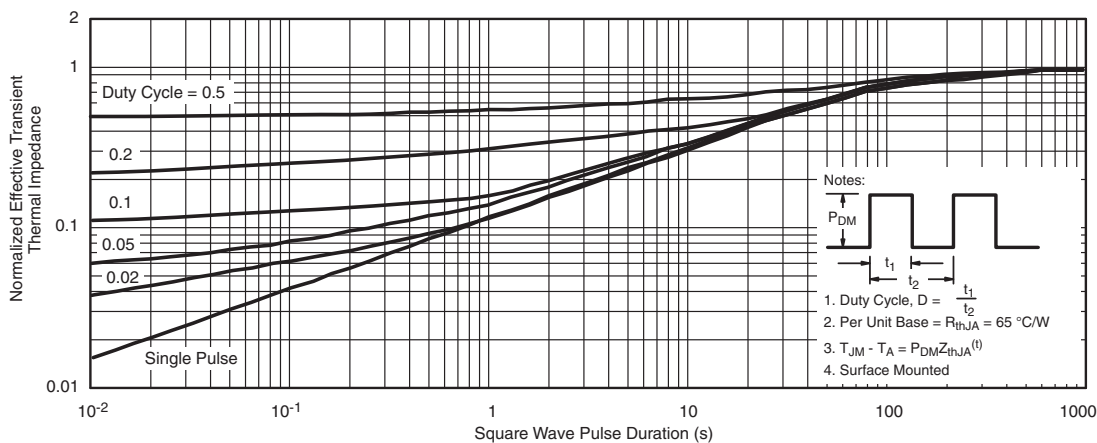
Single Pulse Power, Junction-to-Ambient

Note

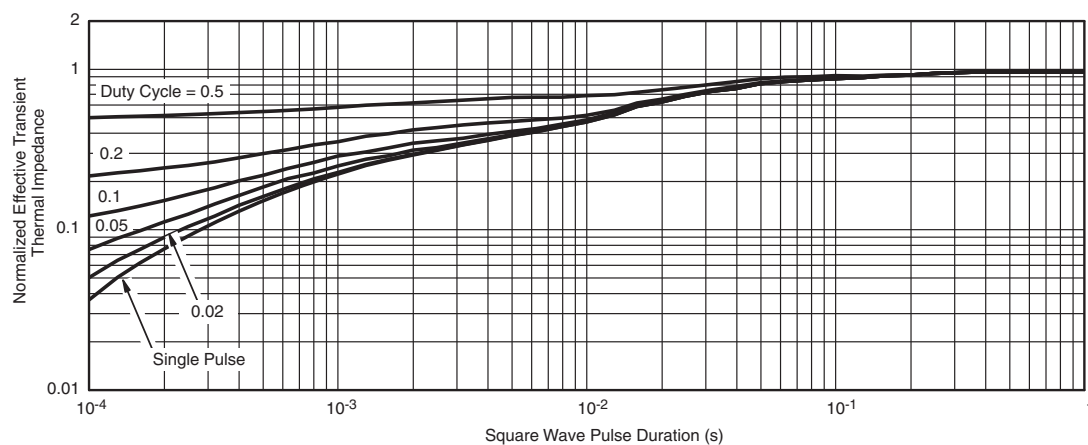
- a. The power dissipation P_D is based on $T_J \text{ max.} = 175^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

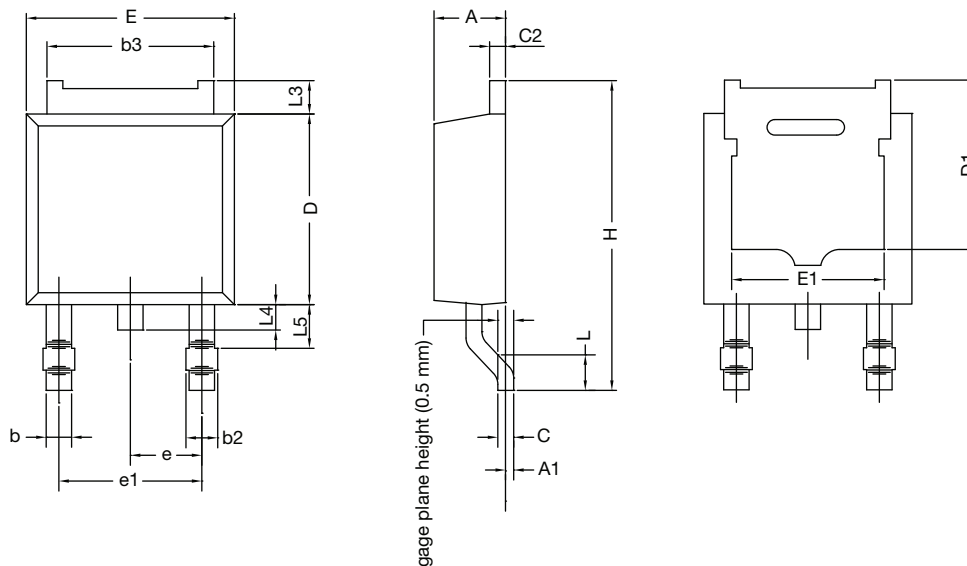


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?73444.

TO-252AA Case Outline

VERSION 1: FACILITY CODE = Y



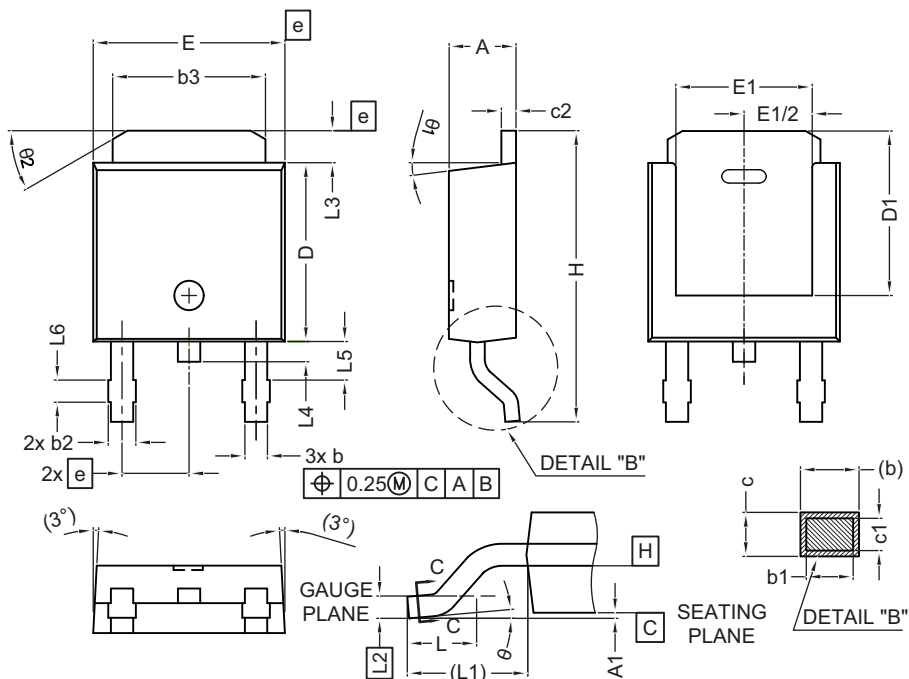
MILLIMETERS		
DIM.	MIN.	MAX.
A	2.18	2.38
A1	-	0.127
b	0.64	0.88
b2	0.76	1.14
b3	4.95	5.46
C	0.46	0.61
C2	0.46	0.89
D	5.97	6.22
D1	4.10	-
E	6.35	6.73
E1	4.32	-
H	9.40	10.41
e	2.28 BSC	
e1	4.56 BSC	
L	1.40	1.78
L3	0.89	1.27
L4	-	1.02
L5	1.01	1.52

Note

- Dimension L3 is for reference only



VERSION 2: FACILITY CODE = N



DIM.	MILLIMETERS	
	MIN.	MAX.
A	2.18	2.39
A1	-	0.13
b	0.65	0.89
b1	0.64	0.79
b2	0.76	1.13
b3	4.95	5.46
c	0.46	0.61
c1	0.41	0.56
c2	0.46	0.60
D	5.97	6.22
D1	5.21	-
E	6.35	6.73
E1	4.32	-
e	2.29 BSC	
H	9.94	10.34

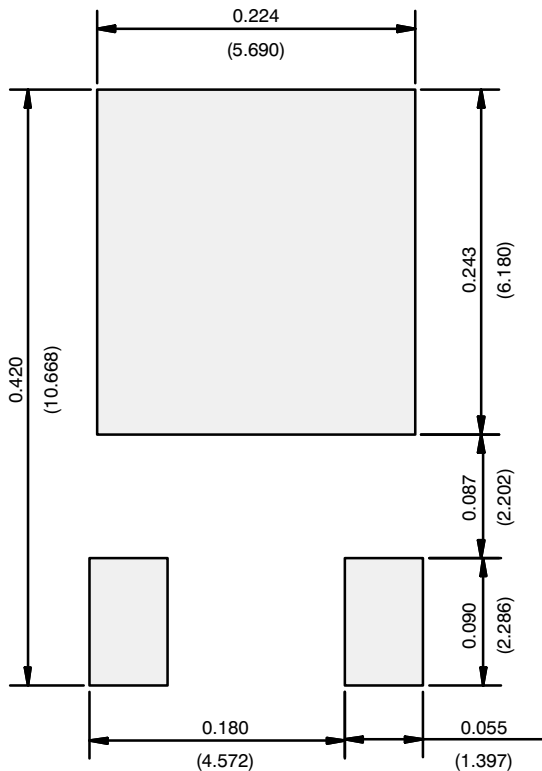
DIM.	MILLIMETERS	
	MIN.	MAX.
L	1.50	1.78
L1	2.74 ref.	
L2	0.51 BSC	
L3	0.89	1.27
L4	-	1.02
L5	1.14	1.49
L6	0.65	0.85
theta	0°	10°
theta1	0°	15°
theta2	25°	35°

Notes

- Dimensioning and tolerance confirm to ASME Y14.5M-1994
- All dimensions are in millimeters. Angles are in degrees
- Heat sink side flash is max. 0.8 mm
- Radius on terminal is optional

ECN: E22-0399-Rev. R, 03-Oct-2022
DWG: 5347

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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