TGA2578

2-6 GHz 30 W GaN Power Amplifier

General Description

Qorvo's TGA2578 is a wideband power amplifier fabricated on Qorvo's 0.25 um GaN on SiC process. Operating from 2 to 6 GHz, it achieves 30 W saturated output power with high efficiency of 40% PAE, and 27 dB small signal gain.

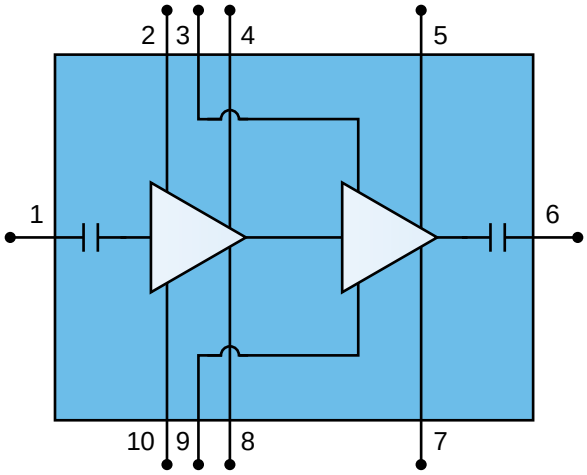
Fully matched to 50 ohms with integrated DC blocking caps on both I/O ports, the TGA2578 is ideally suited to support both commercial and defense related applications.

The TGA2578 is 100% DC and RF tested on-wafer to ensure compliance to power and PAE specifications.

Product Features

- Frequency Range: 2–6 GHz
- Psat: 45 dBm CW
- PAE: 40% CW
- Small Signal Gain: 27 dB
- Input Return Loss: >20 dB
- IM3: -30 dBc @ 40 dBm P_{OUT}/Tone
- Bias: V_D = 28 V, I_{DQ} = 400 mA, V_G = -2.8 V Typical
- Chip Dimensions: 6.4 x 5.0 x 0.10 mm

Functional Block Diagram



Applications

- Communications
- Electronic Warfare
- Test Instrumentation
- EMC Amplifier

Ordering Information

Part	Description
TGA2578	TGA2578 Amplifier, Gel Pack, Qty 10
TGA2578EVB0317	TGA2578 Evaluation Board, Qty 1

Absolute Maximum Ratings

Parameter	Value/Range
Drain Voltage (V_D)	40 V
Gate Voltage Range (V_G)	-8 to 0 V
Drain Current (I_D)	5 A
Gate Current (I_G)	-15 to 30 mA
Power Dissipation, 85 °C (P_{DISS})	92.5 W
Input Power, CW, 50 Ω, (P_{IN})	27 dBm
Input Power, CW, VSWR 3:1, V_D = 30 V, 85 °C, (P_{IN})	27 dBm
Input Power, CW, VSWR 10:1, V_D = 28 V, 85 °C (P_{IN})	25 dBm
Channel temperature (T_{CH})	275 °C
Mounting Temperature (30 Seconds)	320 °C
Storage Temperature	-55 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value/Range
Drain Voltage (V_D)	28 V
Drain Current (I_{DQ})	400 mA
Drain Current Under RF Drive (I_{D_DRIVE})	3800 mA
Gate Voltage (V_G)	-2.8 V

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all operating conditions.

Electrical Specifications

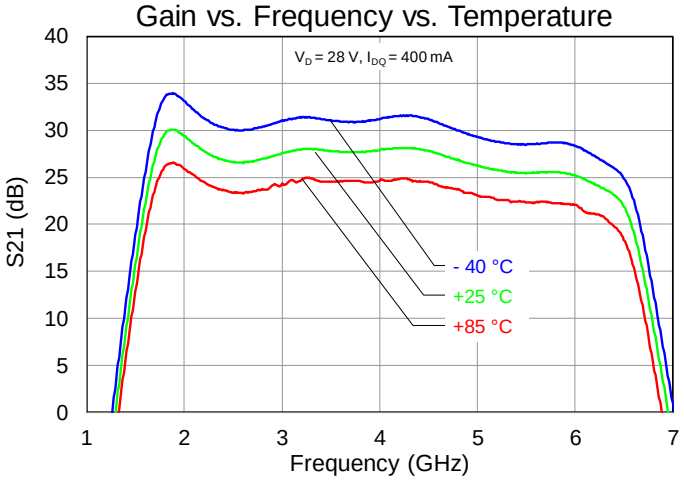
Test conditions unless otherwise noted: 25 °C , V_D = 28 V, I_D = 400 mA, V_G = -2.8 V Typical

Data de-embedded feeding line losses, data include bond wire effects.

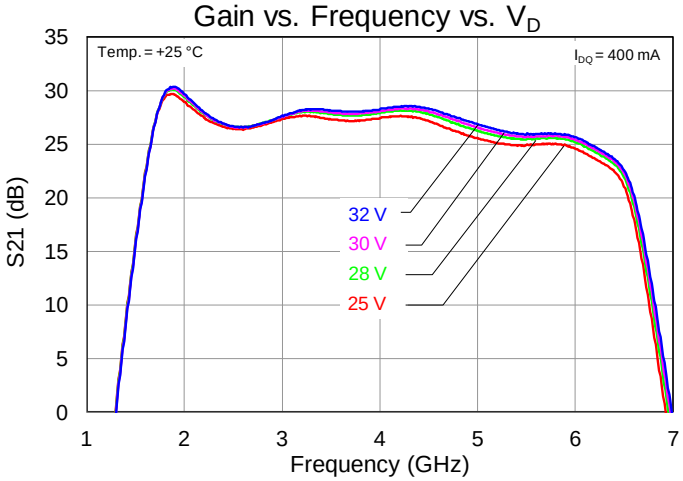
Parameter	Min	Typical	Max	Units
Operational Frequency Range	2		6	GHz
Small Signal Gain		27		dB
Input Return Loss		20		dB
Output Return Loss		5		dB
Output Power @ P_{IN} = 23 dBm		45		dBm
Power Added Efficiency @ Pin = 23 dBm		40		%
IM3 @ P_{OUT}/Tone = 40 dBm		-30		dBc
IM5 @ P_{OUT}/Tone = 40 dBm		-40		dBc
Small Signal Gain Temperature Coefficient		-0.05		dB/°C
Output Power Temperature Coefficient		-0.02		dBm/°C

Typical Performance

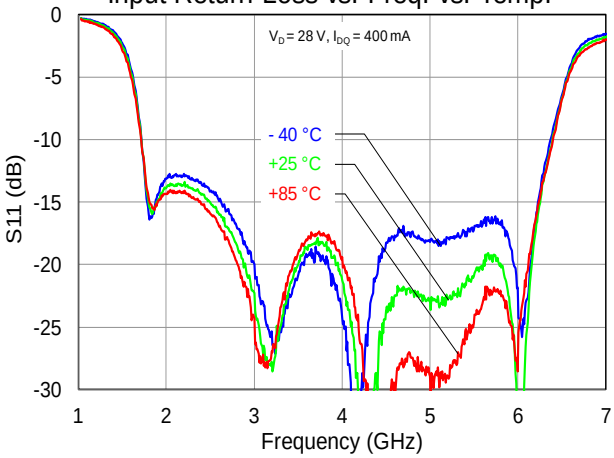
Gain vs. Frequency vs. Temperature



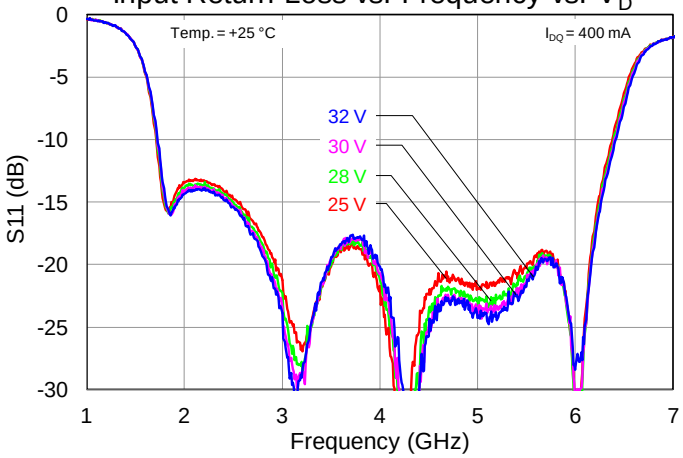
Gain vs. Frequency vs. V_D



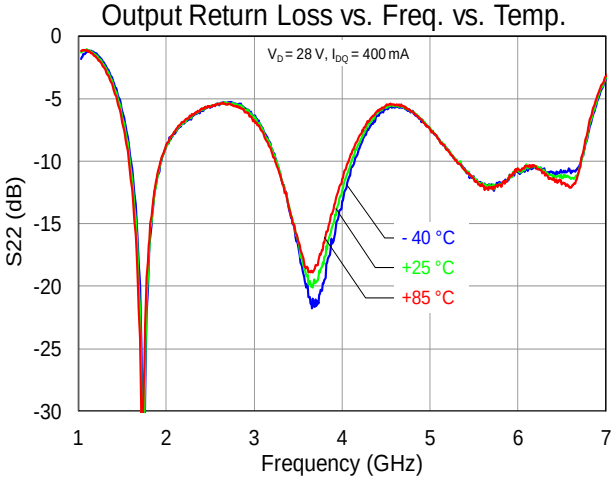
Input Return Loss vs. Freq. vs. Temp.



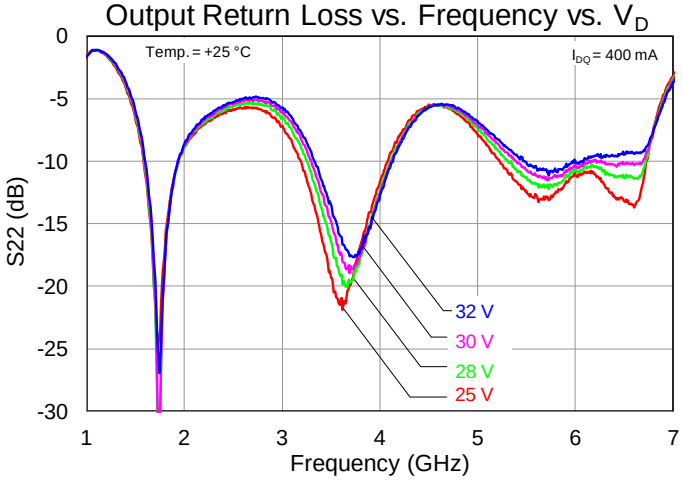
Input Return Loss vs. Frequency vs. V_D



Output Return Loss vs. Freq. vs. Temp.

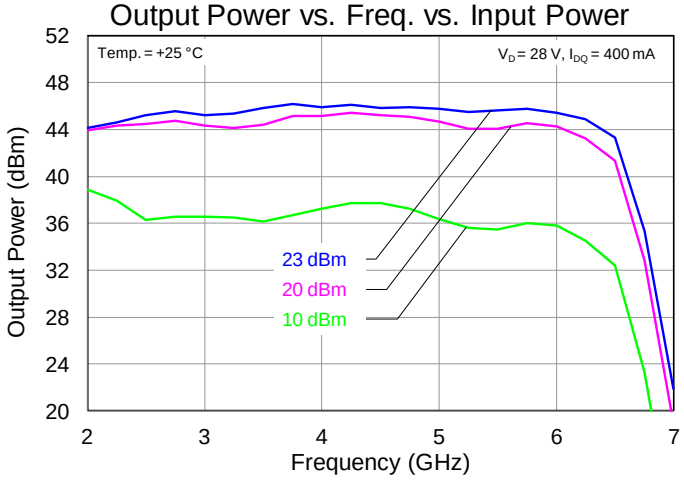


Output Return Loss vs. Frequency vs. V_D

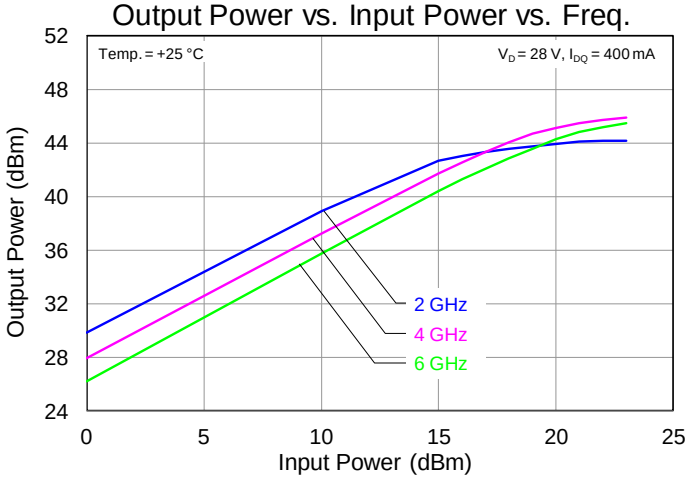


Typical Performance

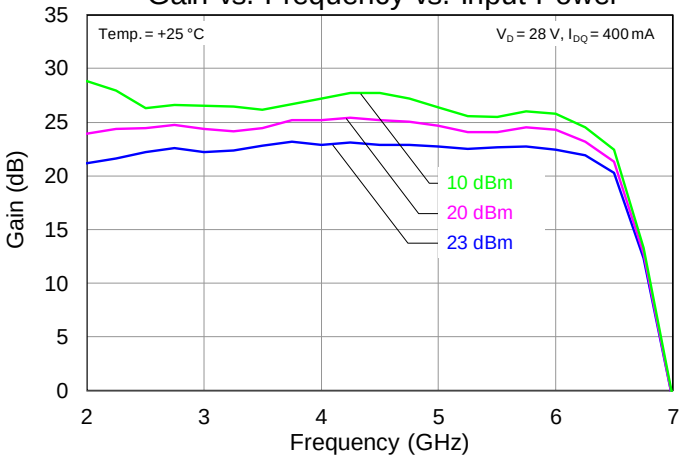
Output Power vs. Freq. vs. Input Power



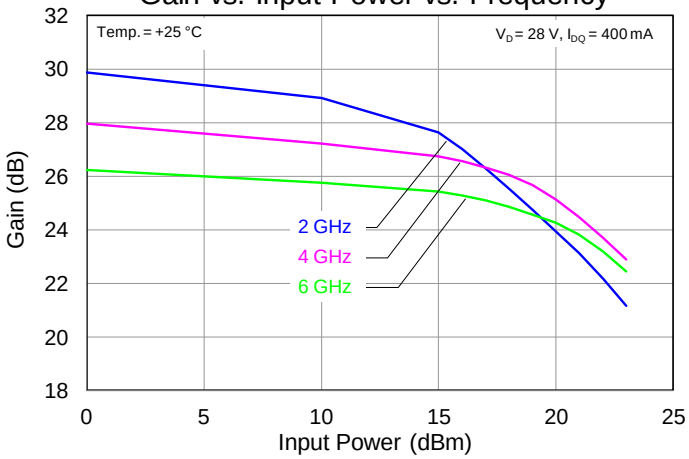
Output Power vs. Input Power vs. Freq.



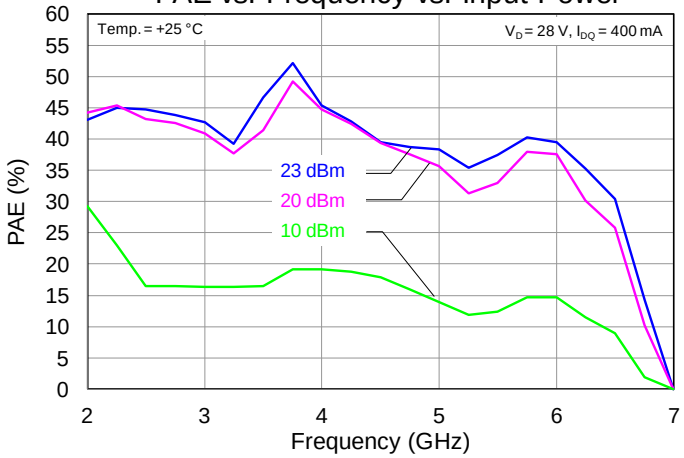
Gain vs. Frequency vs. Input Power



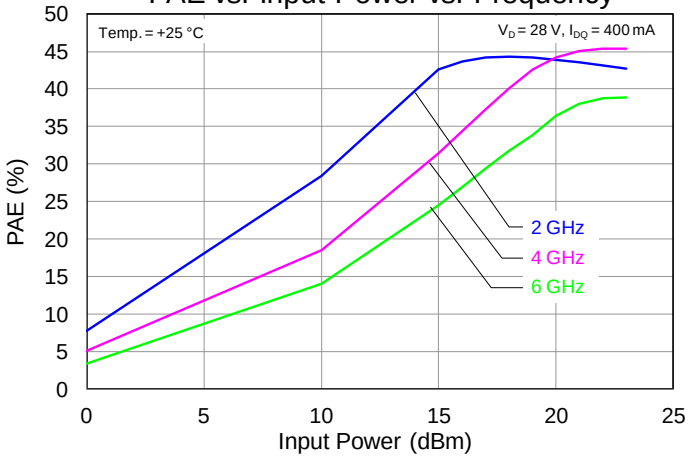
Gain vs. Input Power vs. Frequency



PAE vs. Frequency vs. Input Power

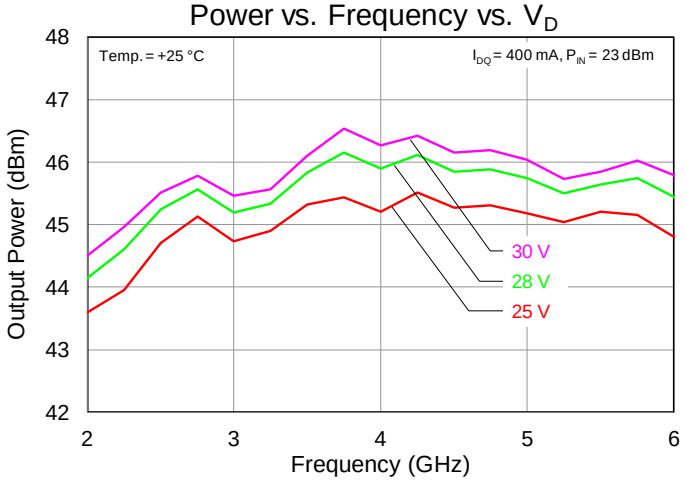


PAE vs. Input Power vs. Frequency

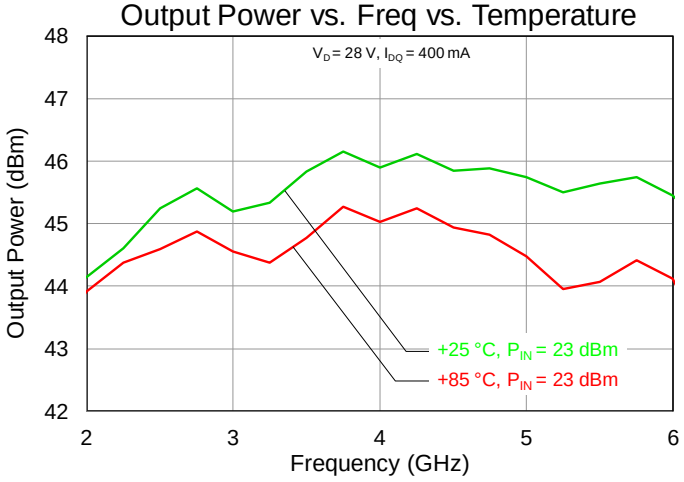


Typical Performance

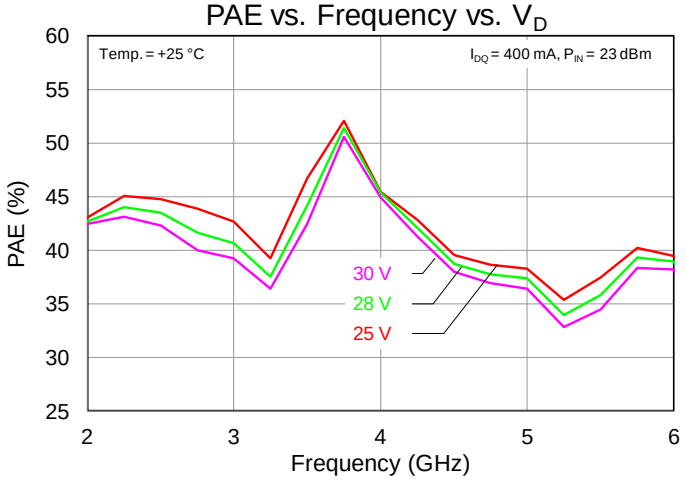
Power vs. Frequency vs. V_D



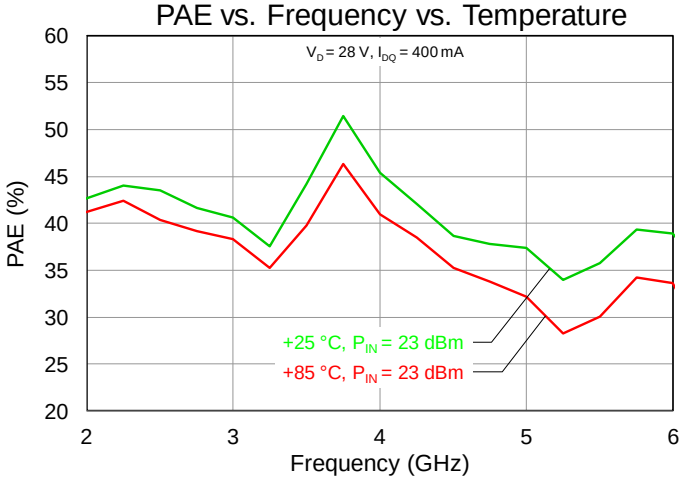
Output Power vs. Freq vs. Temperature



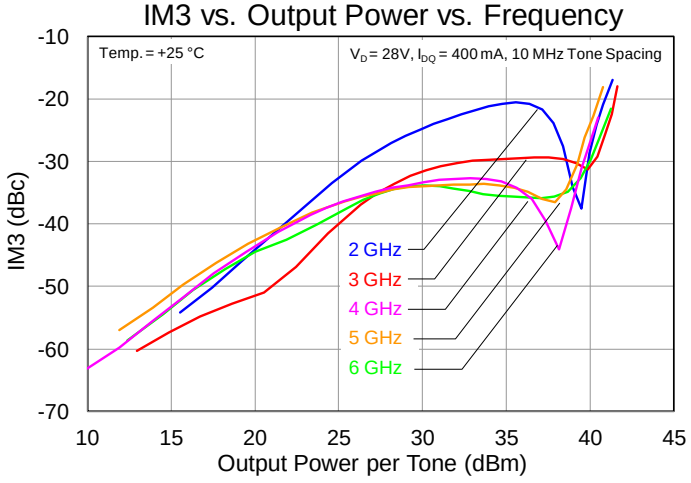
PAE vs. Frequency vs. V_D



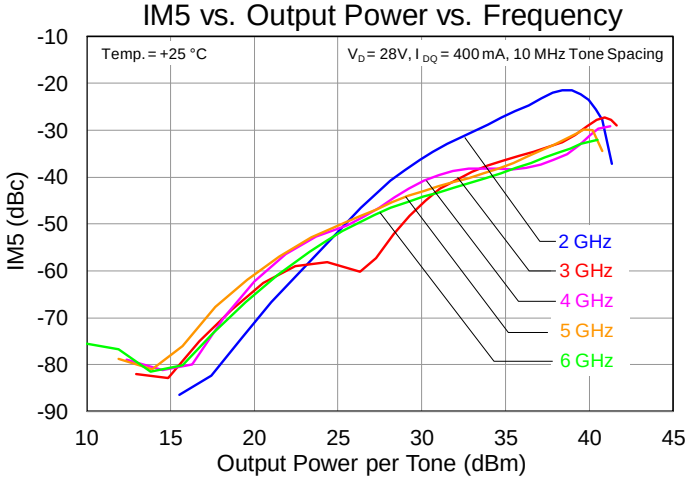
PAE vs. Frequency vs. Temperature



IM3 vs. Output Power vs. Frequency

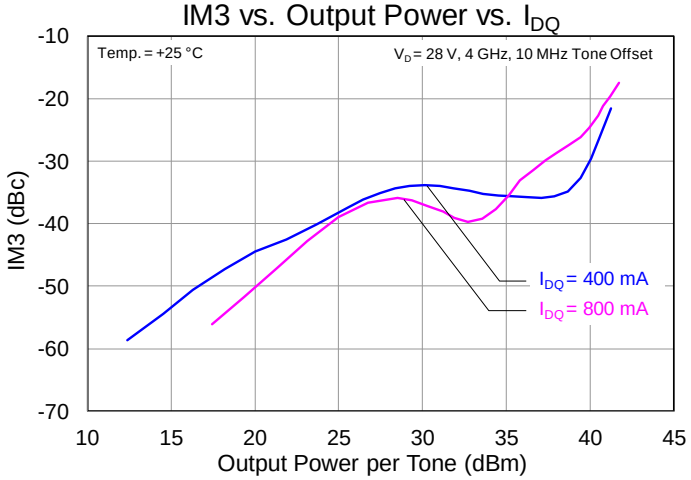


IM5 vs. Output Power vs. Frequency

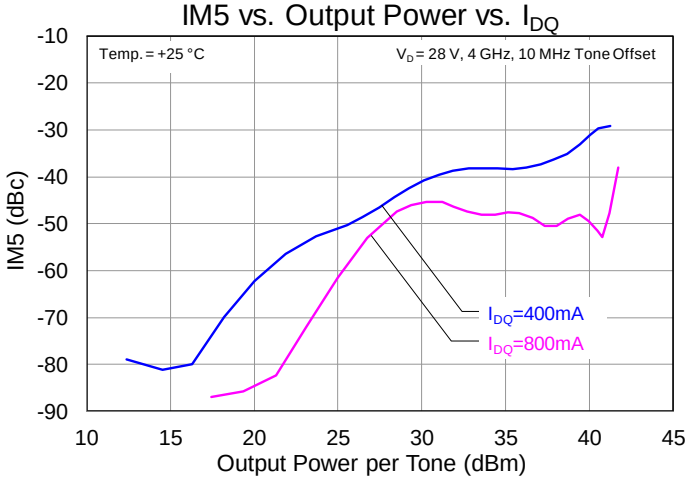


Typical Performance

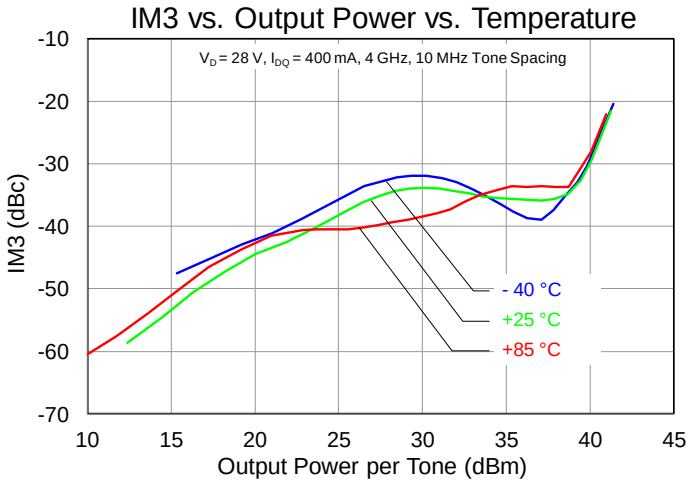
IM3 vs. Output Power vs. I_{DQ}



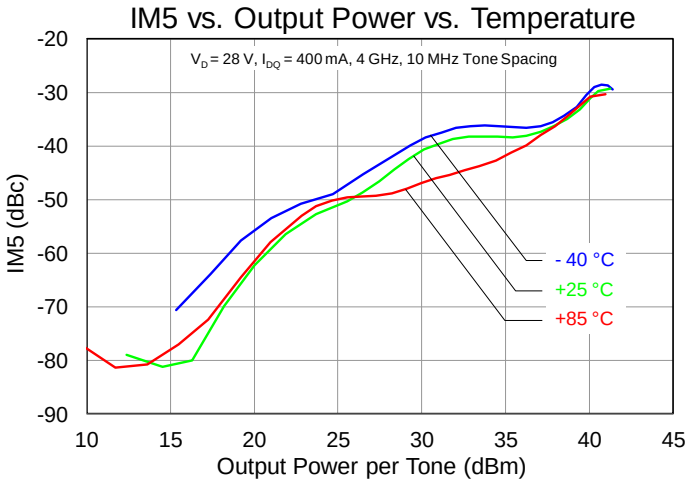
IM5 vs. Output Power vs. I_{DQ}



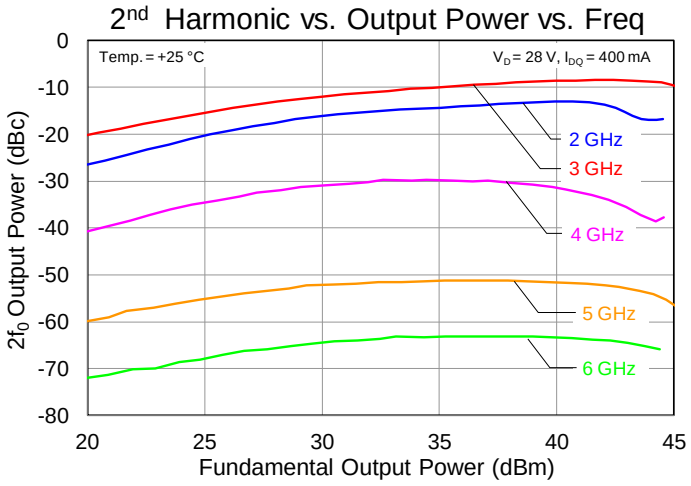
IM3 vs. Output Power vs. Temperature



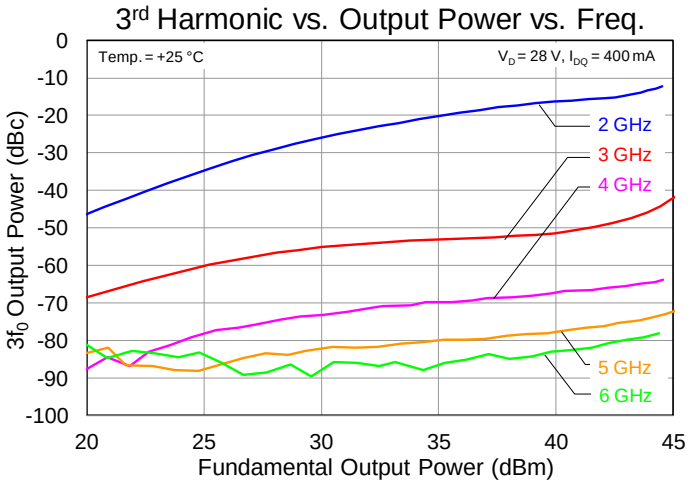
IM5 vs. Output Power vs. Temperature



2nd Harmonic vs. Output Power vs. Freq



3rd Harmonic vs. Output Power vs. Freq.



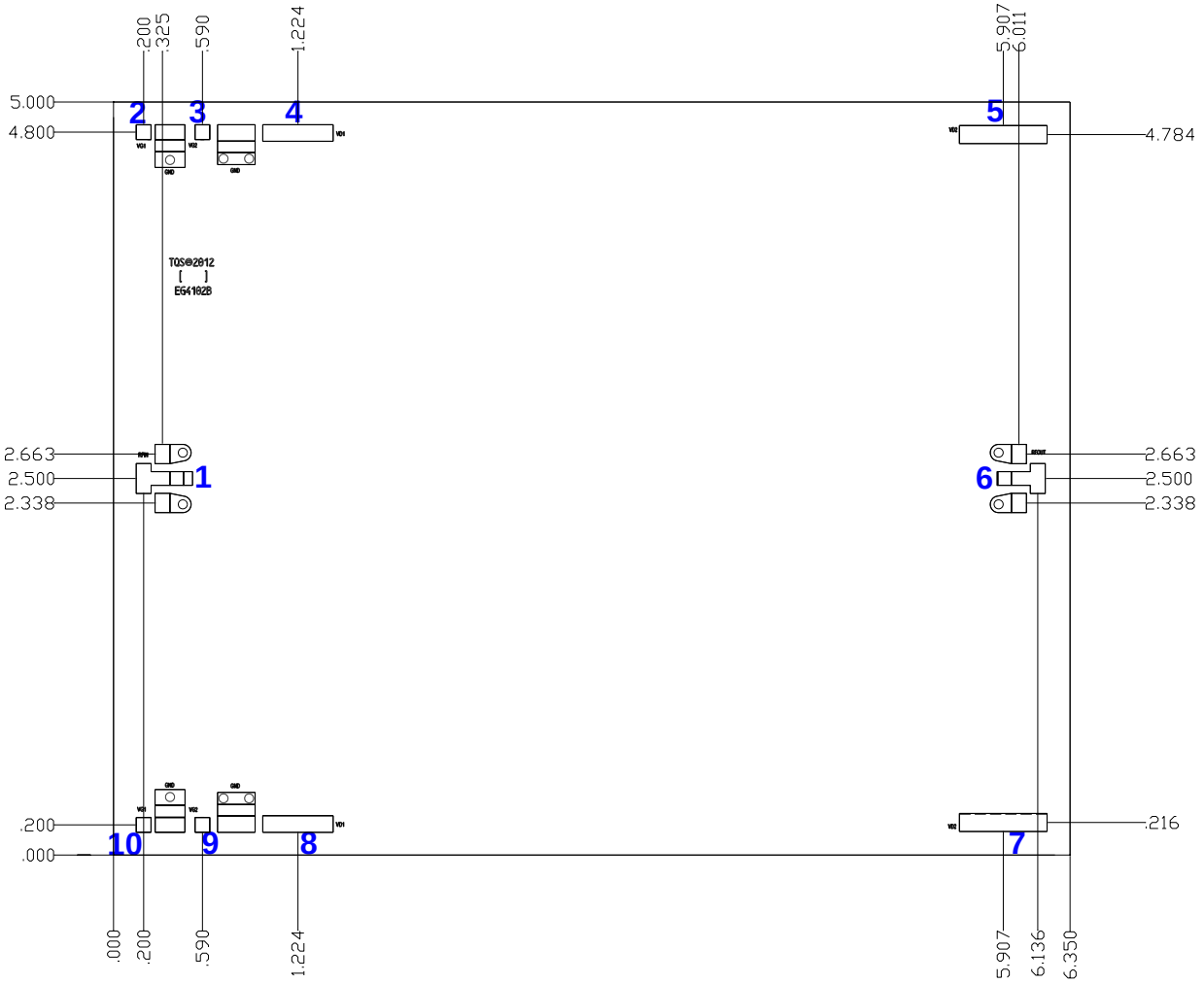
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC})	T_{BASE} = 85 °C, V_D = 28 V, I_{D_Drive} = 3.5 A, P_{OUT} = 45 dBm, P_{DISS} = 66.4 W	1.33	ºC/W
Channel Temperature (T_{CH})		173.5	°C

Notes:

1. Thermal resistance measured to back of carrier plate. MMIC mounted on 20 mils CuMo carrier using 1.5 mil 80/20 AuSn.
2. Channel temperature indicated is an IR scan equivalent temperature. Thermal resistance is calculated using this value. Additional information can be found in the Qorvo Applications Note “GaN Device TCHMAX Theta-JC and Reliability Estimates,” located here https://www.qorvo.com/products/d/da006480

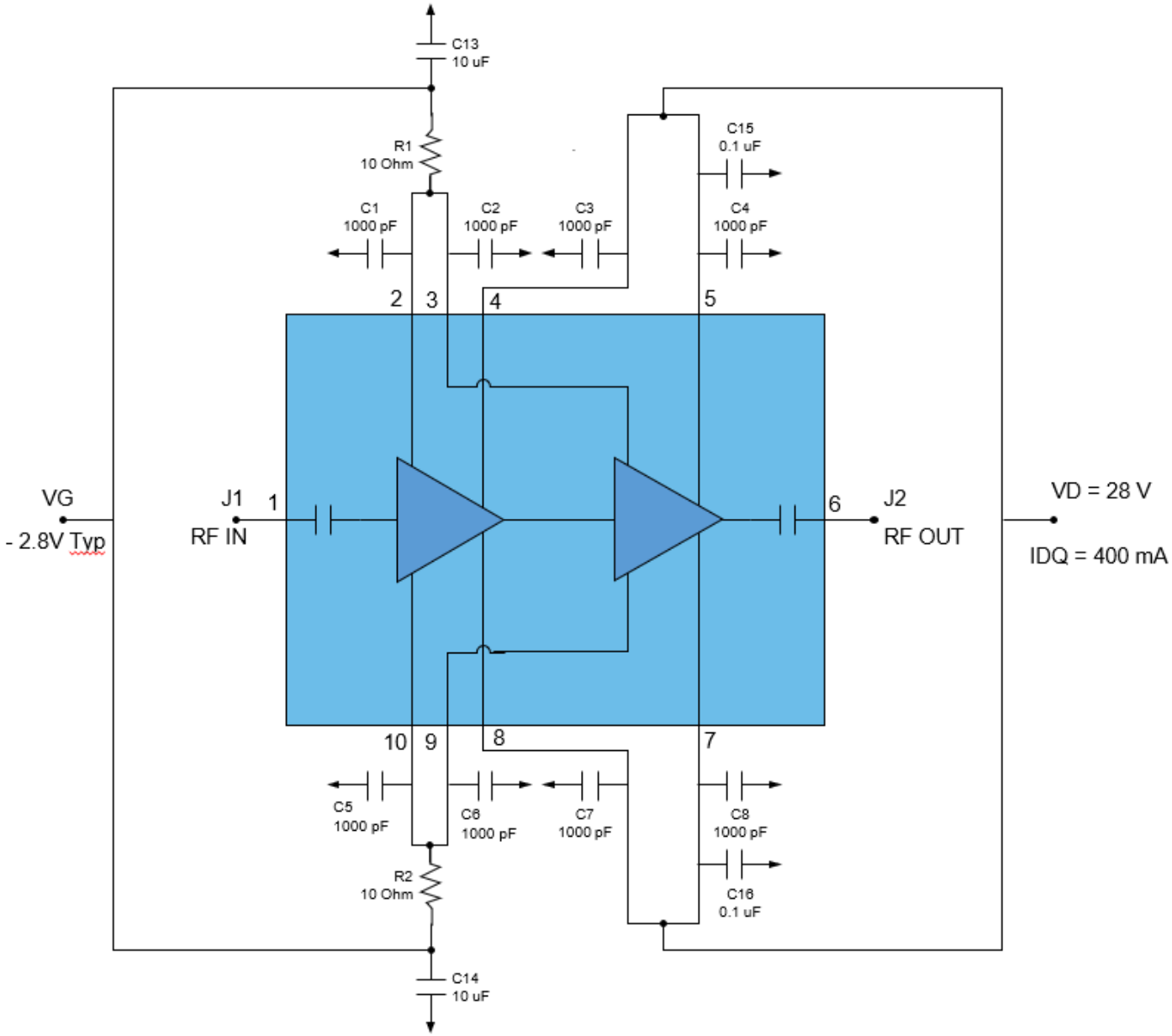
Mechanical Drawing and Bond Pad Descriptions



Unit: millimeters, Thickness: 0.10, Die x, y size tolerance: +/- 0.050
Chip edge to bond pad dimensions are shown to center of pad
Ground is backside of die

Bond Pad	Symbol	Pad Size	Descriptions
1	RF In	0.100 x 0.200	Input; matched to 50 ohms; AC coupled.
2, 10	V_{G1}	0.100 x 0.100	Gate voltage, V_{G1} top and bottom. Bias network is required; must be biased from both sides; see Application Circuit on page 8 as an example.
3, 9	V_{G2}	0.100 x 0.100	Gate voltage, V_{G1} top and bottom. Bias network is required; must be biased from both sides; see Application Circuit on page 8 as an example.
4, 8	V_{D1}	0.450 x 0.100	Drain voltage, V_{D1} top and bottom. Bias network is required; must be biased from both sides; see Application Circuit on page 8 as an example.
5, 7	V_{D2}	0.580 x 0.125	Drain voltage, V_{D2} top and bottom. Bias network is required; must be biased from both sides; see Application Circuit on page 8 as an example.
6	RF Out	0.100 x 0.200	Input; matched to 50 ohms; AC coupled.

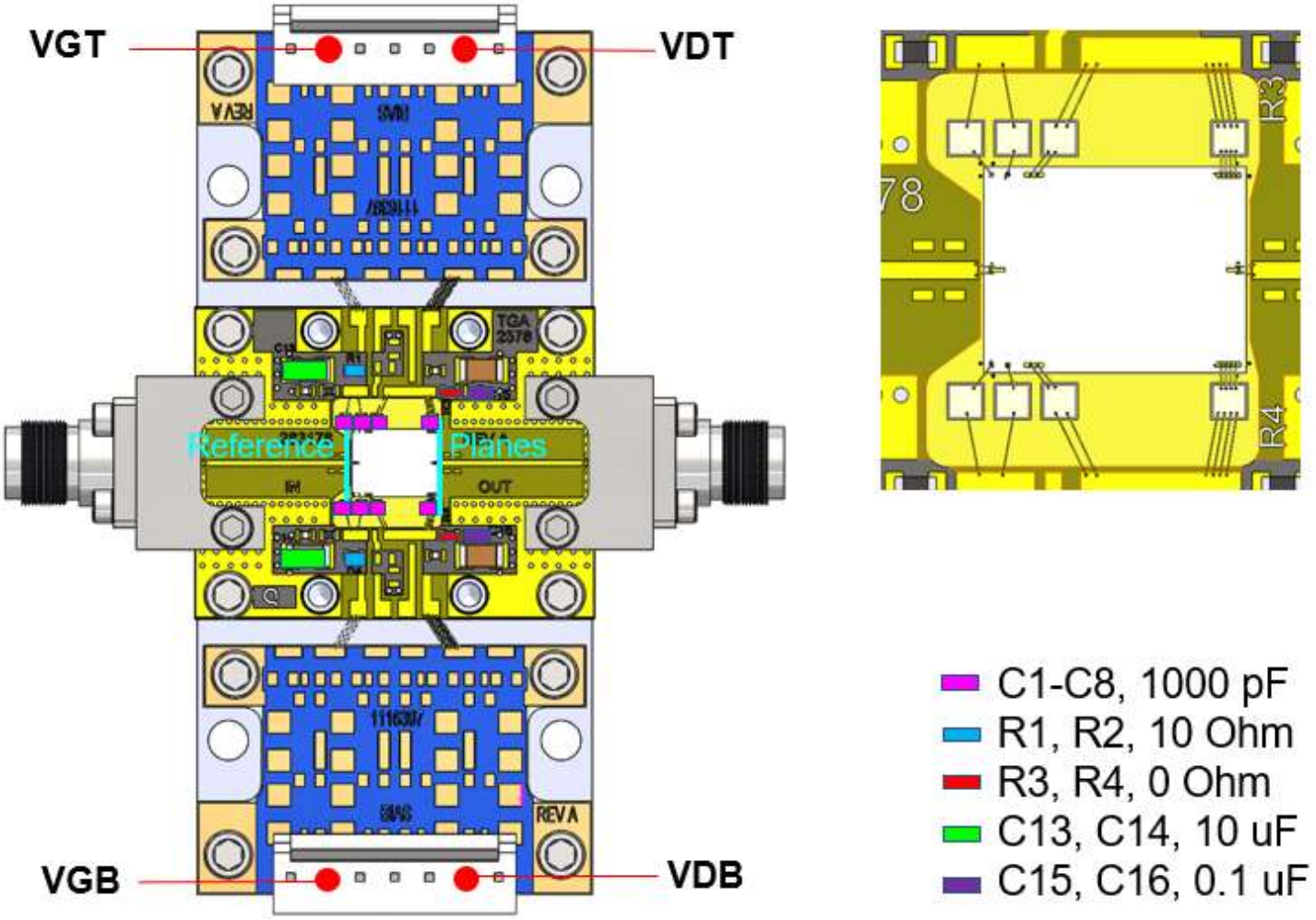
Application Circuit



Bias-up Procedure
1. Set I_D limit to 4.5 A, I_G limit to 25 mA
2. Apply -5.0 V to V_G
3. Apply +28 V to V_D
4. Adjust V_G more positive until I_{DQ} = 400 mA (V_G ~ -2.8 V Typical)
5. Apply RF signal

Bias-down Procedure
1. Turn off RF signal
2. Reduce V_G to -5.0 V. Ensure I_{DQ} ~ 0 mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

Evaluation Board



DC bias must be applied from both sides as shown in Application Circuit

Assembly Notes

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300 °C to 3-4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1B	JEDEC/JESD22-A114

Caution!
ESD-Sensitive Device

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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Email: customer.support@qorvo.com

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