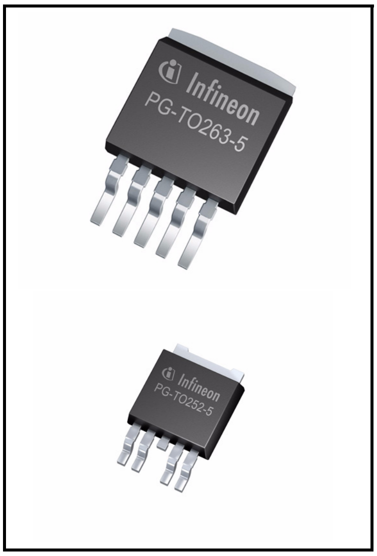
OPTIREG™ linear TLE4270-2

5 V low drop fixed voltage regulator



Features

- Output voltage tolerance ≤ ±2%
- 650 mA output current capability
- Low-drop voltage
- Reset functionality
- Adjustable reset time
- Suitable for use in automotive electronics
- Integrated overtemperature protection
- Reverse polarity protection
- Input voltage up to 42 V
- Overvoltage protection up to 65 V (≤ 400 ms)
- Short-circuit proof
- Wide temperature range
- ESD protection: ±2 kV HBM[1)]
- Green Product (RoHS-compliant)

Potential applications

General automotive applications.

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

The OPTIREG™ linear TLE4270-2 is a 5-V low drop fixed-voltage regulator. The maximum input voltage is 42 V (65 V, ≤ 400 ms). Up to an input voltage of 26 V and for an output current up to 650 mA it regulates the output voltage within a 2% accuracy. The short circuit protection limits the output current of more than 650 mA. The device incorporates overvoltage protection and a temperature protection which turns off the device at high temperatures.

1) ESD susceptibility, human body model (HBM) according to EIA/JESD 22-A114B.

Type	Package	Marking
TLE4270-2G	PG-TO263-5	4270-2G
TLE4270-2D	PG-TO252-5	4270-2D

Table of contents

1 Block diagram

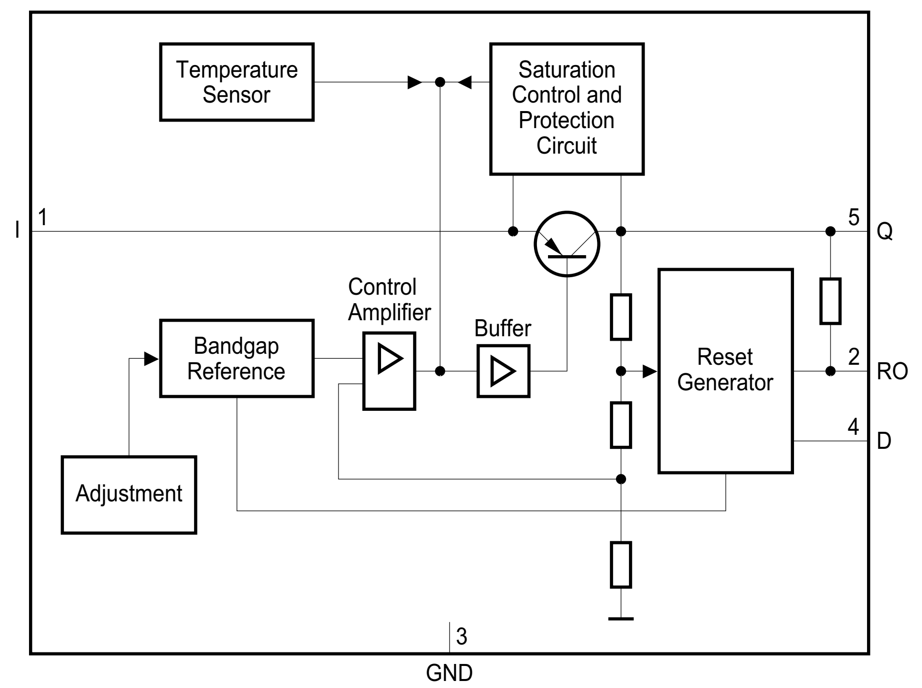


Figure 1 Block diagram

2 Pin configuration

2.1 Pin assignment

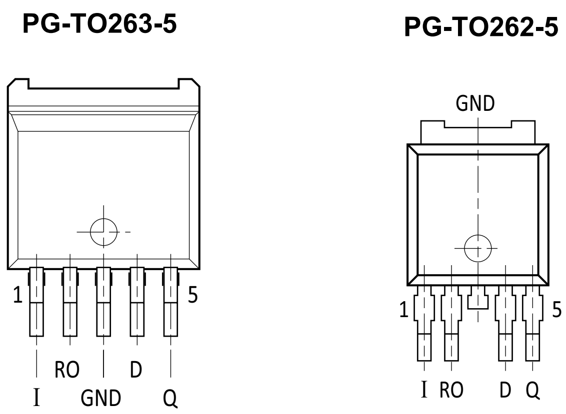


Figure 2 **Pin configuration** (top view)

2.2 Pin definitions and functions

Pin	Symbol	Function
1	I	**Input;** block to ground directly at the IC with a ceramic capacitor
2	RO	**Reset output;** the open collector output is connected to the 5-V output via an integrated resistor of 30 kΩ
3	GND	**Ground;** internally connected to heatsink
4	D	**Reset delay;** connect a capacitor to ground for delay time adjustment
5	Q	**5-V output;** block to ground with 22 µF capacitor, ESR < 3 Ω

3 General product characteristics

3.1 Absolute maximum ratings

Table 1 Absolute maximum ratings

T_j = -40°C to 150°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input I							
Voltage	V_I	-42	–	42	V	–	P_3.1.1
Voltage	V_I	–	–	65	V	$t \leq 400$ ms	P_3.1.2
Current	I_I	–	–	–	–	Internally limited	P_3.1.3
Reset output RO							
Voltage	V_{RO}	-0.3	–	7	V	–	P_3.1.4
Current	I_{RO}	–	–	–	–	Internally limited	P_3.1.5
Reset delay D							
Voltage	V_D	-0.3	–	7	V	–	P_3.1.6
Current	I_D	–	–	–	–	Internally limited	P_3.1.7
Output Q							
Voltage	V_Q	-1.0	–	16	V	–	P_3.1.8
Current	I_Q	–	–	–	–	Internally limited	P_3.1.9
Ground GND							
Current	I_{GND}	-0.5	–	–	A	–	P_3.1.10
Temperatures							
Junction temperature	T_j	–	–	150	°C	–	P_3.1.11
Storage temperature	T_{stg}	-50	–	150	°C	–	P_3.1.12
ESD susceptibility							
ESD susceptibility	$V_{ESD,HBM}$	-2		2	kV	[1] Human body model (HBM)	P_3.1.13

1) ESD susceptibility, human body model (HBM) according to EIA/JESD 22-A114B.

3.2 Functional range

Table 2 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage	V_I	6	–	42	V	–	P_3.2.1
Junction temperature	T_j	-40	–	150	°C	–	P_3.2.2

3.3 Thermal resistance

Table 3 Thermal resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Thermal resistance							
Junction ambient	R_{thJA}	–	–	65	K/W	[1] PG-TO263-5	P_3.3.1
Junction ambient	R_{thJA}	–	–	79	K/W	[1] PG-TO252-5	P_3.3.2
Junction case	R_{thJC}	–	–	3	K/W	PG-TO263-5	P_3.3.3

1) Mounted on PCB, 80 × 80 × 1.5 mm^3; 35 µ Cu; 5 µ Sn; footprint only; zero airflow.

4 Functional description

4.1 Circuit description

The control amplifier compares a reference voltage, which is kept highly accurate by resistance adjustment, to a voltage that is proportional to the output voltage and drives the base of a series transistor via a buffer. Saturation control as a function of the load current prevents any over-saturation of the power element.

The IC also incorporates a number of internal circuits for protection against:

- Overload
- Overvoltage
- Overtemperature
- Reverse polarity

4.2 Electrical characteristics

Table 4 Electrical characteristics

V_I = 13.5 V; T_j = -40°C to 125°C (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output voltage	V_Q	4.90	5.00	5.10	V	5 mA ≤ I_Q ≤ 550 mA; 6 V ≤ V_I ≤ 26 V	P_4.0.1
	V_Q	4.90	5.00	5.10	V	26 V ≤ V_I ≤ 36 V; I_Q ≤ 300 mA	P_4.0.2
Output current limiting	I_{Qmax}	650	850	–	mA	V_Q = 0 V	P_4.0.3
Current consumption $I_q = I_I - I_Q$	I_q	–	1	1.5	mA	I_Q = 5 mA	P_4.0.4
	I_q	–	55	75	mA	I_Q = 550 mA	P_4.0.5
	I_q	–	70	90	mA	I_Q = 550 mA; V_I = 5 V	P_4.0.6
Drop voltage	V_{DR}	–	350	700	mV	[1] I_Q = 550 mA	P_4.0.7
Load regulation	$\Delta V_{Q,Lo}$	–	25	50	mV	I_Q = 5 to 550 mA; V_I = 6 V	P_4.0.8
Line regulation	$\Delta V_{Q,Li}$	–	12	25	mV	V_I = 6 to 26 V I_Q = 5 mA	P_4.0.9
Power supply ripple rejection	*PSRR*	–	54	–	dB	f_r = 100 Hz; V_r = 0.5 Vpp	P_4.0.10
Reset generator							
Switching threshold	V_{RT}	4.5	4.65	4.8	V	–	P_4.0.11
Reset high voltage	V_{ROH}	4.5	–	–	V	–	P_4.0.12
Reset low voltage	V_{ROL}	–	60	–	mV	[2] R_{int} = 30 kΩ; 1.0 V ≤ V_Q ≤ 4.5 V	P_4.0.13
	V_{ROL}	–	200	400	mV	I_R = 3 mA, V_Q = 4.4 V	P_4.0.14
Reset pull-up	R_{int}	18	30	46	kΩ	Internally connected to Q	P_4.0.15

Functional description

Table 4 Electrical characteristics (cont'd)

V_I = 13.5 V; T_j = -40°C to 125°C (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Charge current	$I_{D,c}$	8	14	25	µA	V_D = 1.0 V	P_4.0.16
Upper reset timing threshold	V_{DU}	1.4	1.8	2.3	V	–	P_4.0.17
Lower reset timing threshold	V_{DL}	0.2	0.45	0.8	V	$V_Q < V_{RT}$	P_4.0.18
Delay time	t_{rd}	–	13	–	ms	C_D = 100 nF	P_4.0.19
Reset reaction time	t_{rr}	–	–	3	µs	C_D = 100 nF	P_4.0.20
Overvoltage protection							
Turn-off voltage	$V_{I, ov}$	42	44	46	V	–	P_4.0.21

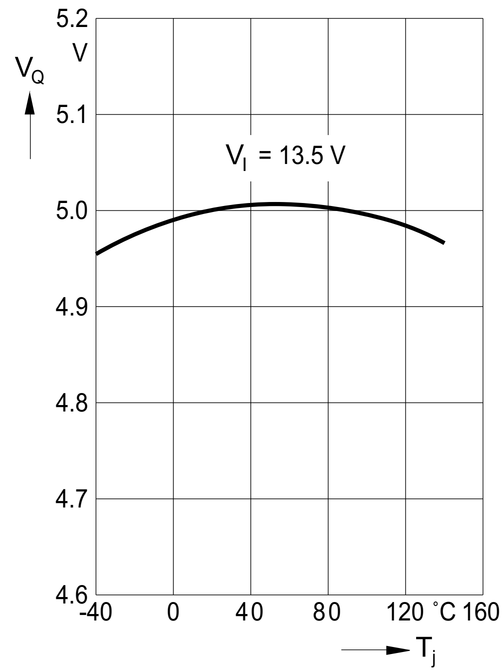
1) Drop voltage = V_I - V_Q (measured when the output voltage has dropped 100 mV from the nominal value obtained at 13.5 V input).

2) Reset peak is always lower than 1.0 V.

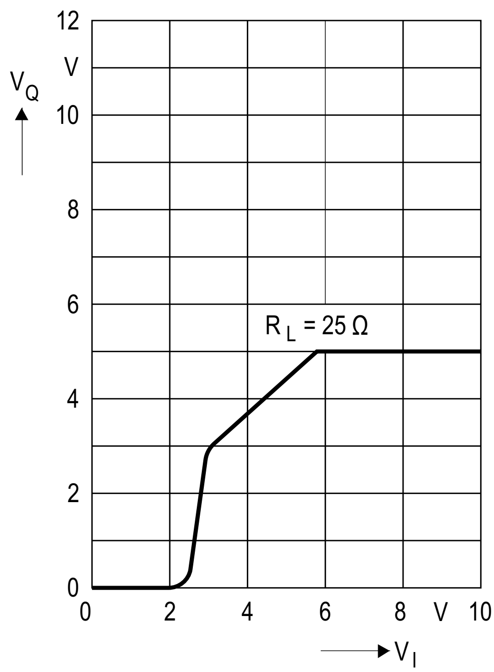
4.3 Typical performance graphs

Typical performance characteristics

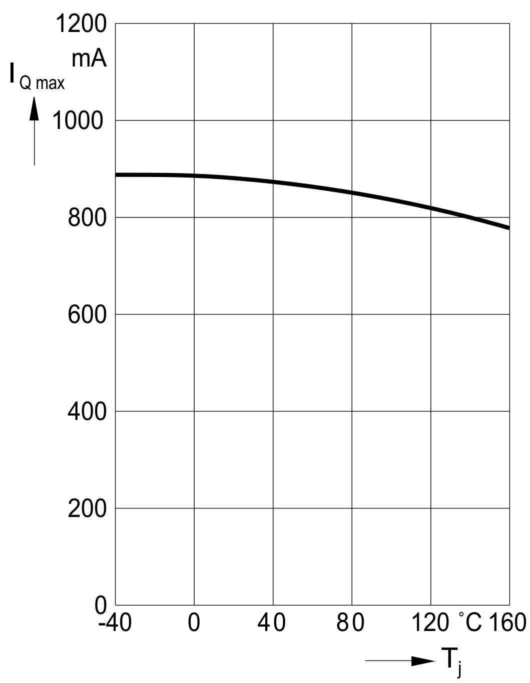
Output voltage V_Q versus junction temperature T_j



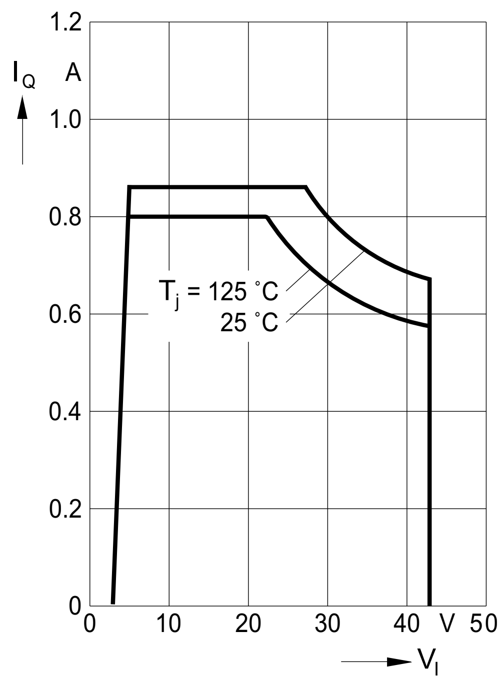
Output voltage V_Q versus input voltage V_I



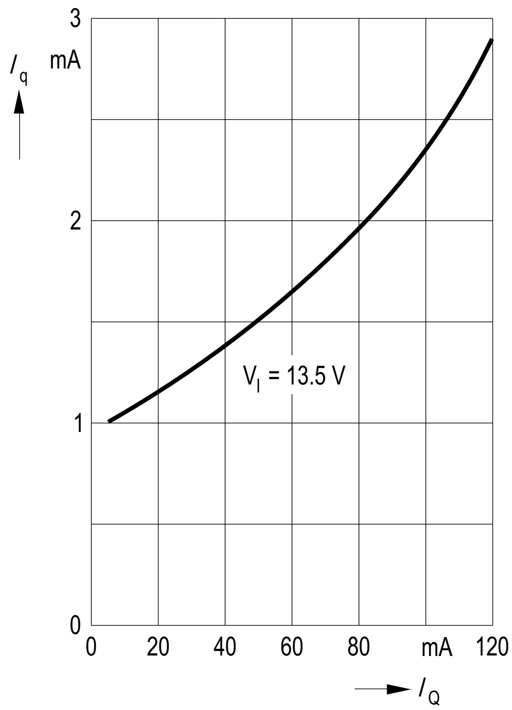
Output current I_Q versus junction temperature T_j



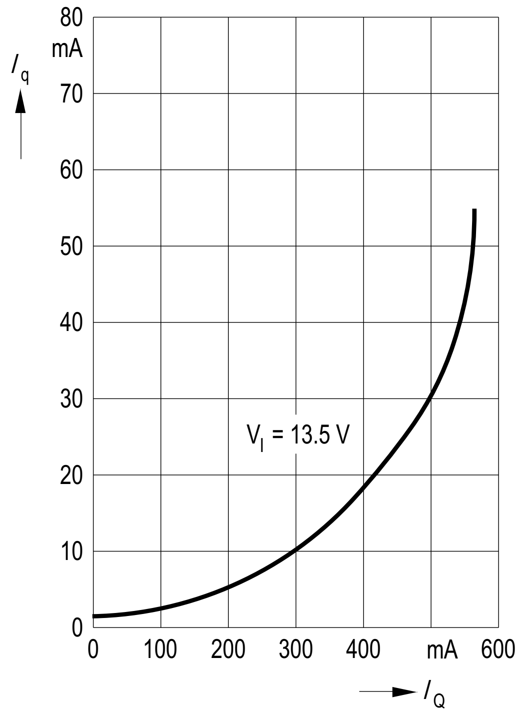
Output current I_Q versus input voltage V_I



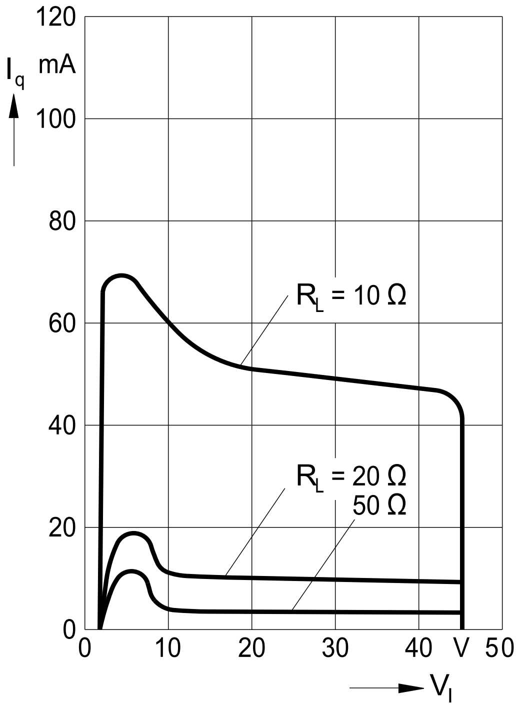
Current consumption I_q versus output current I_Q



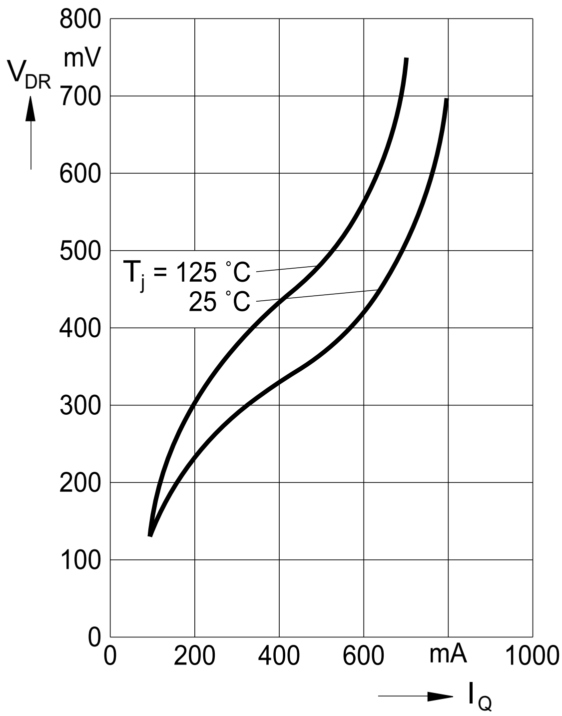
Current consumption I_q versus output current I_Q



Current consumption I_q versus input voltage V_I

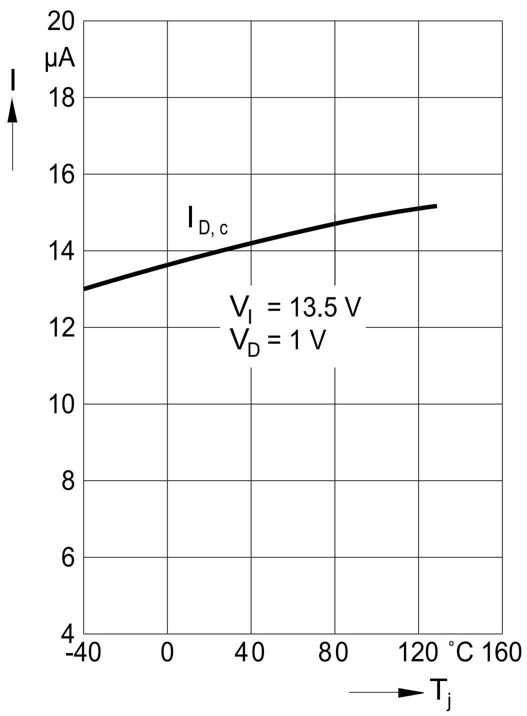


Drop voltage V_{DR} versus output current I_Q

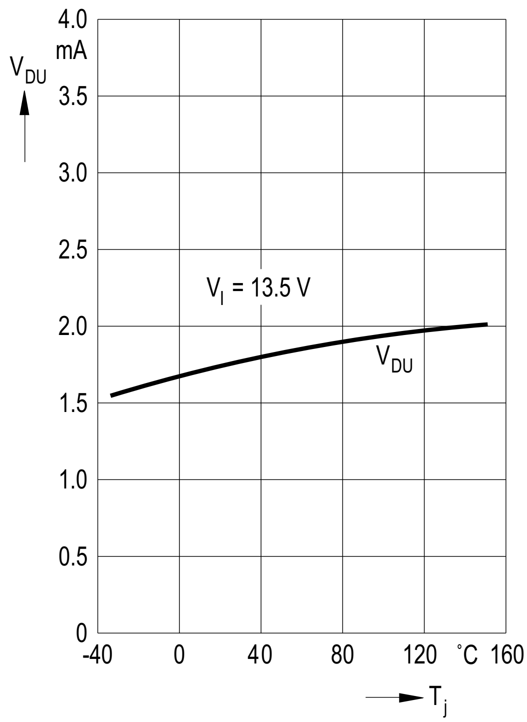


Typical performance characteristics

Charge current $I_{D,c}$ versus junction temperature T_j



Upper reset timing threshold V_{DU} versus junction temperature T_j



5 Application information

The IC regulates an input voltage in the range of V_I = 5.5 V to 36 V to $V_{Q,nom}$ = 5.0 V. Up to 26 V it produces a regulated output current of more than 650 mA. Above 26 V the save-operating-area protection allows operation up to 36 V with a regulated output current of more than 300 mA. Overvoltage protection limits operation at 42 V. The overvoltage protection hysteresis restores operation if the input voltage has dropped below 36 V. A reset signal is generated for an output voltage of V_Q < 4.5 V. The delay for power-on reset can be set externally with a capacitor.

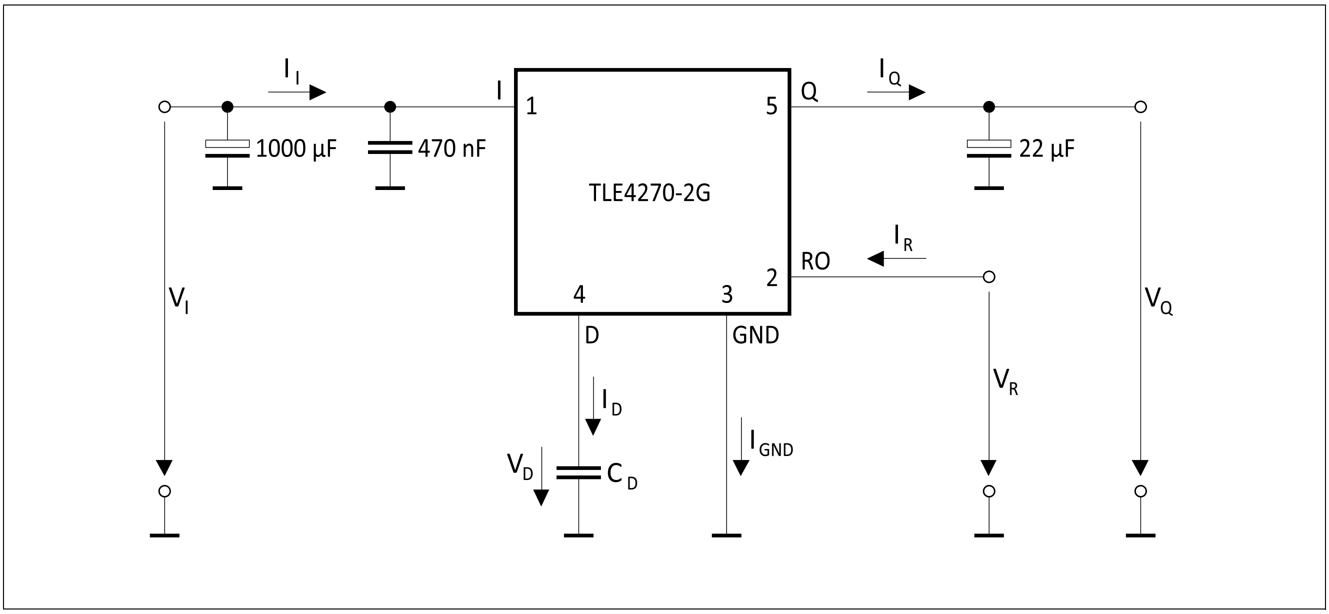


Figure 3 Test circuit

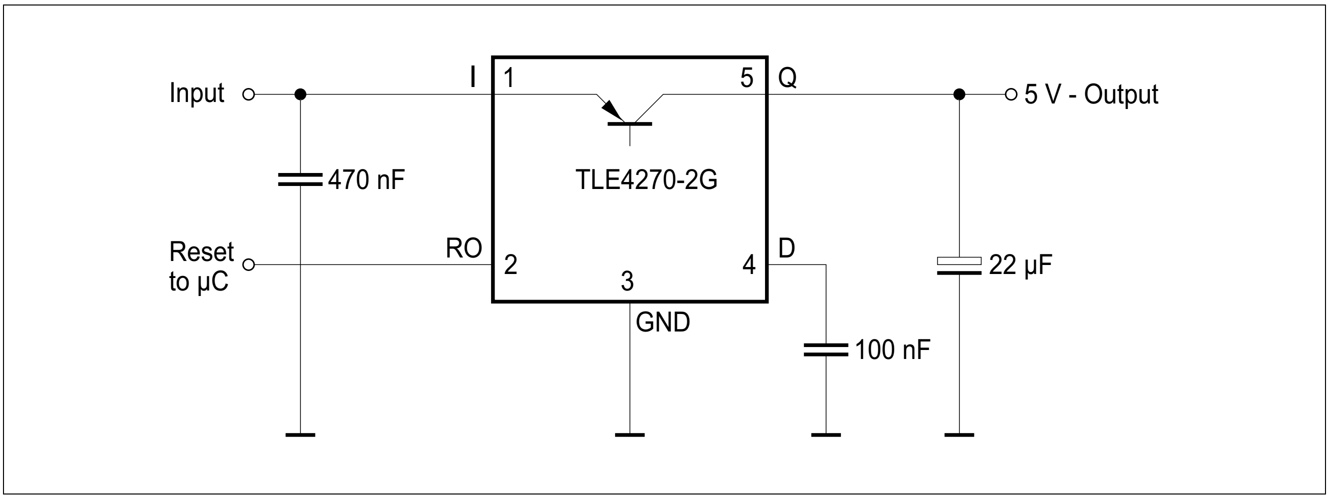


Figure 4 Application circuit

5.1 Design notes for external components

An input capacitor C_I is necessary for compensation of line influences. The resonant circuit consisting of lead inductance and input capacitance can be damped by a resistor of approx. 1 Ω in series with C_I. An output capacitor C_Q is necessary for the stability of the regulating circuit. Stability is guaranteed at values of C_Q ≥ 22 µF and an ESR of < 3 Ω.

5.2 Reset circuitry

If the output voltage decreases below 4.5 V, an external capacitor C_D on pin 4 (D) will be discharged by the reset generator. If the voltage on this capacitor drops below V_{DL}, a reset signal is generated on pin 2 (RO), i.e. reset output is set low. If the output voltage rises above the reset threshold, C_D will be charged with constant current. After the power-on-reset time the voltage on the capacitor reaches V_{DU} and the reset output will be set high again. The value of the power-on-reset time can be set within a wide range depending of the capacitance of C_D.

5.3 Reset timing

The power-on reset delay time is defined by the charging time of an external capacitor C_D which can be calculated as follows:

$$C_D = (\Delta t \times I_{D,c})/\Delta V \tag{5.1}$$

Definitions:

- C_D = delay capacitors
- Δt = reset delay time t_{rd}
- $I_{D,c}$ = charge current, typical 14 µA
- $\Delta V = V_{DU}$, typical 1.8 V

V_{DU} = upper reset timing threshold at C_D for reset delay time

$$t_{rd} = \Delta V \times C_D/I_{D,c} \tag{5.2}$$

The reset reaction time t_{rr} is the time it takes the voltage regulator to set the reset out LOW after the output voltage has dropped below the reset threshold. It is typically 1 µs for delay capacitor of 47 nF. For other values for C_D the reaction time can be estimated using the following equation:

$$t_{rr} \approx 20\ \text{s/F} \times C_D \tag{5.3}$$

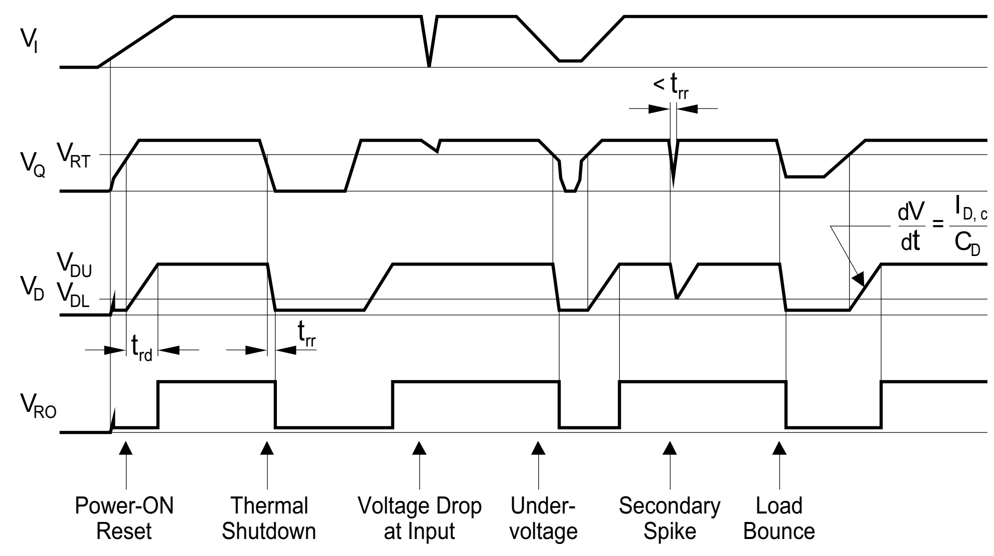
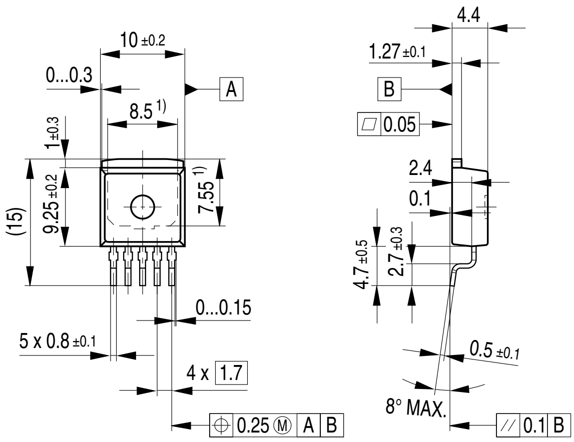


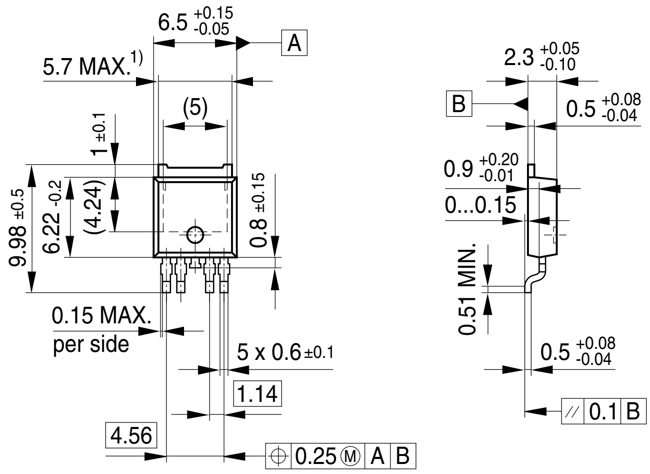
Figure 5 Reset time response

6 Package information



1) Typical
Metal surface min. X = 7.25, Y = 6.9
All metal surfaces tin plated, except area of cut.

Figure 6 PG-TO263-5 (plastic transistor single outline)[1)]



1) Includes mold flashes on each side.
All metal surfaces tin plated, except area of cut.

Figure 7 PG-TO252-5 (plastic transistor single outline)[1)]

Green Product (RoHS-compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a Green Product. Green Products are RoHS-compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

1) Dimensions in mm.

7 Revision history

Version	Date	Changes
1.91	2024-08-20	• Template update and editorial changes • Corrected package reference: P -> PG • Added P_3.1.13
1.9	2020-02-25	Editorial changes, including rearranged content
1.8	2007-11-09	**Page 1**: Changed ESD specification from “>4000V” to “±2 kV HBM” according to PCN No. 2007-08
1.7	2007-03-20	Initial version of RoHS-compliant derivate of TLE 4270. Change of product name to TLE4270-2 due to modified chip layout and size. **Page 1**: AEC certified statement added **Page 1** and **Page 15**: RoHS compliance statement and Green Product feature added **Page 1** and **Page 15**: Package changed to RoHS compliant version Legal Disclaimer updated

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