

Features

- Input Voltage Range: 2.7 V to 5.5V
- Power-Up and Power-Down Sequence Control
- Single Enable Control Signal Input Channel
- Three Power Sequence Channels:
 - ◆ Open-Drain Output
 - ◆ Adjustable Timing Controlled by Capacitor
 - ◆ Support Invert Output
- Support Cascaded Device Output
- Low Power Consumption
- Junction Temperature: -40°C to $+125^{\circ}\text{C}$
- Small MSOP-8 Package

Applications

- Video Surveillance
- Network Equipment and Servers
- Industrial Control
- FPGA/ASIC/CPLD Power Sequence Control
- Multi-channel Power Supply Sequence Control

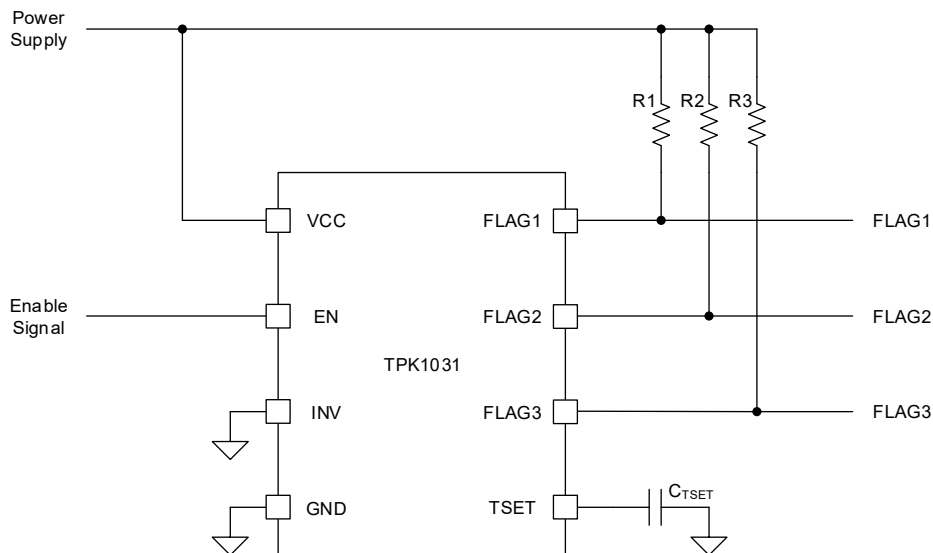
Description

The TPK1031 series products are simple power sequencers, which provide power-up and power-down sequence control of multi-channel power supplies. Furthermore, the TPK1031 series support maximum three devices cascaded to control sequence of nine-channel power rails in one system.

The TPK1031 series products have three open-drain output channels, and all the channels can be pulled up to any required voltage level equal or lower than V_{CC} . When the TPK1031 series are enabled with EN pin goes high, the three output channels toggle with the sequence of FLAG1-FLAG2-FLAG3 after the delay period individually set by the external capacitor; when the TPK1031 series are disabled with EN pin goes low, the three output channels toggle following a reverse sequence after the delay period individually set by the external capacitor.

The TPK1031 series products provide small MSOP-8 package with guaranteed junction temperature range (T_J) from -40°C to $+125^{\circ}\text{C}$.

Typical Application Schematic



Product Family Table

Part Number	Orderable Number	Package	Transport Media, Quantity	MSL	Marking information
TPK1031-S	TPK1031L1-VS1R-S	MSOP-8	3,000	MSL1	K1031

Table of Contents

Features	1
Applications	1
Description	1
Typical Application Schematic	1
Product Family Table	2
Table of Contents	3
Revision History	4
Pin Configuration and Functions	5
Specifications	6
Absolute Maximum Ratings	6
ESD Ratings	6
Recommended Operating Conditions	6
Thermal Information	6
Electrical Characteristics	7
Typical Performance Characteristics	8
Detailed Description	9
Overview	9
Functional Block Diagram	9
Feature Description	9
Application and Implementation	13
Application Information	13
Typical Application	13
Layout Requirements	15
Tape and Reel Information	16
Package Outline Dimensions	17
MSOP-8	17

Revision History

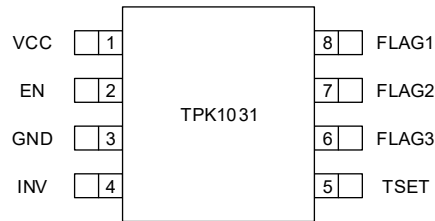
Date	Revision	Notes
2019/05/31	Rev.Pre	Preliminary Version
2019/08/31	Rev.A	Initial Release
2019/12/20	Rev.A.1	Upgrade HBM ESD Ratings to ± 2000 V (Page 6)
2021/07/09	Rev.A.2	1. Correct the Mistake Pin Number of EN from 3 to 2 (Page 5) 2. Add Tape and Reel Information (Page 16)

Pin Configuration and Functions

TPK1031 Series

8-Pin MSOP

Top View



Pin Functions

NAME	PIN NUMBER	TYPE	DESCRIPTION
EN	2	I	Device enable pin.
FLAG1	8	O	Open-drain output pin.
FLAG 2	7	O	Open-drain output pin.
FLAG 3	6	O	Open-drain output pin.
GND	3	—	Ground reference pin.
INV	4	I	Invert output set pin.
TSET	5	O	Delay time set pin.
VCC	1	I	Input power supply.

Specifications

Absolute Maximum Ratings

		MIN	MAX	UNIT
VCC, EN, INV, TSET		-0.3	6	V
FLAG1, FLAG2, FLAG3		-0.3	6	V
T _J	Junction Temperature Range	-40	150	°C
T _{STG}	Storage Temperature Range	-65	150	°C
T _L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond the Absolute Maximum Ratings may permanently damage the device.

(2) All voltage values are with respect to GND.

ESD Ratings

		Condition	Minimum Level	UNIT
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	±2000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	±500	V

Recommended Operating Conditions

		MIN	MAX	UNIT
VCC		2.7	5.5	V
EN, INV, TSET		0	VCC + 0.3	V
FLAG1, FLAG2, FLAG3		0	VCC + 0.3	V
T _J	Junction Temperature Range	-40	125	°C

Thermal Information

PACKAGE	θ _{JA}	θ _{JC}	UNIT
MSOP-8	247	118	°C/W

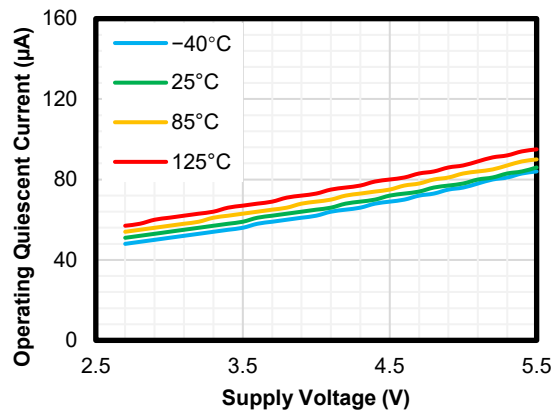
Electrical Characteristics

$T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ (typical value at $T_J = +25^{\circ}\text{C}$), $V_{CC} = 3.3\text{ V}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply						
VCC	Input supply voltage		2.7		5.5	V
ICC	Operating quiescent current	INV = GND		55	100	μA
		INV = VCC		85	130	μA
Enable						
V _{EN_TH}	EN pin threshold voltage		1	1.23	1.5	V
I _{EN}	EN pin pull-up current	V _{EN} = 0 V	5	6.5	8	μA
Open-Drain Output						
V _{OL}	FLAGx pin output low level	I _{FLAGx} = 1.2 mA	0		0.4	V
I _{FLAGx}	FLAGx pin leakage current	V _{FLAGx} = 3.3 V		0.3	1	μA
Delay Time Setup						
I _{TSET_SOURCE}	TSET pin source current		7	11	15	μA
I _{TSET_SINK}	TSET pin sink current		7	11	15	μA
V _{TSET_H}	TSET pin high-level threshold		1	1.14	1.4	V
V _{TSET_L}	TSET pin low-level threshold		0.4	0.5	0.7	V
T _{CLK}	Clock cycle	C _{TSET} = 10 nF	0.9	1.16	1.4	ms
Timing Delays						
t _{d1} , t _{d4}	Timing delays		9		10	Cycles
t _{d2} , t _{d3} , t _{d5} , t _{d6}	Timing delays			8		Cycles
Invert Output Setup						
V _{INV_IH}	Invert pin high-level input		90%			Of VCC
V _{INV_IL}	Invert pin low-level input				10%	Of VCC

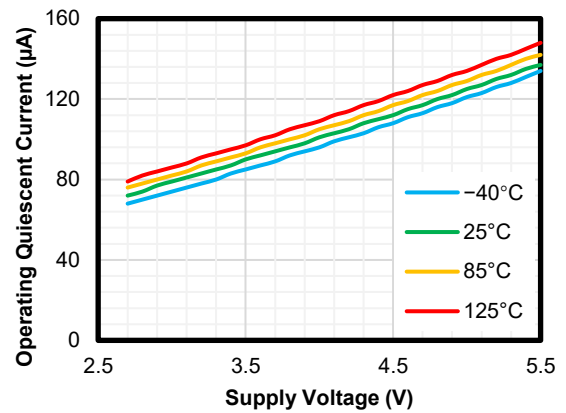
Typical Performance Characteristics

$T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ (typical value at $T_J = +25^{\circ}\text{C}$), $V_{CC} = 3.3\text{ V}$, unless otherwise noted.



INV = GND

Figure 1 Quiescent Current vs Supply Voltage



INV = VCC

Figure 2 Quiescent Current vs Supply Voltage

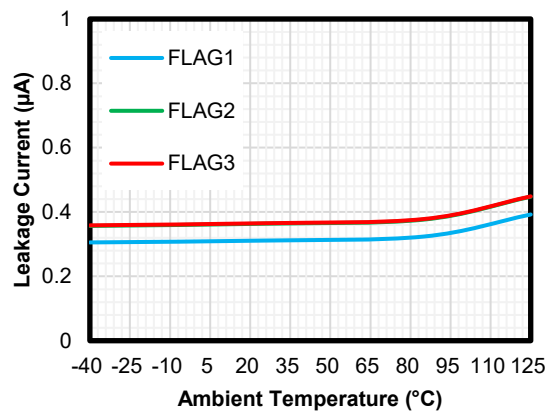


Figure 3 FLAGx Leakage Current vs Temperature

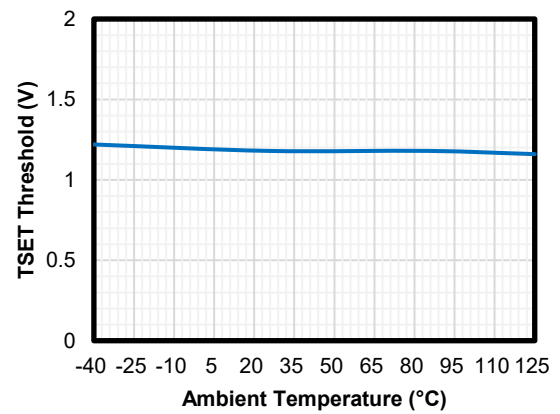
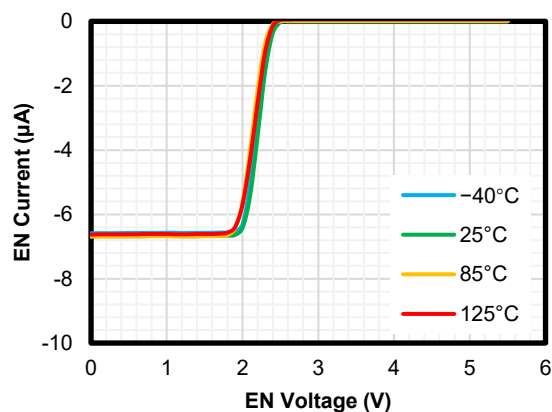
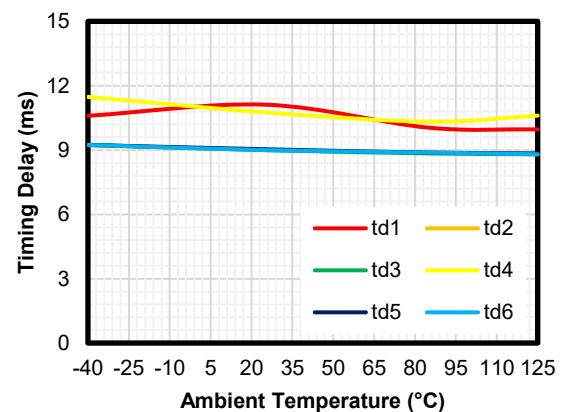


Figure 4 TSET Threshold vs Temperature



INV = GND

Figure 5 EN Input Current vs EN Voltage



$C_{TSET} = 10\text{ nF}$

Figure 6 Timing Delay vs Temperature

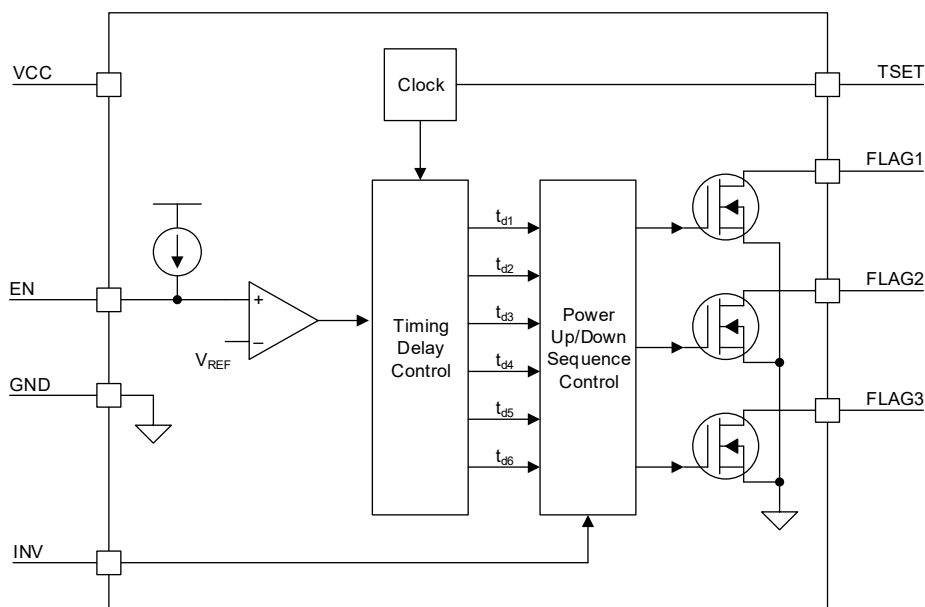
Detailed Description

Overview

The TPK1031 series products are simple power sequencers, which provide power-up and power-down sequence control of multi-channel power supplies. Furthermore, the TPK1031 series support maximum three devices cascaded to control sequence of nine-channel power rails in one system.

The TPK1031 series products have three open-drain output channels, and all the channels can be pulled up to any required voltage level equal or lower than V_{CC} . When the TPK1031 series are enabled with EN pin goes high, the three output channels toggle with the sequence of FLAG1-FLAG2-FLAG3 after the delay period individually set by the external capacitor; when the TPK1031 series are disabled with EN pin goes low, the three output channels toggle following a reverse sequence after the delay period individually set by the external capacitor.

Functional Block Diagram



Feature Description

Device Enable (EN)

The timing sequence of TPK1031 series is controlled by the enable (EN) signal. An internal comparator connected at EN pin, with referenced to the bandgap voltage, set the enable threshold precisely at 1.23 V. With this precision enable threshold, the TPK1031 series can be enabled after a certain delay period set by external capacitor or a certain voltage value determined by external resistor divider.

3-Channel Simple Power Sequencer with Adjustable Timing Control

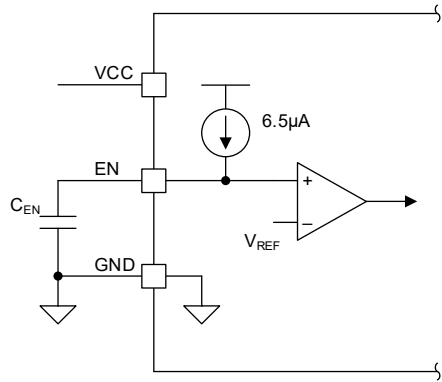


Figure 7 Using Capacitor at EN

When using a capacitor at the EN pin (Figure 7), the enable delay period can be calculated by Equation 1:

$$t_{EN_DLY} = \frac{1.23V \times C_{EN}}{6.5\mu A} \quad (1)$$

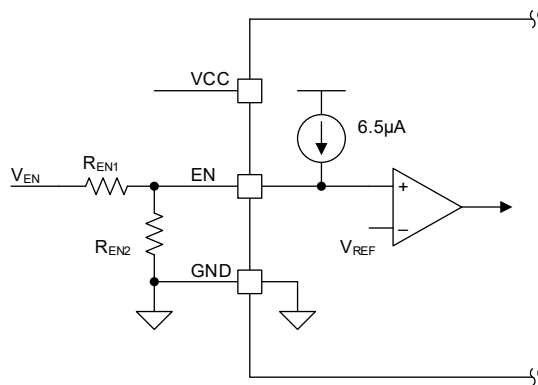


Figure 8 Using Resistor Divider at EN

When using the resistor divider at the EN pin (Figure 8), the resistor divider can be calculated by Equation 2:

$$V_{EN} = V_{EN_TH} \times \frac{R_{EN1} + R_{EN2}}{R_{EN2}} - 6.5\mu A \times R_{EN1} \quad (2)$$

The TPK1031 series also implement the EN pin de-glitch function. When there are ripple across the enable threshold at the EN pin, the device will always reset if the EN pin falls below the threshold. The timing delay only start counting at the last EN rising threshold (Figure 9).

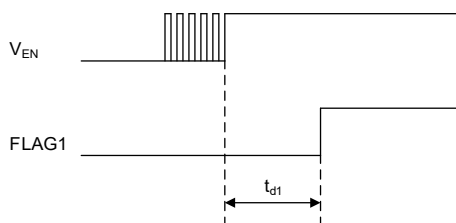


Figure 9 Enable De-glitch (INV = Low)

Inverted Output (INV)

The voltage level of TPK1031 series output flags is selectable HIGH or LOW by setting the INV voltage.

When INV = LOW,

- Output flags turn to HIGH sequentially after each timing delay period when the device enable signal comes.
- Output flags turn to LOW sequentially after each timing delay period when the device disable signal comes.

When INV = HIGH,

- Output flags turn to LOW sequentially after each timing delay period when the device enable signal comes.
- Output flags turn to HIGH sequentially after each timing delay period when the device disable signal comes.

Adjustable Timing Delay

The delay period between TPK1031 series output flags is adjustable with a small external capacitor C_{TSET} at T_{SET} pin. The T_{SET} pin charges/discharges the capacitor C_{TSET} with about $\pm 11 \mu A$ source/sink current, I_{TSET_SOURCE} and I_{TSET_SINK} , between voltage threshold V_{TSET_H} and V_{TSET_L} . The charging period, T_{CHG} , and discharging period, T_{DISCHG} , compose one delay clock cycle, T_{CLK} .

Figure 10 shows the delay clock cycle timing waveform.

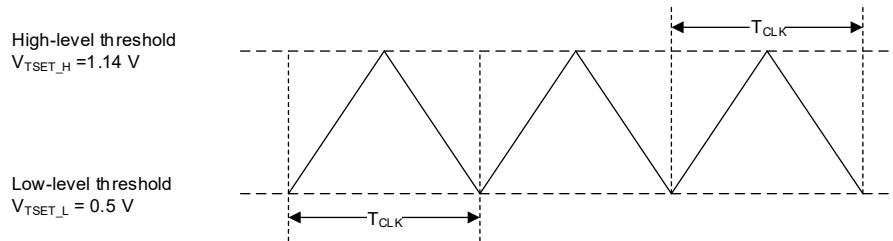


Figure 10 Delay Clock Cycle Timing Waveform

The delay clock period can be calculated by Equation 3:

$$T_{CLK} = \left(\frac{V_{TSET_H} - V_{TSET_L}}{I_{TSET_SOURCE}} + \frac{V_{TSET_H} - V_{TSET_L}}{I_{TSET_SINK}} \right) \times C_{TSET} \quad (3)$$

Power Sequence (FLAGx)

When the TPK1031 series devices are enabled, all the output flags will be released sequentially. The timing delay period between two adjacent flags is determined by the product of each delay clock period and the internal delay clock counter.

Figure 11 and Figure 12 show the power sequences of the output flags.

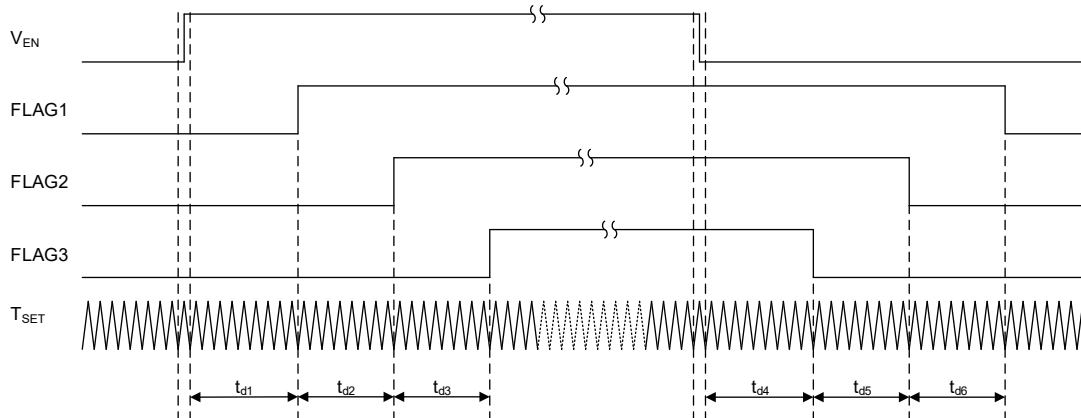


Figure 11 Power Up and Power Down Sequence when INV = LOW

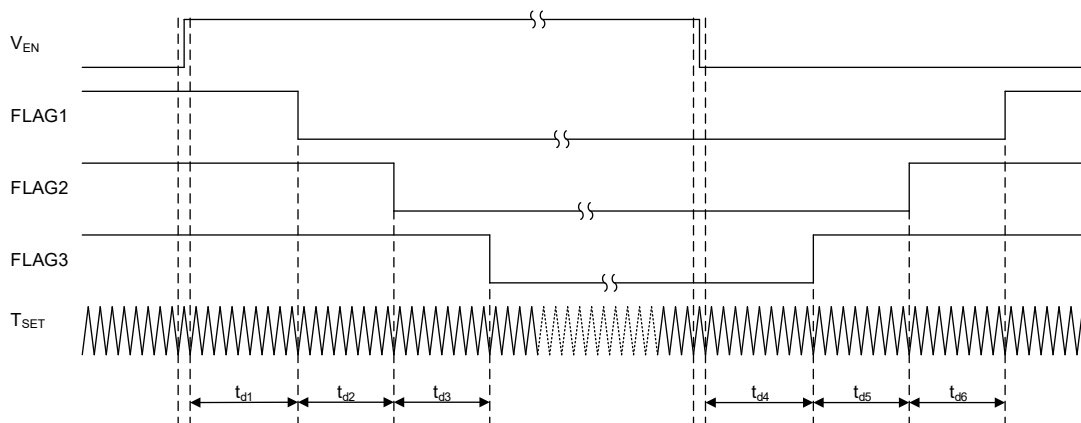


Figure 12 Power Up and Power Down Sequence when INV = HIGH

Power Sequence Interruption

When the enable signal keeps constant during the entire power up or power down sequence, the TPK1031 series devices will operate the whole sequence as shown in Figure 11 and Figure 12. However, if the enable signal falling or rising edge comes during the power up or power down sequence, the device will enter the interrupt status and initialize a new power down or power up sequence.

Figure 13 shows the power sequence with EN interruption when INV is LOW.

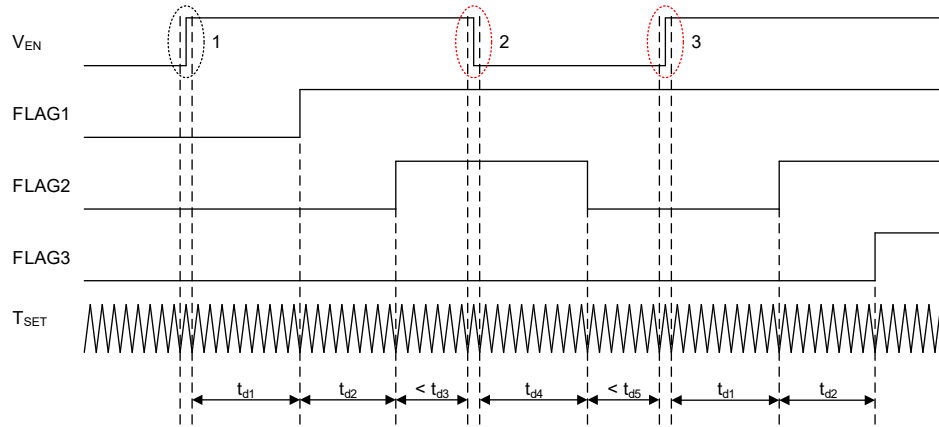


Figure 13 Power Sequence Interruption when INV = LOW

Notes:

1. Device enable signal
2. Enable interrupt during the power up sequence
3. Enable interrupt during the power down sequence

Application and Implementation

NOTE

Information in the following applications sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPK1031 series products are 3-channel simple power sequencers, which provide power-up and power-down sequence control of multi-channel power supplies. The following application schematic shows a typical usage of the TPK1031 series.

Typical Application

Figure 14 and Figure 15 shows the typical application schematic of the TPK1031 series.

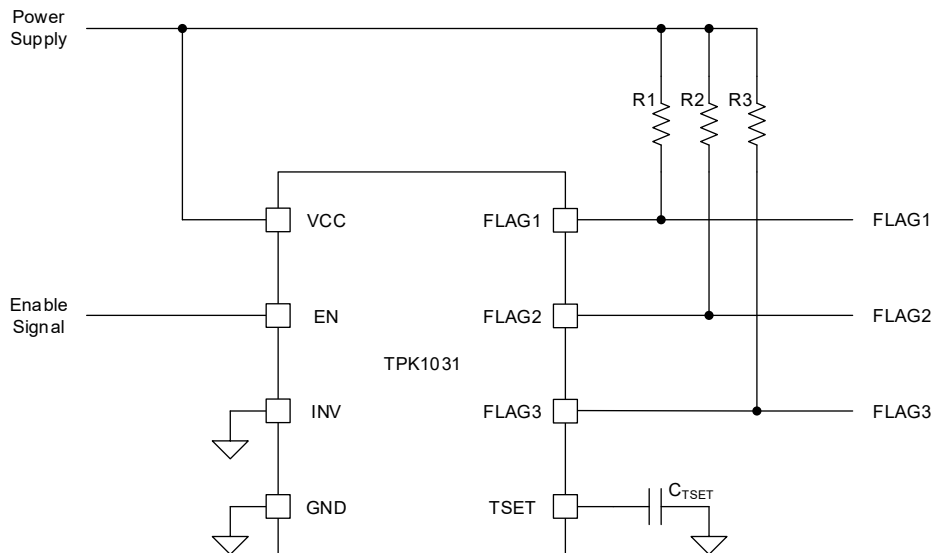


Figure 14 VCC and FLAGx with Same Power Rail

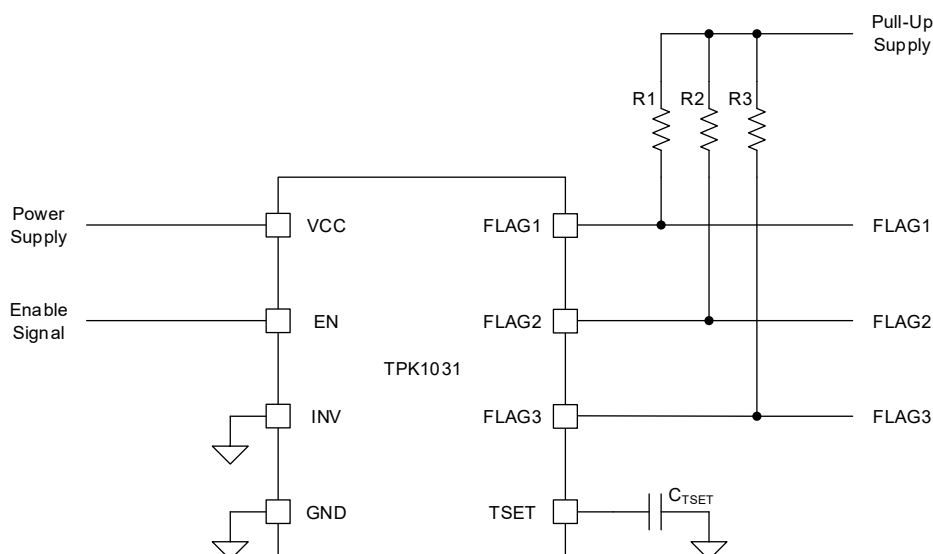


Figure 15 VCC and FLAGx with Different Power Rails

Design Parameters

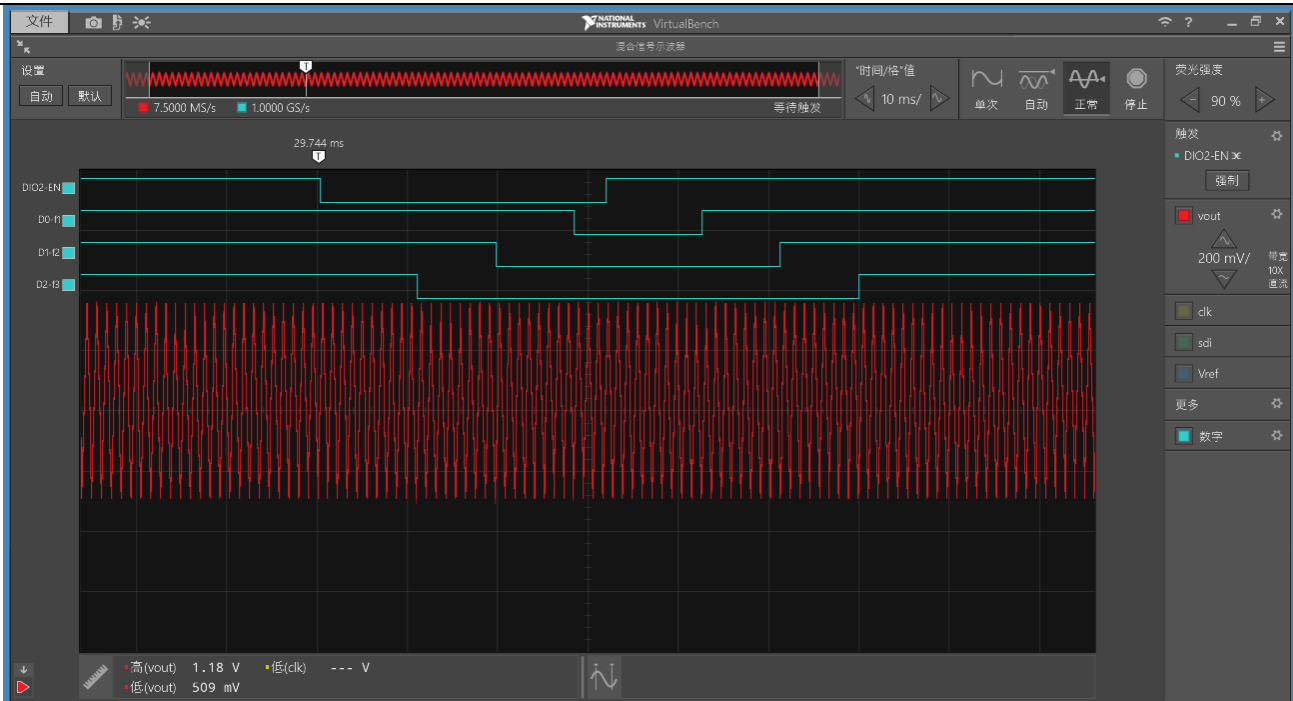
For this design example, use the parameters listed in Table 1.

Table 1 Design Parameters

PARAMETERS	VALUE
Power supply voltage range, VCC	2.7 V to 5.5 V
Enable signal voltage	LOW (< 10% of VCC), HIGH (>90% of VCC)
Pull-up resistors, R1, R2, R3	100 kΩ
Timing delay capacitor, C _{TSET} ⁽¹⁾	10 nF
t _{d1} , t _{d4} ⁽¹⁾	10.44 ms to 11.60 ms
t _{d2} , t _{d3} , t _{d6} , t _{d6} ⁽¹⁾	9.28 ms

(1) See [Adjustable Timing Delay](#) section for more details

Application Waveform



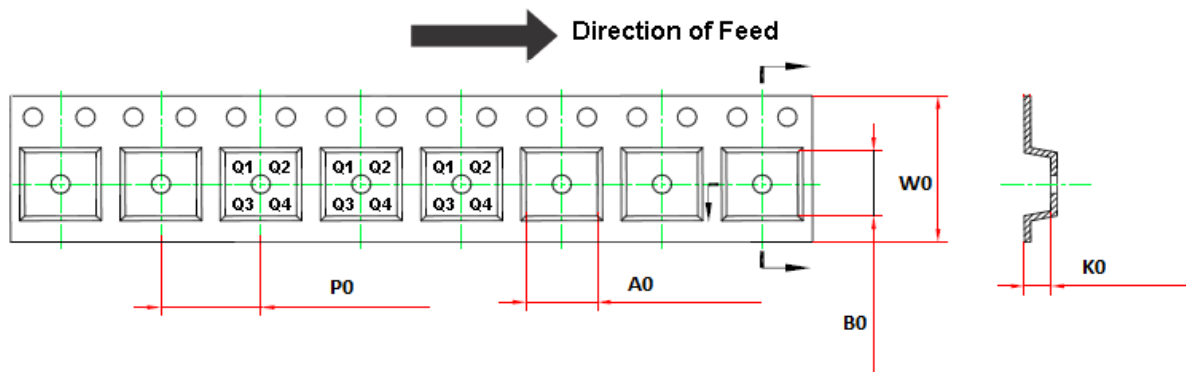
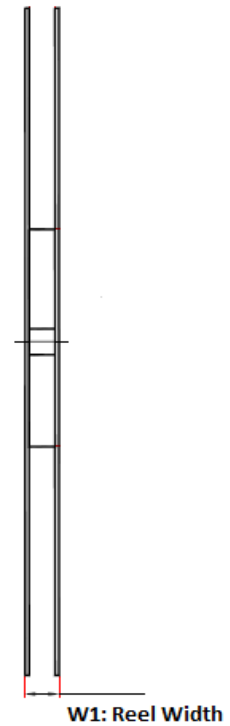
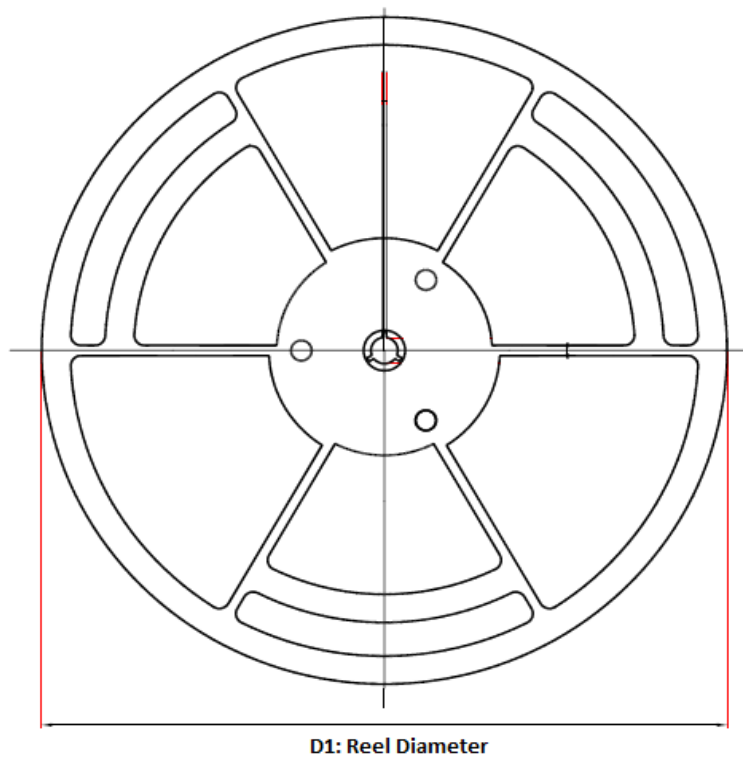
INV = GND

Figure 16 Power Up and Power Down Sequence

Layout Requirements

- FLAGx pull-up resistors, recommended 100 k Ω , should be placed closely to the flag output pins and the pull-up power supply. The traces should be equal to each other, and the trace length should be as short as possible.
- Timing delay capacitor should be placed as close as possible to the TSET pin, and straight trace without via is recommended.

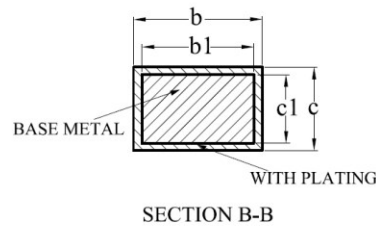
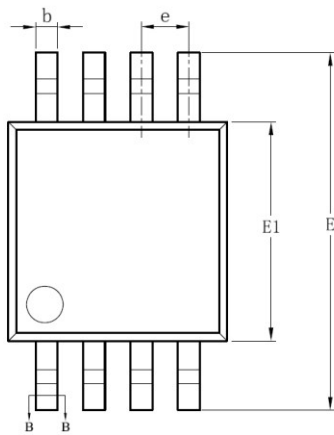
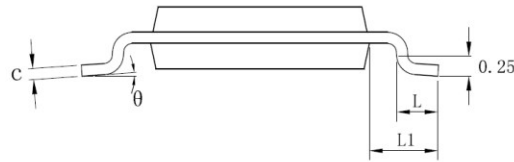
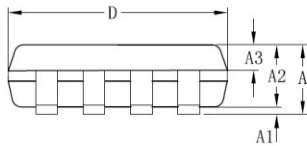
Tape and Reel Information



Order Number	Package	D1	W1	A0	B0	K0	P0	W0	Pin1 Quadrant
TPK1031L1-VS1R-S	MSOP-8	330	17.6	5.2	3.3	1.5	8	12	Q1

Package Outline Dimensions

MSOP-8



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.10
A1	0.05	—	0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.28	—	0.36
b1	0.27	0.30	0.33
c	0.15	—	0.19
c1	0.14	0.15	0.16
D	2.90	3.00	3.10
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
e	0.65BSC		
L	0.40	—	0.70
L1	0.95REF		
θ	0	—	8°