3-Channel Simple Power Sequencer

Features

- Input Voltage Range: 2.5 V to 5.5V
- Power-up and Power-down Sequence Control
- Single Enable Control Signal Input Channel
- Three Power Sequence Channels:
  - Open-Drain Output
  - Selectable Timing Options
  - Selectable Power-down Sequence Options
- Support Cascaded Device Output
- Low Power Consumption
- Junction Temperature: −40°C to +125°C
- Small SOT23-6 Package

Applications

- Video Surveillance
- Network Equipment and Servers
- Industrial Control
- FPGA/ASIC/CPLD Power Sequence Control
- Power Supply Sequence Control

Description

The TPK1032 series of products is a simple power sequencer, which provides power-up and power-down sequence control of multi-channel power supplies. Furthermore, the TPK1032 series supports a maximum of three devices cascaded to control the sequence of nine-channel power rails in one system.

The TPK1032 series of products has three open-drain output channels, and all the channels can be pulled up to any required voltage level equal to or lower than V_{CC}. When the TPK1032 series is enabled and the EN pin goes high, the three output channels turn to high with the sequence of FLAG1-FLAG2-FLAG3 after the selected delay period individually. When the TPK1032 series is disabled and the EN pin goes low, the three output channels turn low one by one with the selected sequence after the selected delay period individually.

The TPK1032 series of products provides a SOT23-6 package with a guaranteed junction temperature range (T_J) from −40°C to +125°C.

Typical Application Circuit

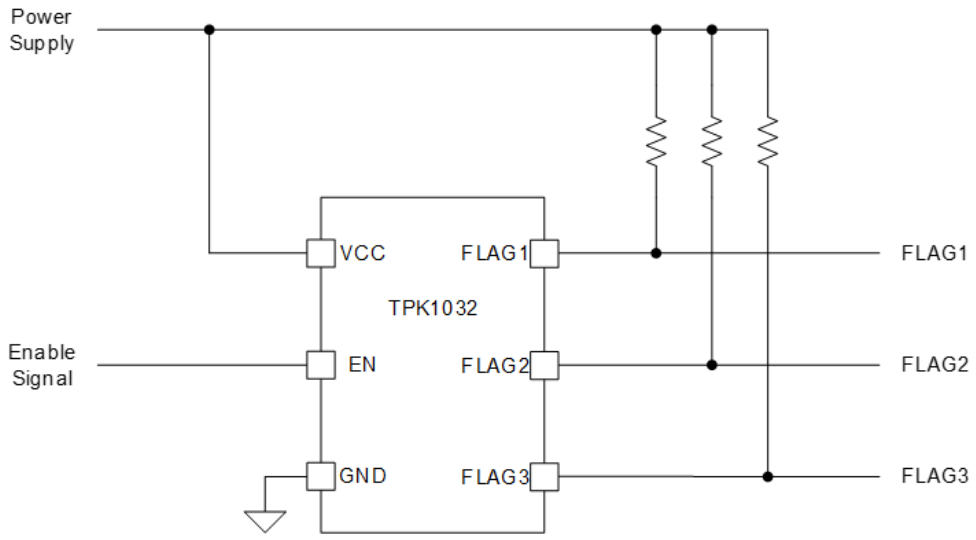


Table of Contents

Product Family Table

Order Number	Package	Marking Information	MSL	Transport Media, Quantity
TPK1032AAL1-S6TR	SOT23-6	KAA	1	Tape and Reel, 3000
TPK1032ABL1-S6TR (1)	SOT23-6	KAB	1	Tape and Reel, 3000
TPK1032ACL1-S6TR (1)	SOT23-6	KAC	1	Tape and Reel, 3000
TPK1032ADL1-S6TR (1)	SOT23-6	KAD	1	Tape and Reel, 3000
TPK1032AEL1-S6TR	SOT23-6	KAE	1	Tape and Reel, 3000
TPK1032AFL1-S6TR	SOT23-6	KAF	1	Tape and Reel, 3000

(1) For future products, contact the 3PEAK factory for more information and samples.

TPK1032 X Y L1-S6TR

X: Sequence Designator

Designator	Power-up Sequence	Power-down Sequence
A	FLAG1 – FLAG2 – FLAG3	FLAG3 – FLAG2 – FLAG1
B	FLAG1 – FLAG2 – FLAG3	FLAG3 – FLAG1 – FLAG2
C	FLAG1 – FLAG2 – FLAG3	FLAG2 – FLAG3 – FLAG1
D	FLAG1 – FLAG2 – FLAG3	FLAG2 – FLAG1 – FLAG3
E	FLAG1 – FLAG2 – FLAG3	FLAG1 – FLAG3 – FLAG2
F	FLAG1 – FLAG2 – FLAG3	FLAG1 – FLAG2 – FLAG3

Y: Delay Designator

Designator	t_{D1} (ms)	t_{D2} (ms)	t_{D3} (ms)	t_{D4} (ms)	t_{D5} (ms)	t_{D6} (ms)
A	11	11	11	11	11	11
B	30	30	30	30	30	30
C	60	60	60	60	60	60
D	120	120	120	120	120	120
E	2.2	2.2	2.2	2.2	2.2	2.2
F	18	18	18	18	18	18

Revision History

Date	Revision	Notes
2019-05-31	Rev.Pre.0	Preliminary version.
2019-08-31	Rev.A.0	Initial released version.
2022-07-29	Rev.A.1	Updated the t_d ratio in the EC table.
2023-08-09	Rev.A.2	Updated delay time of E version to 2.2ms, F version to 18ms. Updated to the latest datasheet version. Added tape and reel information. Updated HBM ESD rating to ±2000V. Added footprint information.

Pin Configuration and Functions

TPK1032 Series
SOT23-6
Top View

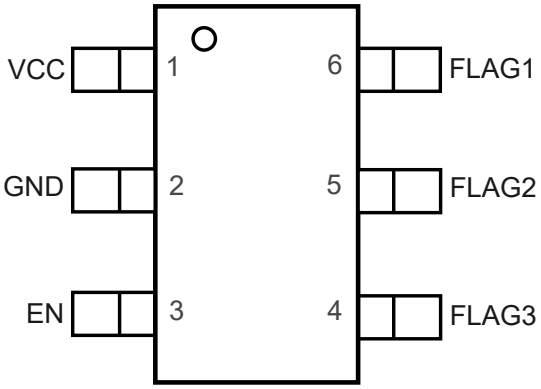


Table 1. Pin Functions

Pin No.	Name	I/O	Description
3	EN	I	The enable pin of the device.
6	FLAG1	O	The open-drain output pin.
5	FLAG2	O	The open-drain output pin.
4	FLAG3	O	The open-drain output pin.
2	GND		The ground reference pin.
1	VCC	I	The input power supply.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
	V_{CC}, EN	−0.3	6	V
	FLAG1, FLAG2, FLAG3	−0.3	6	V
T_J	Maximum Operating Junction Temperature	−40	150	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering, 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
(2) All voltage values are with respect to GND.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Max	Unit
V_{CC}		2.7	5.5	V
EN		0	V_{CC} + 0.3	V
FLAG1, FLAG2, FLAG3		0	V_{CC} + 0.3	V
T_J	Junction Temperature Range	−40	125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOT23-6	206	140	°C/W

Electrical Characteristics

All test conditions: T_J = −40℃ to +125℃ (typical value at T_J = +25℃), V_{CC} = 3.3 V, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power Supply						
V_{CC}	Input Supply Voltage		2.5		5.5	V
I_{CC}	Operating Quiescent Current			55	100	μA
Enable						
V_{EN_TH}	EN Pin Threshold Voltage		1	1.23	1.5	V
I_{EN}	EN Pin Pull-up Current	V_{EN} = 0 V	5	6.5	8	μA
Open-Drain Output						
V_{OL}	FLAGx Pin Output Low Level	I_{FLAGx} = 1.2 mA	0		0.4	V
I_{FLAGx}	FLAGx Pin Leakage Current	V_{FLAGx} = 3.3 V		0.3	1	μA
Power-up Sequence						
t_{d1}	Timer Delay 1 Tolerance	All other timing options	−15%		15%	
		2-ms timing option	−20%		20%	
t_{d2}	Timer Delay 2 Tolerance	All other timing options	−15%		15%	
		2-ms timing option	−20%		20%	
t_{d3}	Timer Delay 3 Tolerance	All other timing options	−15%		15%	
		2-ms timing option	−20%		20%	
Power-down Sequence						
t_{d4}	Time Delay 4 Tolerance	All other timing options	−15%		15%	
		2-ms timing option	−20%		20%	
t_{d5}	Time Delay 5 Tolerance	All other timing options	−15%		15%	
		2-ms timing option	−20%		20%	
t_{d6}	Time Delay 6 Tolerance	All other timing options	−15%		15%	
		2-ms timing option	−20%		20%	
Inverting Output Setup						
$\frac{t_{dx} - 70\ \mu s}{t_{dx+1}}$	Ratio of Timing Delays	For x = 1 or 4, 2-ms timing option	90%		110%	
$\frac{t_{dx} - 400\mu s}{t_{dx+1}}$	Ratio of Timing Delays	For x = 1 or 4, all other timing options	95%		105%	
$\frac{t_{dx}}{t_{dx+1}}$	Ratio of Timing Delays	For x = 2 or 5	95%		105%	

Typical Performance Characteristics

All test conditions: T_J = −40℃ to +125℃ (typical value at T_J = +25℃), V_{CC} = 3.3 V, Delay = 10 ms, unless otherwise noted.

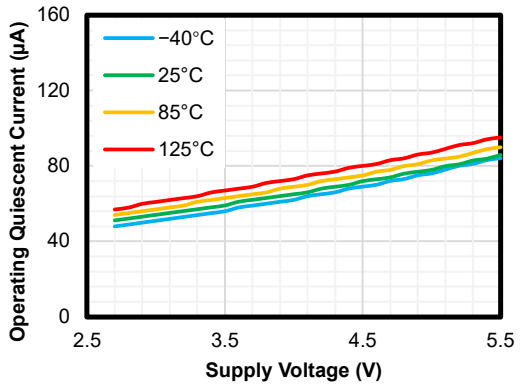


Figure 1. Quiescent Current vs. Supply Voltage

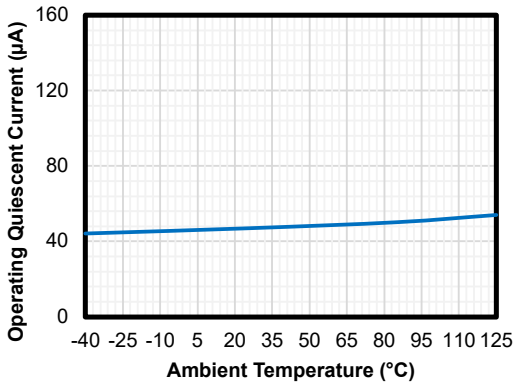


Figure 2. Quiescent Current vs. Temperature

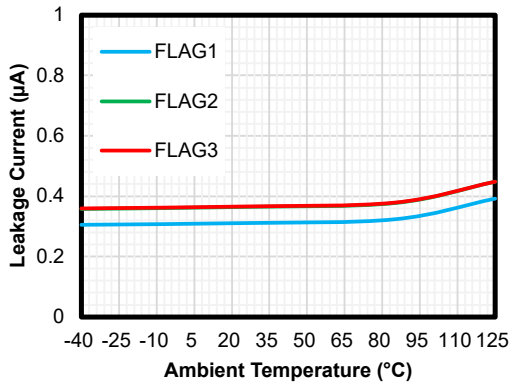


Figure 3. FLAGx Leakage Current vs. Temperature

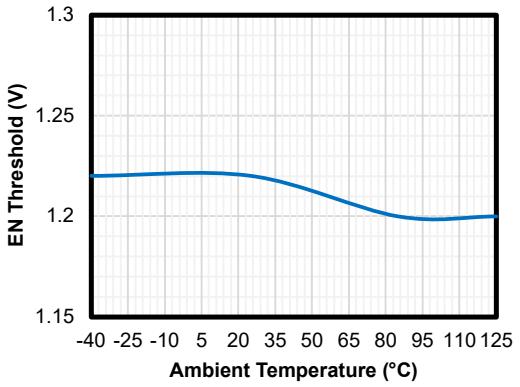


Figure 4. Enable Threshold vs. Temperature

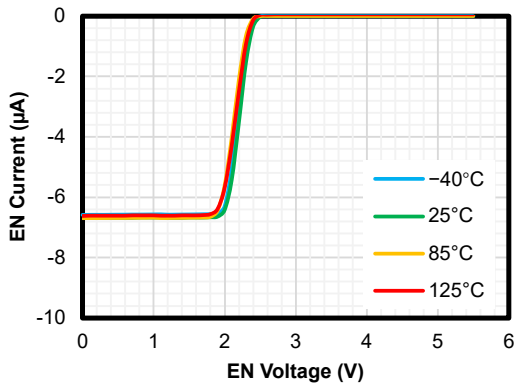


Figure 5. EN Input Current vs. EN Voltage

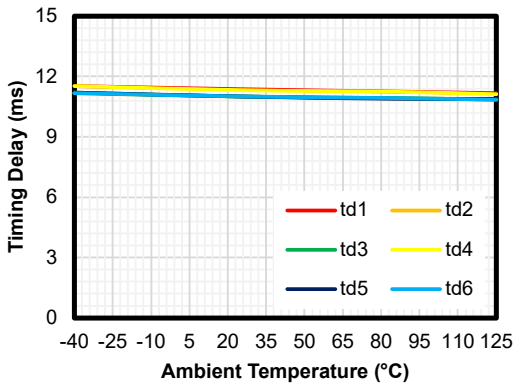


Figure 6. Timing Delay vs. Temperature

Detailed Description

Overview

The TPK1032 series of products is a simple power sequencer, which provides power-up and power-down sequence control of multi-channel power supplies. Furthermore, the TPK1032 series supports a maximum of three devices cascaded to control the sequence of nine-channel power rails in one system.

The TPK1032 series of products has three open-drain output channels, and all the channels can be pulled up to any required voltage level equal to or lower than V_{CC}. When the TPK1032 series is enabled and the EN pin goes high, the three output channels turn to high with the sequence of FLAG1-FLAG2-FLAG3 after the selected delay period individually. When the TPK1032 series is disabled and the EN pin goes low, the three output channels turn low one by one with the selected sequence after the selected delay period individually.

Functional Block Diagram

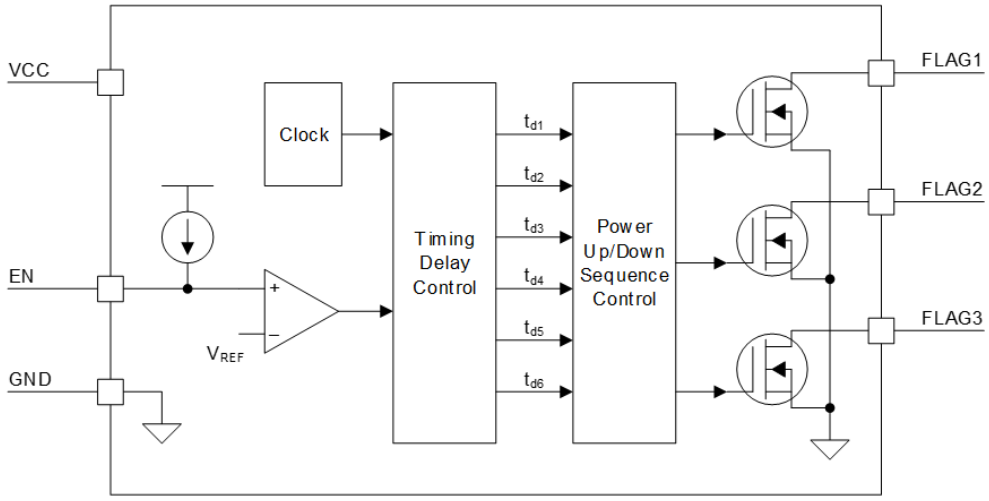


Figure 7. Functional Block Diagram

Feature Description

Enable (EN)

The timing sequence of the TPK1032 series is controlled by the enable (EN) signal. When the device powers up, all the flags keep low until the EN pin is pulled high. An internal comparator, with the reference voltage connected at the negative terminal, sets the enable threshold precisely at 1.22 V. When the EN pin voltage is higher than the threshold, the power-up sequence starts.

With the precision enable threshold, the TPK1032 series can be enabled after a certain delay period set by an external capacitor or a certain voltage value determined by an external resistor divider.

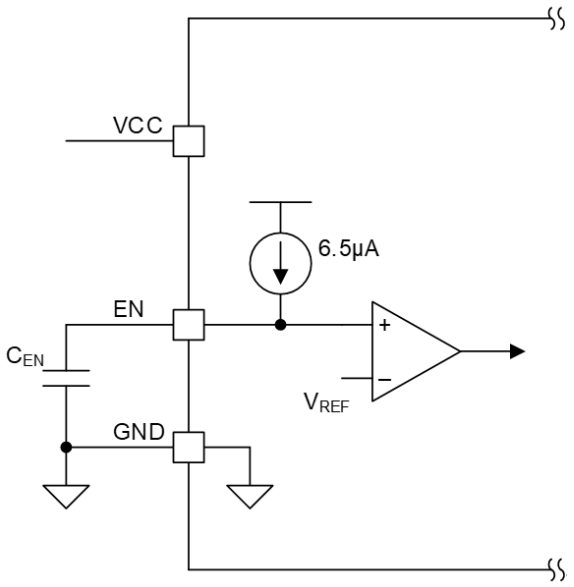


Figure 8. Using Capacitor at EN

Note: It is not recommended to connect EN to V_{CC} directly. EN should be kept low before V_{CC} is ready.

When using a capacitor at the EN pin (Figure 8), the enable delay period can be calculated by Equation 1.

$$t_{EN\_DLY} = \frac{1.23\ V \times C_{EN}}{6.5\ \mu A} \quad (1)$$

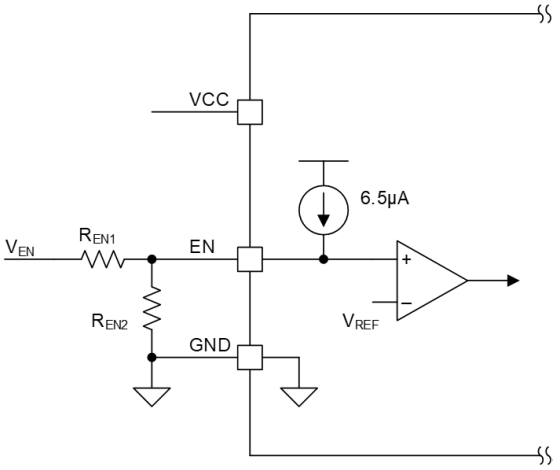


Figure 9. Using Resistor Divider at EN

When using the resistor divider at the EN pin (Figure 9), the resistor divider can be calculated by Equation 2.

$$V_{EN} = V_{EN\_TH} \times \frac{R_{EN1} + R_{EN2}}{R_{EN2}} - 6.5\ \mu A \times R_{EN1} \quad (2)$$

The TPK1032 series also implements the EN pin de-glitch function. When there are ripples across the enable threshold at the EN pin, the device always resets if the EN pin falls below the threshold. The timing delay only starts counting at the last EN rising threshold (Figure 10).

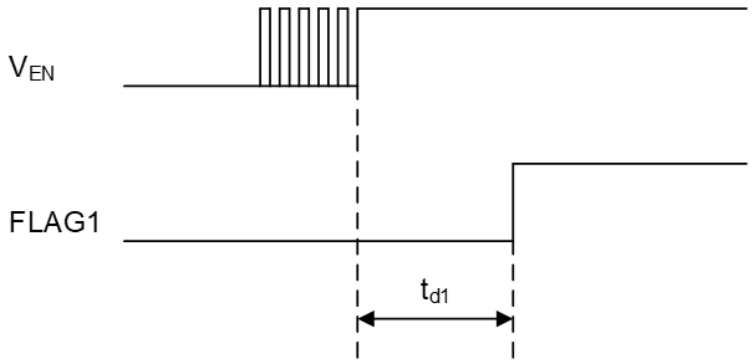


Figure 10. Enable De-glitch

Power Sequence (FLAGx)

When the TPK1032 series of devices is enabled, all the output flags are released sequentially. The timing delay period between two adjacent flags is determined by the internal delay periods of the device.

Figure 11 shows the power sequences of the output flags.

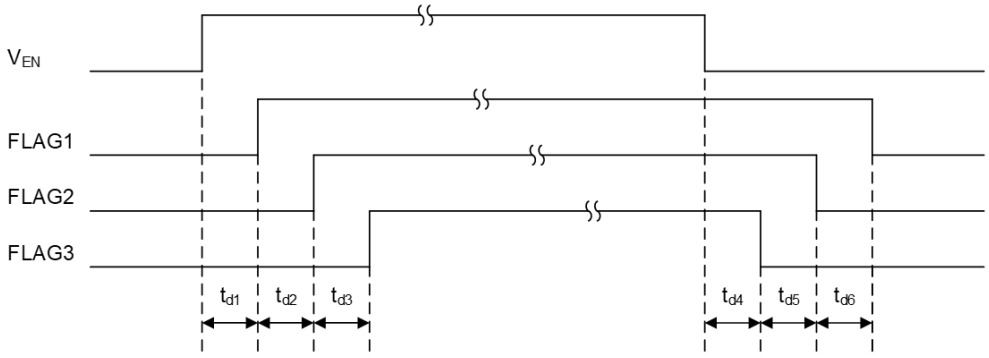


Figure 11. Power Up and Power Down Sequence

Power Sequence Interruption

When the enable signal keeps constant during the entire power-up or power-down sequence, the TPK1032 series operates the whole sequence as shown in Figure 11. However, if the enable signal falling or rising edge comes during the power up or power down sequence, the device enters the interrupt status and initializes a new power down or power up sequence.

Figure 12 shows the power sequence with EN interruption.

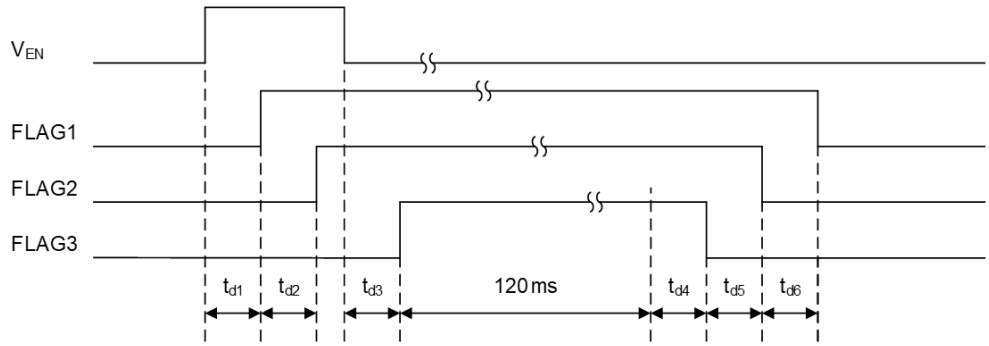


Figure 12. Interrupt of Power up Sequence

Figure 13 shows the power-down sequence with EN interruption.

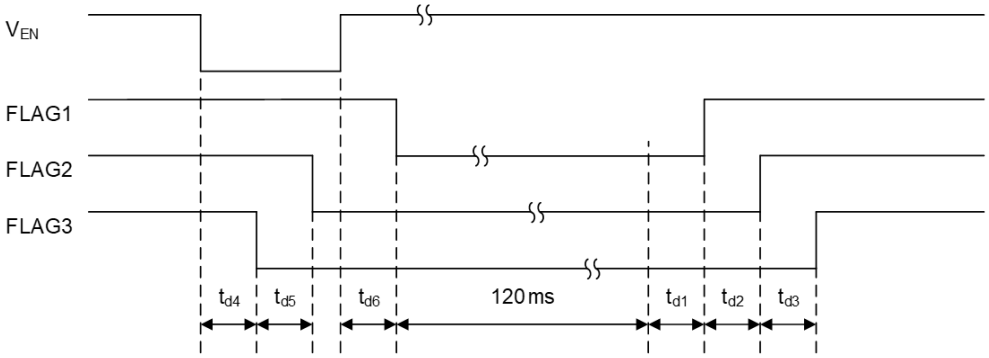


Figure 13. Interrupt of Power Down Sequence

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPK1032 series is a 3-channel simple power sequencer, which provides power-up and power-down sequence control of multi-channel power supplies. The following application schematic shows a typical usage of the TPK1032 series.

Typical Application

Figure 14 and Figure 15 shows the typical application schematic of the TPK1032 series.

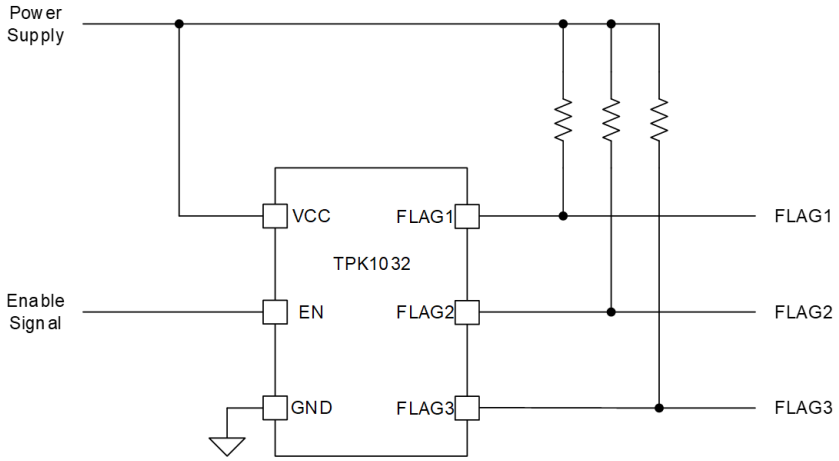


Figure 14. V_{CC} and FLAGx with the Same Power Rail

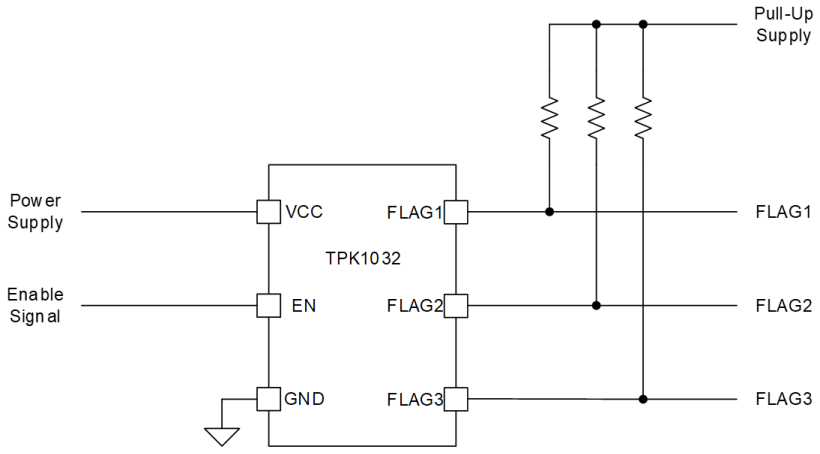


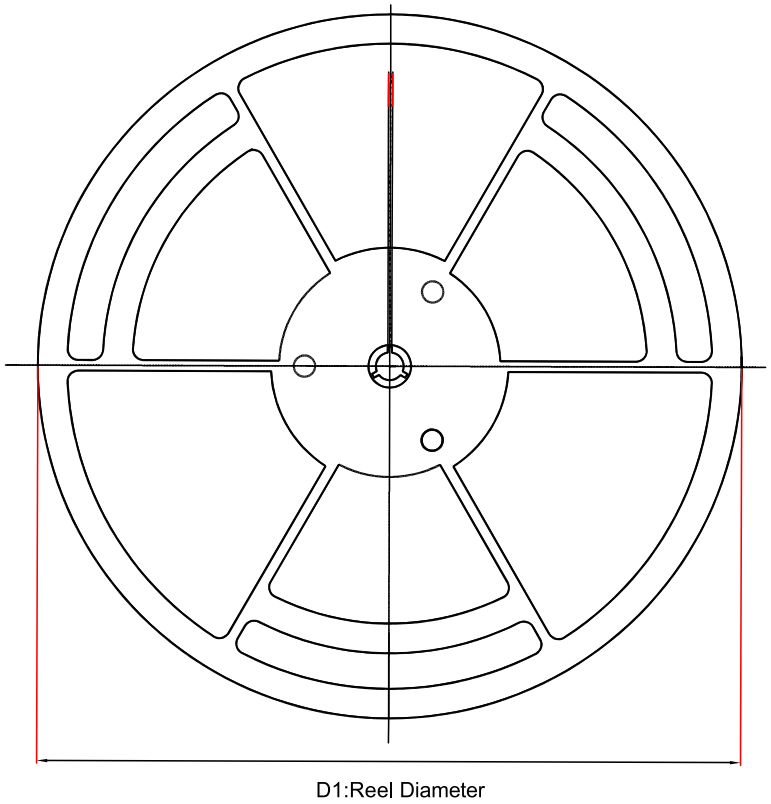
Figure 15. V_{CC} and FLAGx with Different Power Rails

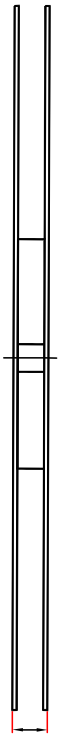
Layout

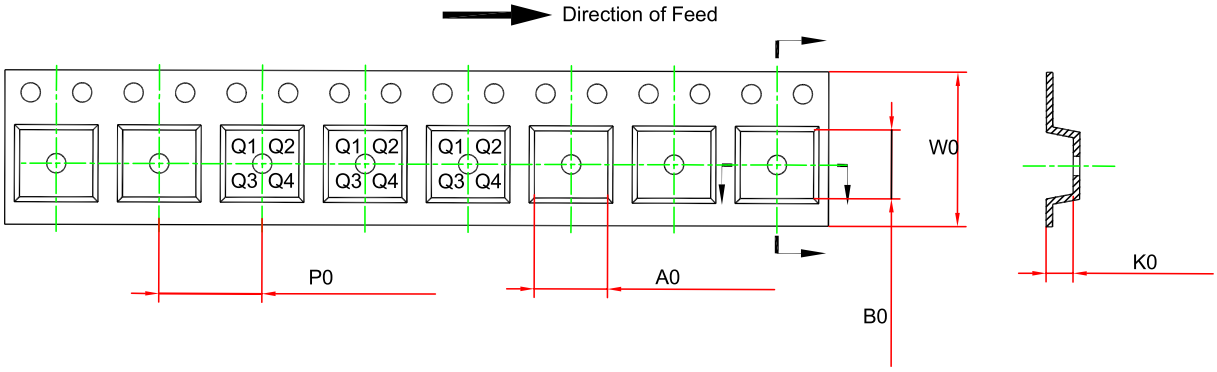
Layout Requirements

- The FLAGx pull-up resistors, recommended 100 kΩ, should be placed close to the flag output pins and the pull-up power supply. The traces should be equal to each other, and the trace length should be as short as possible.

Tape and Reel Information





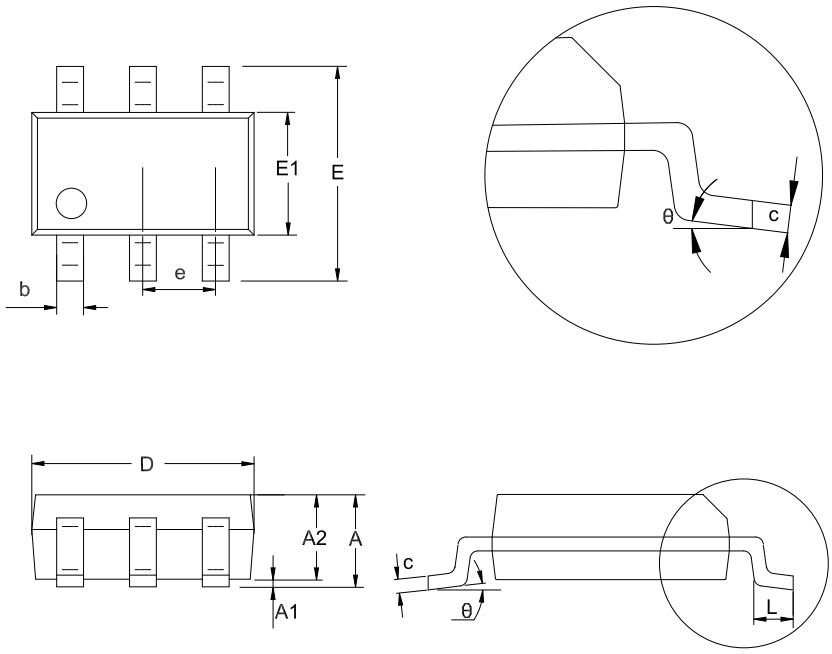


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPK1032AxL1-S6TR	SOT23-6	180	12	3.3	3.2	1.4	4	8	Q3

Package Outline Dimensions

SOT23-6

Package Outline Dimensions S6T(SOT23-6-A)

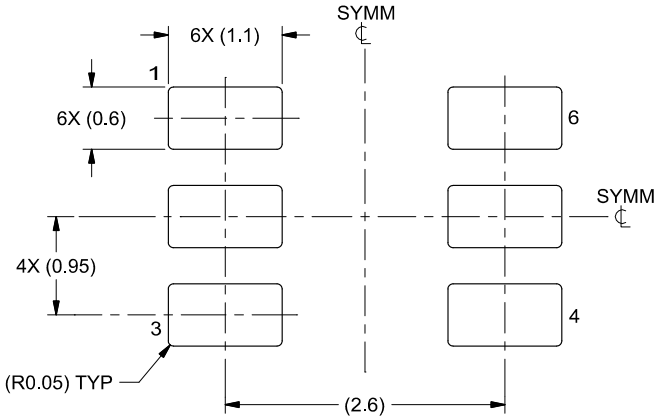


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.280	0.500	0.011	0.020
c	0.100	0.230	0.004	0.009
D	2.820	3.020	0.111	0.119
E	2.600	3.000	0.102	0.118
E1	1.500	1.720	0.059	0.068
e	0.950 BSC		0.037 BSC	
L	0.300	0.600	0.012	0.024
θ	0	8°	0	8°

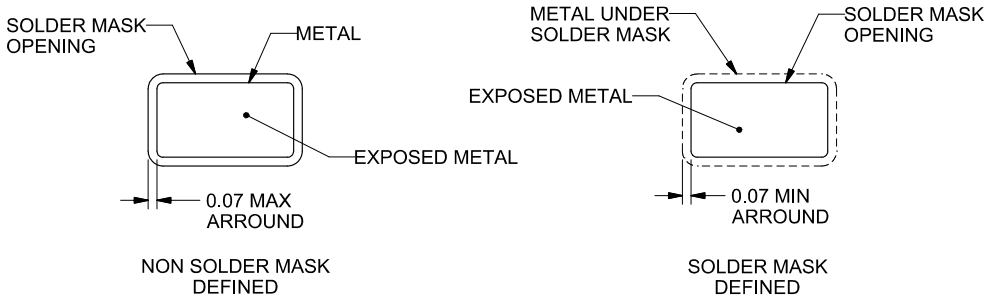
NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Example Board Layout — S6T(SOT23-6-A)



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



SOLDERMASK DETAILS

NOTES

1. Size of metal pad may vary due to creepage requirement.
2. Vias are optional depending on application. It is recommended that vias under paste be filled, plugged or tented.
3. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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