

20-V 200-mA Ultra-Low Noise Ultra-High PSRR Low Dropout Linear Regulator

Features

- Wide Input Voltage Range: 2.5 V to 20 V
- Adjustable Output Voltage Range: 1.2 V to 15 V
- $\pm 2\%$ Accuracy over Line Regulation, Load Regulation, and Operating Temperature Range
- 200-mA Maximum Output Current
- Low Dropout Voltage: 400 mV Max at 200 mA
- Ultra-High PSRR:
 - 110 dB at 1 kHz
 - 80 dB at 1 MHz
- Ultra-Low Output Noise:
 - $1 \mu\text{V}_{\text{RMS}}$ from 10 Hz to 100 kHz
 - $2 \text{ nV}/\sqrt{\text{Hz}}$ at 10 kHz
- Excellent Transient Response
- Precision Enable Threshold
- Adjustable Current Limit with External Resistor
- Open-Drain Power Good Indication
- Adjustable Power-Good Threshold
- Stable with a minimum 4.7- μF Output Capacitor
- Integrated Protection
 - Over-Current Protection
 - Over-Temperature Protection
- Package Options:
 - DFN3X3-10

Applications

- Low-Noise Power Supplies
- Analog Supply: PLL, VCO, Mixer, LNA, ADC
- Low-Noise Instrumentation
- ATE Test Equipment

Description

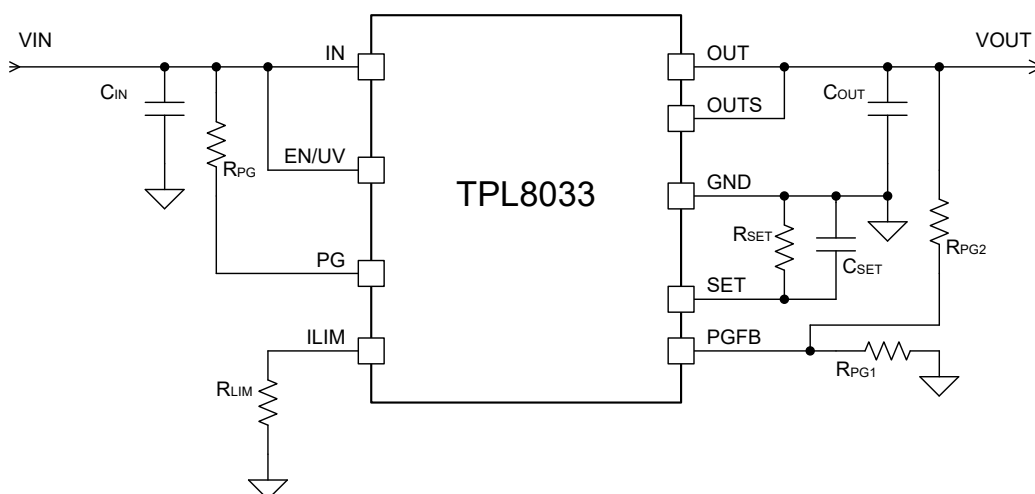
The TPL8033 is a 20-V 200-mA high-performance low-dropout linear regulator with $1\text{-}\mu\text{V}_{\text{RMS}}$ ultra-low noise and 110-dB ultra-high PSRR. The TPL8033 supports adjustable output from 1.2 V to 15 V with a single resistor and is stable with 4.7 μF to 100 μF .

The TPL8033 implements a precision current reference and a high-performance voltage buffer. With an external capacitor connecting to the current reference, the output voltage noise can be further reduced.

The TPL8033 features adjustable output current limit with a single external resistor and adjustable power-good threshold with an external resistors divider. The TPL8033 also integrates over-current protection and over-temperature protection to enhance system reliability.

The TPL8033 provides thermal-enhanced 10-pin DFN3X3 and EMSOP packages with guaranteed operating temperature ranging from -40°C to $+125^{\circ}\text{C}$.

Typical Application Circuit



**20-V 200-mA Ultra-Low Noise Ultra-High PSRR Low Dropout Linear
Regulator****Table of Contents**

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20-V 200-mA Ultra-Low Noise Ultra-High PSRR Low Dropout Linear Regulator**Product Family Table**

Order Number	Output Voltage (V)	Output Current	Package
TPL8033AD-DF8R	Adjustable	200 mA	DFN3X3-10

Revision History

Date	Revision	Notes
2022-09-10	Rev.Pre.0	Preliminary Revision.
2023-02-28	Rev.A.0	Initial Released.

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Pin Configuration and Functions

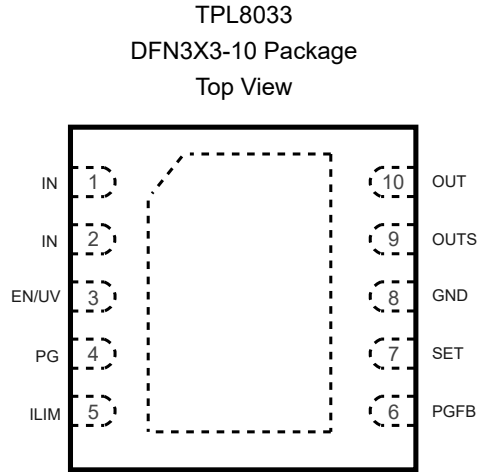


Table 1. Pin Functions: TPL8033

Pin	Name	I/O	Description
DFN3X3			
3	EN/UV	I	Enable/UVLO pin. Drive EN/UV high to turn on the regulator; drive EN/UV low to turn off the regulator. Connecting an external resistor divider from IN, EN/UV to GND to set the UVLO threshold. For automatic startup, connect EN to IN directly.
8	GND	-	Ground reference pin. Connect GND to PCB ground plane directly.
5	ILIM	O	Current limit adjustment pin. Connect a resistor from ILIM to GND to set an accurate output current limit value.
1, 2	IN	I	Input voltage pin. A 10- μ F or larger ceramic capacitor from IN to GND (as close as possible to IN pin) is required to reduce the jitter from the previous-stage power supply.
10	OUT	O	Regulated output voltage pin. A 4.7- μ F or larger ceramic capacitor from OUT to GND (as close as possible to OUT pin) is required to ensure the regulator stability.
9	OUTS	I	Output voltage sense input pin. Kelvin connect OUTS to the output capacitor and the load.
4	PG	O	Open-drain power-good output pin. Leave PG open if not used.
6	PGFB	I	Power-good threshold-setup pin. Connecting an external resistor divider from OUT, PGFB to GND to set the programmable power good threshold. Tie PGFB to IN directly if power good and fast start-up functionalities are not used.
7	SET	O	Output voltage setup pin. Connect a resistor from SET to GND to set the output voltage. A capacitor from SET to GND is recommended to improve output noise, PSRR and transient response performance.

(1) The exposed Pad MUST be connected to a large-area ground plane directly to maximize the thermal performance.

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Specifications**Absolute Maximum Ratings ⁽¹⁾**

Parameter		Min	Max	Unit
IN, EN/UV		-0.3	22	V
OUT, OUTS, SET		-0.3	16	V
PG, PGFB		-0.3	22	V
OUT – OUTS		-1.2	1.2	V
ILIM		-0.3	1	V
T _J	Maximum Junction Temperature	-40	150	°C
T _{STG}	Storage Temperature Range	-65	150	°C
T _L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

(2) All voltage values are with respect to ground.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±3000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±1500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Max	Unit
V _{IN}		2.5	20	V
V _{EN/UV}		0	20	V
V _{OUT} , V _{OUTS}		1.2	15	V
V _{SET}		0	15	V
V _{PG} , V _{PGFB}		0	20	V
V _{ILIM}		0	0.3	V
I _{OUT}		0	200	mA
C _{OUT}		4.7	100	μF
T _J	Junction Temperature Range	-40	125	°C

**20-V 200-mA Ultra-Low Noise Ultra-High PSRR Low Dropout Linear
Regulator****Thermal Information**

Package Type	θ_{JA}	θ_{JB}	$\theta_{JC,BOTTOM}$	Unit
DFN3X3-10	58	15	32	°C/W

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Electrical Characteristics

All test conditions: $V_{IN} = V_{OUT(NOM)} + 1\text{ V}$ or 2.5 V , whichever is greater; OUTS ties directly to OUT, $C_{IN} = C_{OUT} = 4.7\text{ }\mu\text{F}$, $C_{SET} = 4.7\text{ }\mu\text{F}$, $V_{EN/UV} = 5\text{ V}$, $I_{OUT} = 1\text{ mA}$, $-40^{\circ}\text{C} \leq T_J \leq +125^{\circ}\text{C}$, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Unit
Supply Voltage and Current					
$V_{IN}^{(1)}$	Input Supply Voltage	$V_{IN, MIN}$		20	V
$V_{IN, UVLO}$	Input Voltage Under-Voltage Lockout Threshold	V_{IN} rising	1.9	2.4	V
		Hysteresis	100		mV
$I_Q^{(2)}$	Quiescent Current	$I_{OUT} = 10\text{ }\mu\text{A}$, $T_J = 25^{\circ}\text{C}$	2.2		mA
		$I_{OUT} = 1\text{ mA}$	2.8		mA
		$I_{OUT} = 50\text{ mA}$	3.6		mA
		$I_{OUT} = 100\text{ mA}$	5.1		mA
I_{SD}	Shutdown Current	$V_{EN/UV} = 0\text{ V}$	4		μA
Enable and Power Good					
$V_{EN/UV}$	EN/UV Pin Voltage Threshold	$V_{EN/UV}$ rising	1.23		V
		Hysteresis	120		mV
$I_{EN/UV}$	EN/UV Pin Current	$V_{IN} = 20\text{ V}$, $V_{EN/UV} = 0\text{ V}$	-1	1	μA
		$V_{IN} = 20\text{ V}$, $V_{EN/UV} = 1.24\text{ V}$, $T_J = 25^{\circ}\text{C}$	0.15		μA
		$V_{IN} = 0\text{ V}$, $V_{EN/UV} = 20\text{ V}$	0.5		μA
V_{PGFB}	PGFB Pin Voltage Threshold	V_{PGFB} rising	300		mV
		Hysteresis	8		mV
I_{PGFB}	PGFB Pin Current	$V_{IN} = 2\text{ V}$, $V_{PGFB} = 300\text{ mV}$	1.5		nA
$V_{OL(PG)}$	PG Pin Low-Level Output Voltage	$V_{OUT} < V_{PG}$, source 0.1 mA to PG pin	57	100	mV
I_{PG}	PG Pin Leakage Current	$V_{OUT} > V_{PG}$, apply 20 V at PG pin		1	μA
Output Voltage and Current					
I_{SET}	SET Pin Current	$V_{IN} = 2.5\text{ V}$, $V_{OUT} = 1.2\text{ V}$, $I_{OUT} = 1\text{ mA}$, $T_J = 25^{\circ}\text{C}$	100		μA
		$V_{IN} = 2.5\text{ V}$ to 20 V , $V_{OUT} = 1.2\text{ V}$ to 15 V , $I_{OUT} = 1\text{ mA}$ to 200 mA	100		μA
	Fast Startup SET Pin Current	$V_{IN} = 2.8\text{ V}$, $V_{OUT} = 1.3\text{ V}$, $V_{PGFB} = 289\text{ mV}$, $T_J = 25^{\circ}\text{C}$	2		mA
ΔI_{SET}	Change in I_{SET} with V_{SET}	$V_{IN} = 20\text{ V}$, $I_{OUT} = 1\text{ mA}$, $V_{SET} = 1.3\text{ V}$ to 15 V	30		nA
		$V_{IN} = 20\text{ V}$, $I_{OUT} = 1\text{ mA}$, $V_{SET} = 1.2\text{ V}$ to 15 V	30		nA

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Parameter		Conditions	Min	Type	Max	Unit
Output Voltage and Current						
ΔI_{SET}	SET Pin Current Line Regulation	$V_{IN} = 2.5\text{ V to }20\text{ V}$, $V_{OUT} = 1.2\text{ V}$, $I_{OUT} = 1\text{ mA}$		2		nA/V
	SET Pin Current Load Regulation	$V_{IN} = 2.5\text{ V}$, $V_{OUT} = 1.2\text{ V}$, $I_{OUT} = 1\text{ mA to }200\text{ mA}$		3		nA
V_{OS}	Output Voltage Offset, $V_{OUT} - V_{SET}$	$V_{IN} = 2.5\text{ V}$, $V_{OUT} = 1.2\text{ V}$, $I_{OUT} = 1\text{ mA}$, $T_J = 25^\circ\text{C}$		1		mV
		$V_{IN} = 2.5\text{ V to }20\text{ V}$, $V_{OUT} = 1.2\text{ V to }15\text{ V}$, $I_{OUT} = 1\text{ mA to }200\text{ mA}$		2		mV
ΔV_{OS}	Change in V_{OS} with V_{SET}	$V_{IN} = 20\text{ V}$, $I_{OUT} = 1\text{ mA}$, $V_{SET} = 1.2\text{ V to }15\text{ V}$		30		$\mu\text{V/V}$
	V_{OS} Voltage Line Regulation	$V_{IN} = 2.5\text{ V to }20\text{ V}$, $V_{OUT} = 1.2\text{ V}$, $I_{OUT} = 1\text{ mA}$		0.03		mV
	V_{OS} Voltage Load Regulation	$V_{IN} = 2.5\text{ V}$, $V_{OUT} = 1.2\text{ V}$, $I_{OUT} = 1\text{ mA to }200\text{ mA}$		0.3		mV
$V_{DO}^{(3)}$	Dropout Voltage	$I_{OUT} = 1\text{ mA}$, $T_J = 25^\circ\text{C}$		250		mV
		$I_{OUT} = 50\text{ mA}$		250		mV
		$I_{OUT} = 150\text{ mA}$		250		mV
		$I_{OUT} = 200\text{ mA}$		250		mV
I_{CL}	Internal Current Limit	$V_{IN} = 2.5\text{ V}$, $V_{OUT} = 0\text{ V}$		320		mA
		$V_{IN} = 12\text{ V}$, $V_{OUT} = 0\text{ V}$, $T_J = 25^\circ\text{C}$		320		mA
		$V_{IN} = 20\text{ V}$, $V_{OUT} = 0\text{ V}$		320		mA
	Adjustable Current Limit	Current limit ratio		125		mA $\times$ k Ω
		$V_{IN} = 2.5\text{ V}$, $V_{OUT} = 0\text{ V}$, $R_{LIM} = 625\text{ }\Omega$		200		mA
		$V_{IN} = 2.5\text{ V}$, $V_{OUT} = 0\text{ V}$, $R_{LIM} = 2.5\text{ k}\Omega$		50		mA
t_{STR}	Start-Up Time	$V_{IN} = 6\text{ V}$, $V_{OUT} = 5\text{ V}$, $I_{LOAD} = 200\text{ mA}$, $C_{SET} = 0.47\text{ }\mu\text{F}$, $V_{PGFB} = 6\text{ V}$		55		ms
		$V_{IN} = 6\text{ V}$, $V_{OUT} = 5\text{ V}$, $I_{LOAD} = 200\text{ mA}$, $C_{SET} = 4.7\text{ }\mu\text{F}$, $V_{PGFB} = 6\text{ V}$		550		ms
		$V_{IN} = 6\text{ V}$, $V_{OUT} = 5\text{ V}$, $I_{LOAD} = 200\text{ mA}$, $C_{SET} = 4.7\text{ }\mu\text{F}$, $R_{PG1} = 50\text{ k}\Omega$, $R_{PG2} = 700\text{ k}\Omega$ (with Fast Start-Up to 90% of V_{OUT})		10		ms

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Parameter		Conditions	Min	Type	Max	Unit
PRSS and Output Noise						
PSRR	Power Supply Rejection Ratio	$I_{OUT} = 200\text{ mA}$, $V_{Ripple} = 500\text{ mV}_{PP}$, $f = 120\text{ Hz}$, $C_{OUT} = 4.7\text{ }\mu\text{F}$, $C_{SET} = 4.7\text{ }\mu\text{F}$		110		dB
		$I_{OUT} = 200\text{ mA}$, $V_{Ripple} = 150\text{ mV}_{PP}$, $f = 10\text{ kHz}$, $C_{OUT} = 4.7\text{ }\mu\text{F}$, $C_{SET} = 0.47\text{ }\mu\text{F}$		90		dB
		$I_{OUT} = 200\text{ mA}$, $V_{Ripple} = 150\text{ mV}_{PP}$, $f = 100\text{ kHz}$, $C_{OUT} = 4.7\text{ }\mu\text{F}$, $C_{SET} = 0.47\text{ }\mu\text{F}$		80		dB
		$I_{OUT} = 200\text{ mA}$, $V_{Ripple} = 150\text{ mV}_{PP}$, $f = 1\text{ MHz}$, $C_{OUT} = 4.7\text{ }\mu\text{F}$, $C_{SET} = 0.47\text{ }\mu\text{F}$		80		dB
		$I_{OUT} = 200\text{ mA}$, $V_{Ripple} = 80\text{ mV}_{PP}$, $f = 10\text{ MHz}$, $C_{OUT} = 4.7\text{ }\mu\text{F}$, $C_{SET} = 0.47\text{ }\mu\text{F}$		50		dB
V_N	Output Noise Spectral Density	$V_{OUT} = 3.3\text{ V}$, $I_{OUT} = 200\text{ mA}$, $f = 10\text{ Hz}$, $C_{OUT} = 4.7\text{ }\mu\text{F}$, $C_{SET} = 0.47\text{ }\mu\text{F}$		525		nV/ $\sqrt{\text{Hz}}$
		$V_{OUT} = 1.2\text{ V to }15\text{ V}$, $I_{OUT} = 200\text{ mA}$, $f = 10\text{ Hz}$, $C_{OUT} = 4.7\text{ }\mu\text{F}$, $C_{SET} = 4.7\text{ }\mu\text{F}$		68		nV/ $\sqrt{\text{Hz}}$
		$V_{OUT} = 1.2\text{ V to }15\text{ V}$, $I_{OUT} = 200\text{ mA}$, $f = 10\text{ kHz}$, $C_{OUT} = 4.7\text{ }\mu\text{F}$, $C_{SET} = 4.7\text{ }\mu\text{F}$		2.3		nV/ $\sqrt{\text{Hz}}$
		$V_{OUT} = 3.3\text{ V}$, $I_{OUT} = 200\text{ mA}$, $f = 10\text{ Hz to }100\text{ kHz}$, $C_{OUT} = 4.7\text{ }\mu\text{F}$, $C_{SET} = 0.47\text{ }\mu\text{F}$		2.5		μV_{RMS}
		$V_{OUT} = 1.2\text{ V to }15\text{ V}$, $I_{OUT} = 200\text{ mA}$, $f = 10\text{ Hz to }100\text{ kHz}$, $C_{OUT} = 4.7\text{ }\mu\text{F}$, $C_{SET} = 4.7\text{ }\mu\text{F}$		1		μV_{RMS}
	I_{SET} Current RMS Output Noise	$BW = 10\text{ Hz to }100\text{ kHz}$		6		nA _{RMS}
Temperature Range						
T_{SD}	Thermal Shutdown Threshold			170		°C
		Hysteresis		20		°C

(1) $V_{IN,MIN} = V_{OUT(NOM)} + 1\text{ V}$ or 2.5 V , whichever is greater.

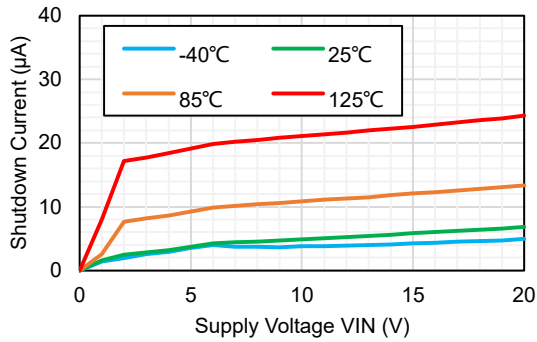
(2) I_{SET} and I_{LIM} are not included.

(3) Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. Dropout voltage is measured for output $\geq 2\text{ V}$. In dropout, the output voltage is equal to: $V_{IN} - V_{DROPOUT}$.

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Typical Performance Characteristics

All test conditions: $V_{IN} = V_{OUT(NOM)} + 1\text{ V}$ or 2.5 V , whichever is greater; $OUTS$ ties directly to OUT , $C_{IN} = C_{OUT} = 4.7\text{ }\mu\text{F}$, $C_{SET} = 4.7\text{ }\mu\text{F}$, $V_{EN/UV} = 5\text{ V}$, $I_{OUT} = 1\text{ mA}$, $-40^{\circ}\text{C} \leq T_J \leq +125^{\circ}\text{C}$, unless otherwise noted.



$V_{EN/UV} = 0\text{ V}$

Figure 1. Shutdown Current

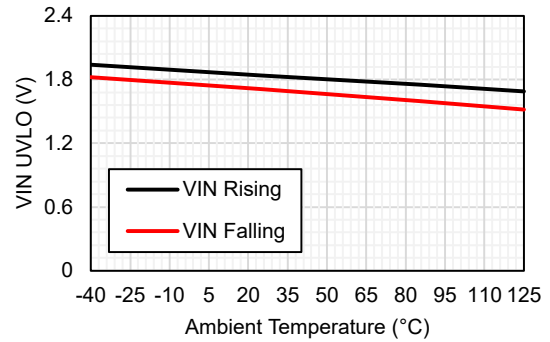


Figure 2. Supply Voltage UVLO

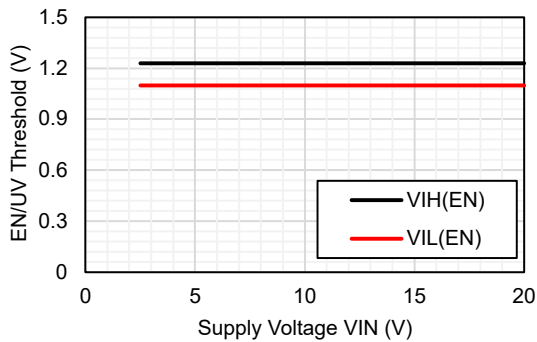
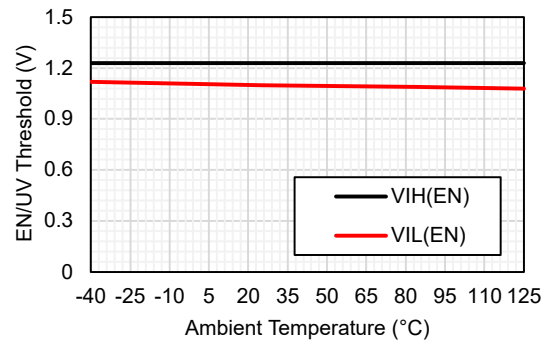
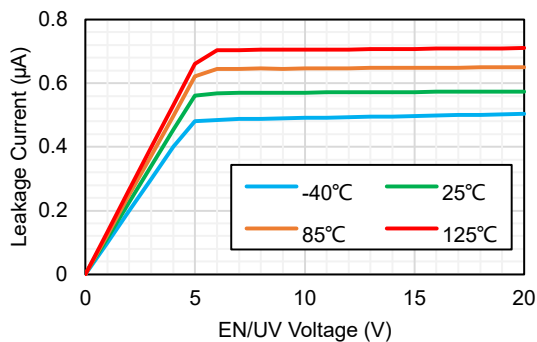


Figure 3. EN/UV Threshold



$V_{IN} = 2.5\text{ V}$

Figure 4. EN/UV Threshold vs Temperature



$V_{EN/UV} = V_{IN}$

Figure 5. EN/UV Leakage Current

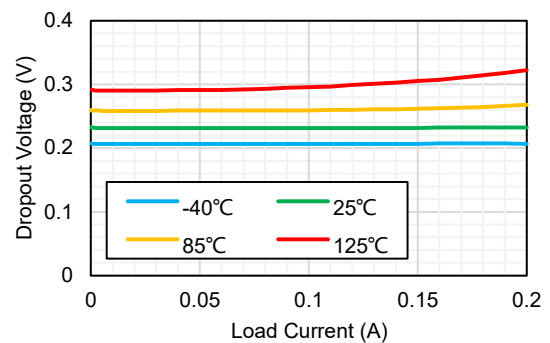
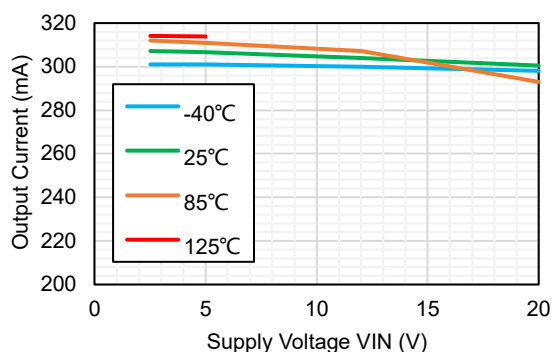
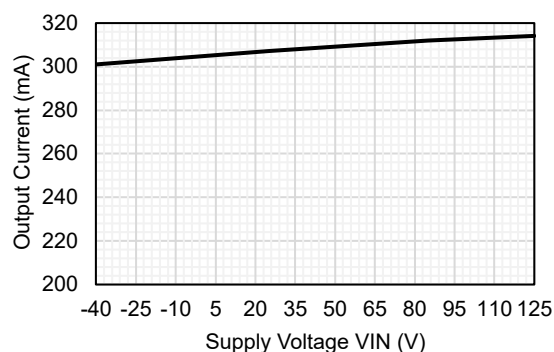
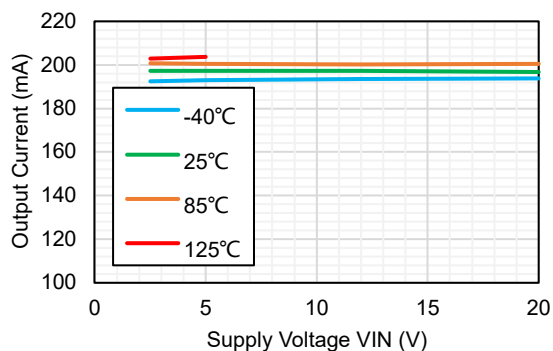
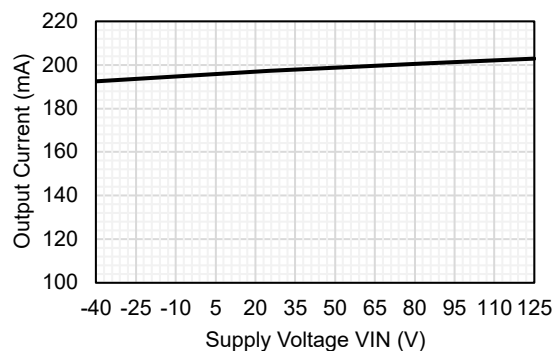
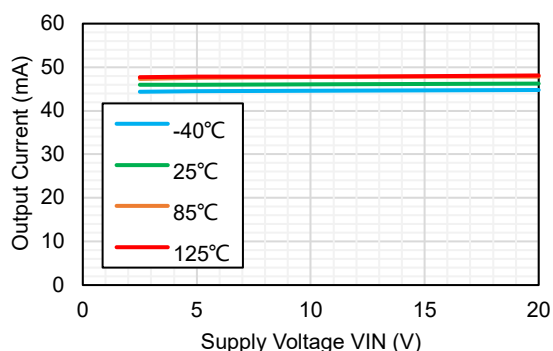
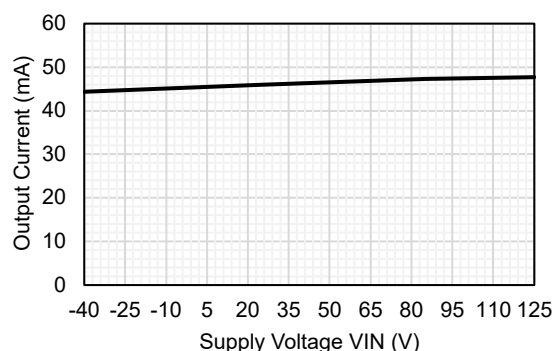
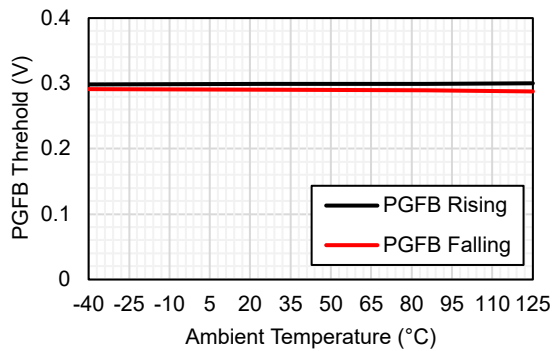
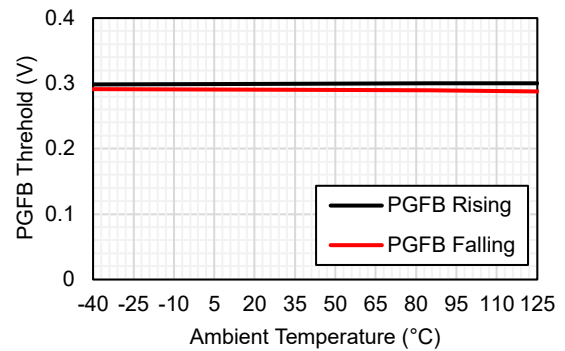
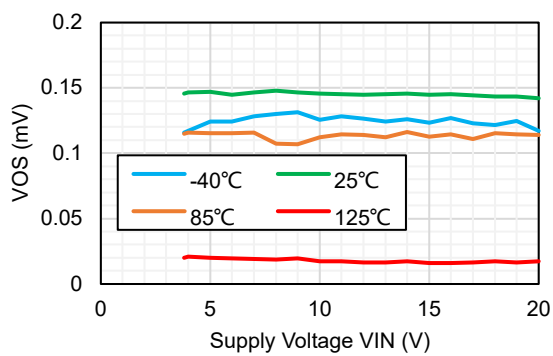
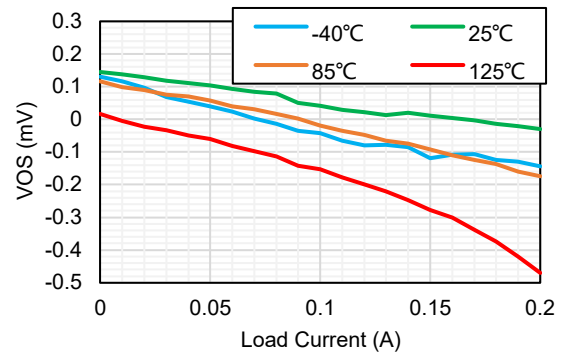
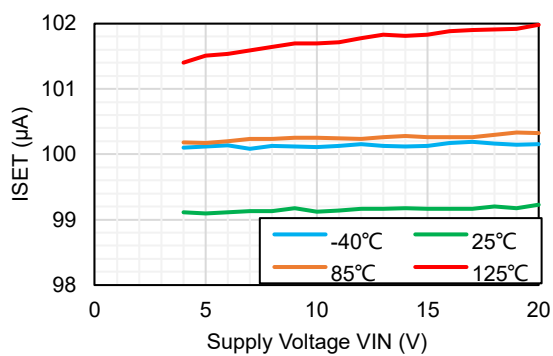
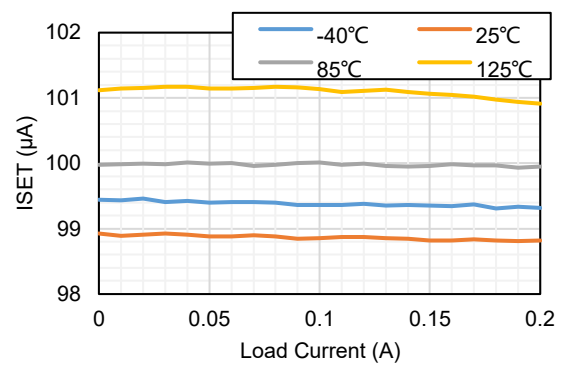


Figure 6. Dropout Voltage

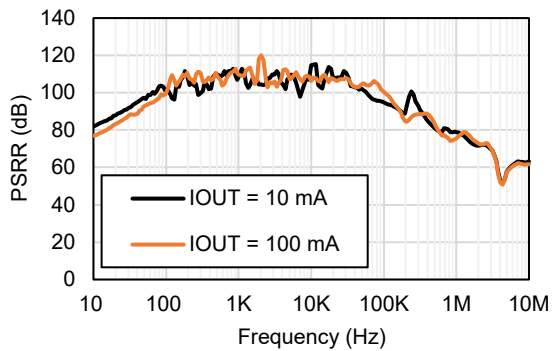
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 $R_{ILIM} = 0$
Figure 7. Current Limit

 $R_{ILIM} = 0$
Figure 8. Current Limit vs Temperature

 $R_{ILIM} = 620 \Omega$
Figure 9. Current Limit

 $R_{ILIM} = 620 \Omega$
Figure 10. Current Limit vs Temperature

 $R_{ILIM} = 2.5 k\Omega$
Figure 11. Current Limit

 $R_{ILIM} = 2.5 k\Omega$
Figure 12. Current Limit vs Temperature

20-V 200-mA Ultra-Low Noise Ultra-High PSRR Low Dropout Linear Regulator

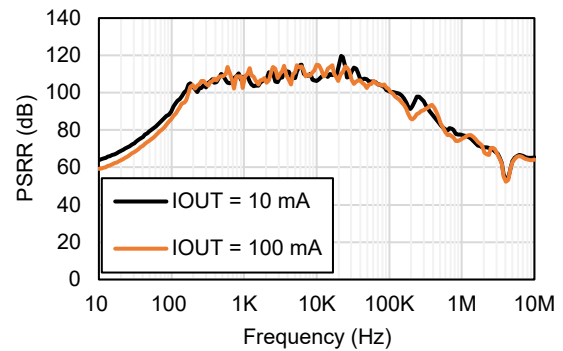

 $V_{IN} = 2.5\text{ V}$
Figure 13. PGFB Threshold

 $V_{IN} = 20\text{ V}$
Figure 14. PGFB Threshold

Figure 15. VOS Line Regulation

 $V_{IN} = 4.3\text{ V}$
Figure 16. VOS Load Regulation

Figure 17. ISET Line Regulation

Figure 18. ISET Load Regulation

20-V 200-mA Ultra-Low Noise Ultra-High PSRR Low Dropout Linear Regulator



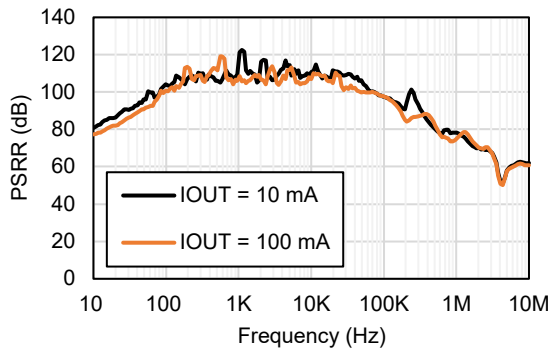
$V_{IN} = 5.3 \text{ V}$, $V_{OUT} = 3.3 \text{ V}$, $C_{SET} = 4.7 \mu\text{F}$

Figure 19. PSRR



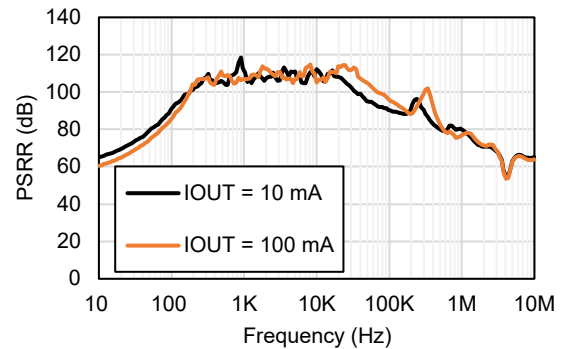
$V_{IN} = 5.3 \text{ V}$, $V_{OUT} = 3.3 \text{ V}$, $C_{SET} = 0.47 \mu\text{F}$

Figure 20. PSRR



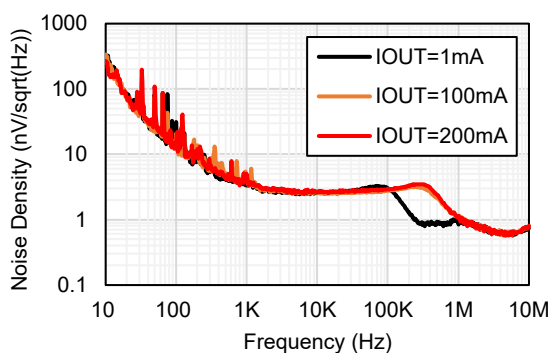
$V_{IN} = 5 \text{ V}$, $V_{OUT} = 3.3 \text{ V}$, $C_{SET} = 4.7 \mu\text{F}$

Figure 21. PSRR



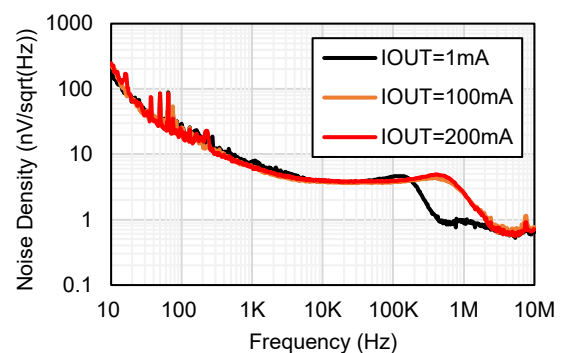
$V_{IN} = 5 \text{ V}$, $V_{OUT} = 3.3 \text{ V}$, $C_{SET} = 0.47 \mu\text{F}$

Figure 22. PSRR



$V_{IN} = 5 \text{ V}$, $V_{OUT} = 3.3 \text{ V}$, $C_{SET} = 4.7 \mu\text{F}$

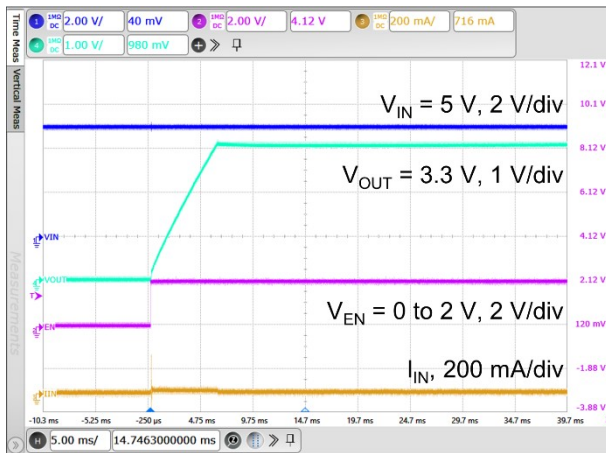
Figure 23. Noise



$V_{IN} = 2.5 \text{ V}$, $V_{OUT} = 1.2 \text{ V}$, $C_{SET} = 4.7 \mu\text{F}$

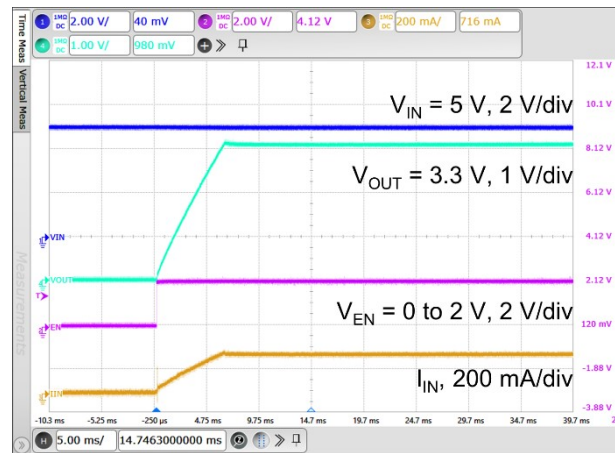
Figure 24. Noise

20-V 200-mA Ultra-Low Noise Ultra-High PSRR Low Dropout Linear Regulator



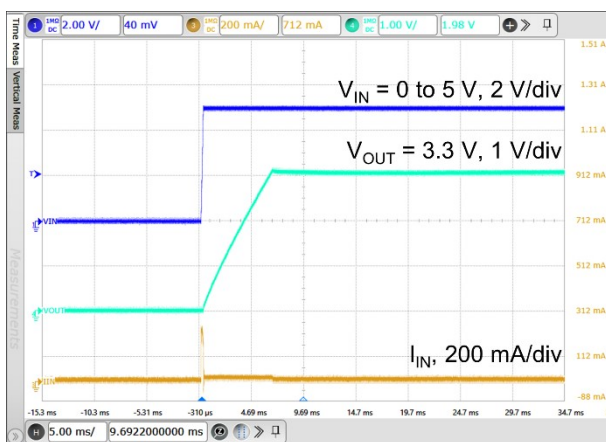
$I_{OUT} = 0$

Figure 25. EN/UV Startup



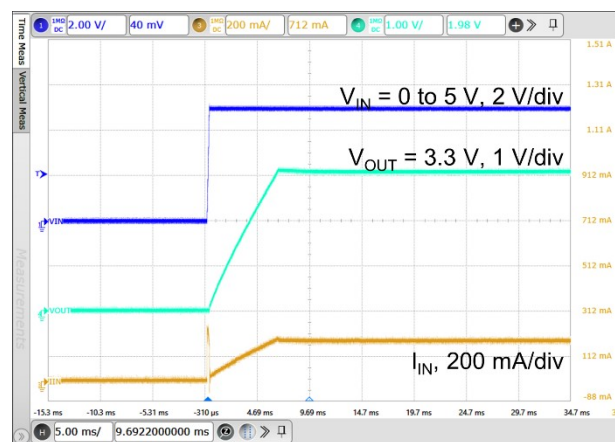
$I_{OUT} = 200$ mA

Figure 26. EN/UV Startup



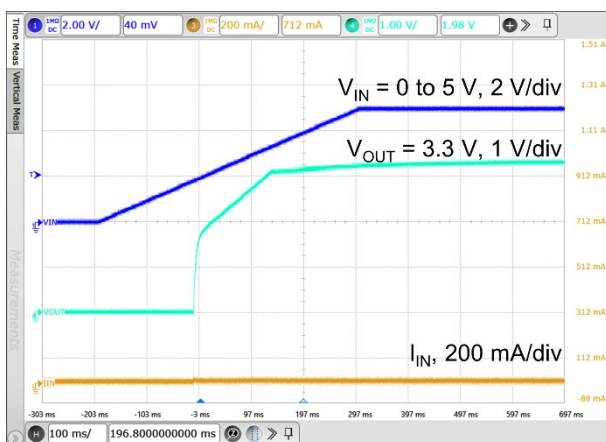
V_{IN} starts in 100 μ s, $I_{OUT} = 0$

Figure 27. V_{IN} Startup



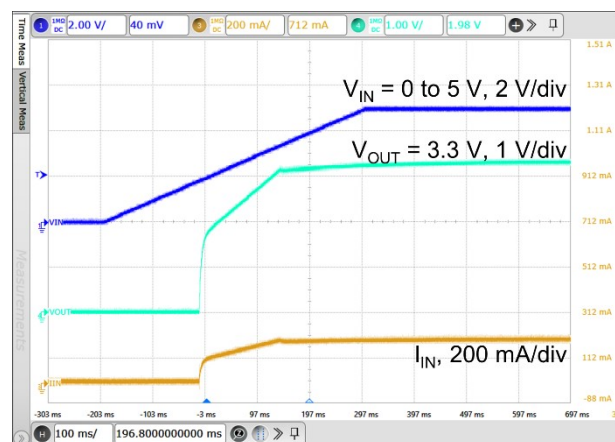
V_{IN} starts in 100 μ s, $I_{OUT} = 200$ mA

Figure 28. V_{IN} Startup



V_{IN} starts in 500 ms, $I_{OUT} = 0$

Figure 29. V_{IN} Startup



V_{IN} starts in 500 ms, $I_{OUT} = 200$ mA

Figure 30. V_{IN} Startup

20-V 200-mA Ultra-Low Noise Ultra-High PSRR Low Dropout Linear Regulator

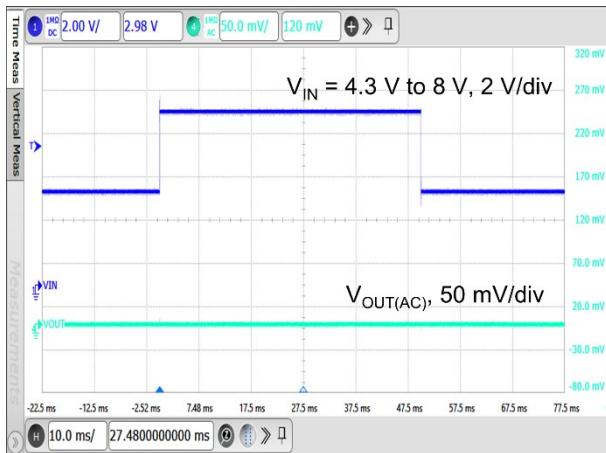


Figure 31. Line Transient

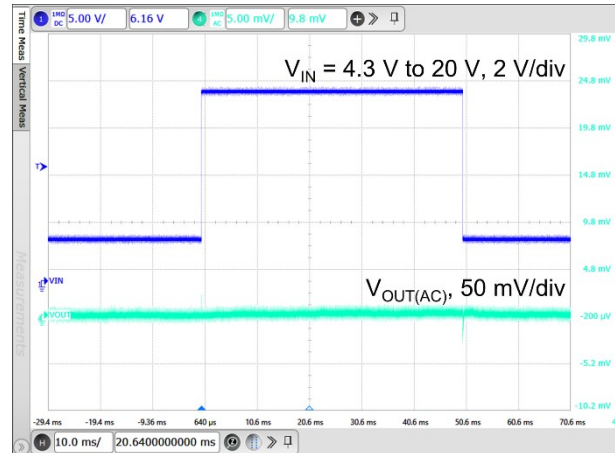


Figure 32. Line Transient

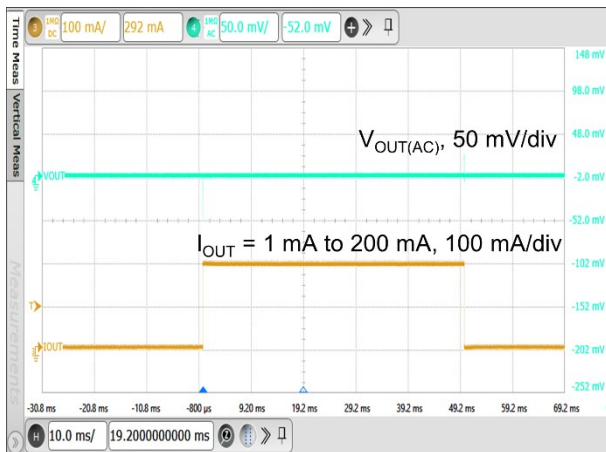


Figure 33. Load Transient

20-V 200-mA Ultra-Low Noise Ultra-High PSRR Low Dropout Linear Regulator

Detailed Description

Overview

The TPL8033 is a 20-V 200-mA high-performance low-dropout linear regulator with 1- μV_{RMS} ultra-low noise and 110-dB ultra-high PSRR. The TPL8033 support adjustable output from 1.2 V to 15 V with a single resistor and is stable with 4.7 μF to 100 μF .

The TPL8033 implements a precision current reference and a high-performance voltage buffer. With an external capacitor connecting to the current reference, the output voltage noise can be further reduced.

The TPL8033 features adjustable output current limit with a single external resistor and adjustable power-good threshold with an external resistors divider. The TPL8033 also integrates over-current protection and over-temperature protection to enhance system reliability.

Functional Block Diagram

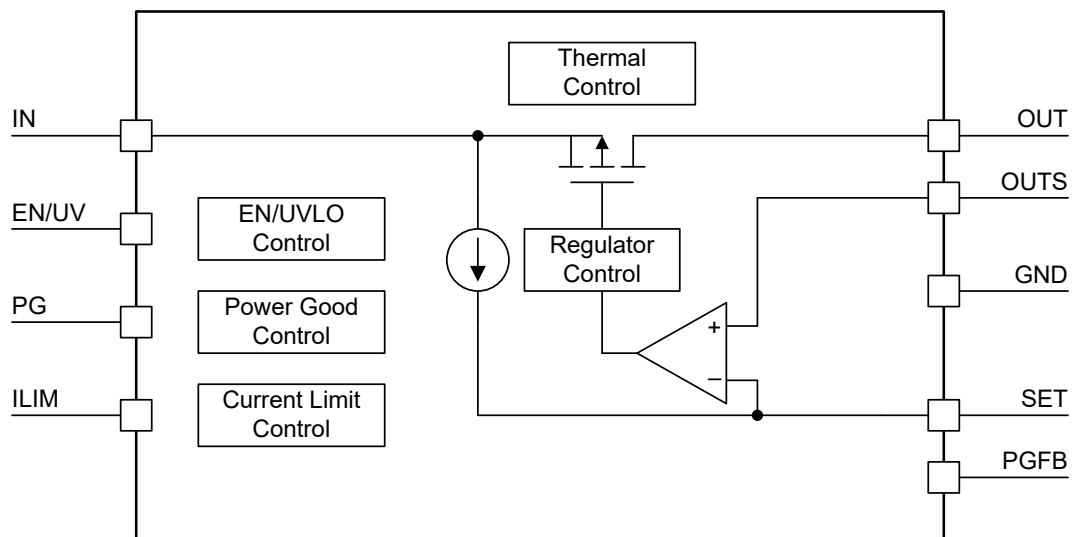


Figure 34. Functional Block Diagram

Feature Description

Enable/UVLO (EN/UV)

The TPL8033 integrates an EN/UV pin to turn on or turn off the device. This pin has an accurate 1.23-V turn-on threshold with 120-mV hysteresis. This EN/UV threshold can be used to set an accurate under-voltage lockout (UVLO) threshold of the input voltage with a resistor divider connected from V_{IN} to GND. The UVLO threshold can be calculated according to [Equation 1](#).

$$V_{\text{IN, UVLO}} = 1.23\text{V} \times \left(1 + \frac{R_{\text{EN2}}}{R_{\text{EN1}}}\right) + I_{\text{EN}} \times R_{\text{EN2}} \quad (1)$$

where,

- R_{EN1} is the low-side resistor connected from the EN/UV pin to the GND pin.
- R_{EN2} is the high-side resistor connected from the IN pin to the EN/UV pin.
- I_{EN} is the EN/UV pin current. This current can be neglected if the R_{EN1} is less than 100 k Ω .

20-V 200-mA Ultra-Low Noise Ultra-High PSRR Low Dropout Linear Regulator

If accurate UVLO is not used, connect EN/UV pin to VIN directly or a digital logic control circuit.

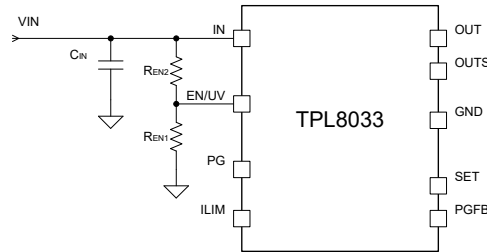


Figure 35. UVLO Threshold

Adjustable Output Voltage (SET, OUT, OUTS)

The TPL8033 integrates a precision 100- μ A current source flowing out of the SET pin. The output voltage can be set by connecting an external resistor (R_{SET}) and capacitor (C_{SET}) at this SET pin. Below table provides different output voltage options with corresponding external resistors.

The OUTS pin of the TPL8033 provides a Kelvin sense connection to the output. The ground side of the resistor at the SET pin provides a Kelvin sense connection to the ground side of the load.

Table 2. Output Voltage and R_{SET} Resistors

V_{OUT} (V)	R_{SET} (k Ω)
2.5	24.9
3.3	33.2
5	49.9
12	121
15	150

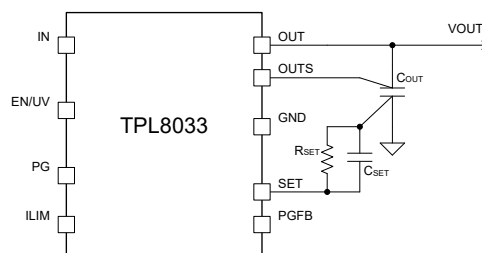


Figure 36. OUTS Pin Kelvin Sense Connction

Power Good (PG)

The TPL8033 integrates an open-drain output power good indicator. Connect the PG pin to a pull-up voltage through a resistor from 10 k Ω to 100 k Ω if the power good function is used. Left the PG pin open if it is not used.

After regulator startup, the PG pin keeps low impedance until the output voltage reaches the power good threshold, $V_{PG,TH}$. When the output voltage is higher than $V_{PG,TH}$, the PG pin turns to high output impedance, and PG is pulled up to a high voltage level to indicate the output voltage is ready.

Please note, the power good function is disabled in shutdown mode.

20-V 200-mA Ultra-Low Noise Ultra-High PSRR Low Dropout Linear Regulator

Adjustable Power Good Threshold (PGFB)

The TPL8033 integrates an adjustable power-good threshold, of which the value can be set by an external resistor divider. Use [Equation 2](#) to calculate the power good threshold.

$$V_{PG, TH} = 0.3V \times \left(1 + \frac{R_{PG2}}{R_{PG1}}\right) + I_{PGFB} \times R_{PG2} \quad (2)$$

where,

- R_{PG1} is the low-side resistor connected from the PGFB pin to the GND pin.
- R_{PG2} is the high-side resistor connected from the OUT pin to the PGFB pin.
- I_{PGFB} is the PGFB pin current. This current can be neglected if the R_{PG1} is less than 30 k Ω .

Please note, the adjustable power good function is disabled in shutdown mode.

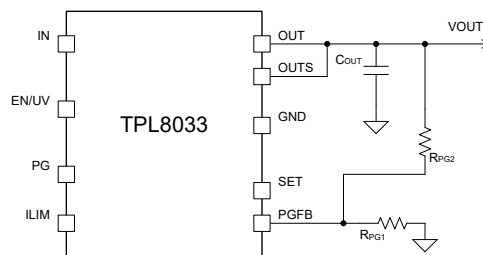


Figure 37. Power Good Threshold

Over-Current Protection(ILIM)

The TPL8033 integrates a current limit circuit that helps to protect the device during fault conditions. The default current limit value is typically 320 mA, and the TPL8033 also provides an adjustable option set by an external resistor R_{LIM} . Use [Equation 3](#) to calculate the adjustable current limit value.

$$\text{Current} \quad (3)$$

For example:

- when $R_{LIM} = 2.5 \text{ k}\Omega$, the output current limit is set to 50 mA.
- when $R_{LIM} = 625 \Omega$, the output current limit is set to 200 mA.

Over-Temperature Protection

The over-temperature protection starts to work when the junction temperature exceeds the thermal shutdown threshold, which turns off the regulator immediately. Until when the device cools down and the junction temperature falls below a value which equals to the thermal shutdown threshold minus thermal shutdown hysteresis, the regulator turns on again.

The junction temperature range should be limited according to the [Recommended Operating Conditions](#) table, continuously operating above the junction temperature range reduces the device lifetime.

20-V 200-mA Ultra-Low Noise Ultra-High PSRR Low Dropout Linear Regulator

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPL8033 is a 20-V 200-mA high-performance low-dropout linear regulator with 1- μV_{RMS} ultra-low noise and 110-dB ultra-high PSRR.

Typical Application

The [Figure 38](#) shows the typical application schematic.

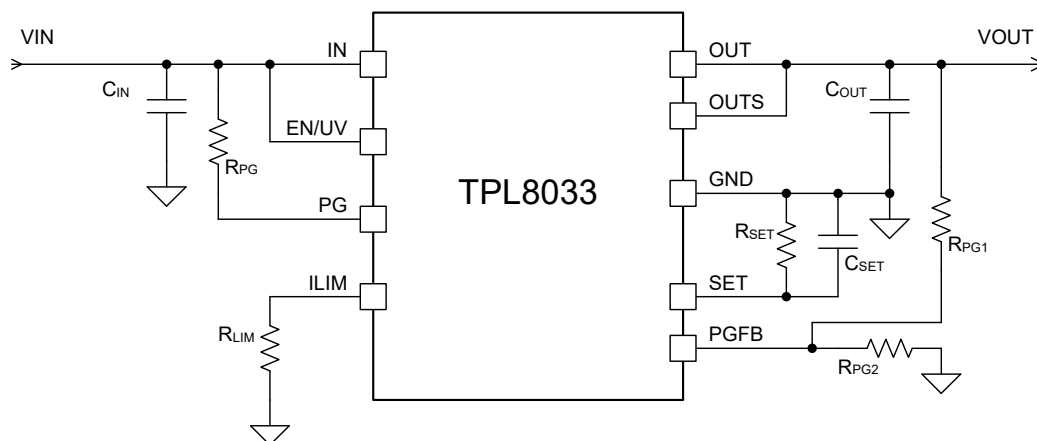


Figure 38. Typical Application Circuit

Input Capacitor and Output Capacitor

3PEAK recommends adding a 10- μF or greater capacitor at the IN pin to keep the input voltage stable. The voltage rating of the capacitors must be higher than the maximum input voltage.

To ensure the loop stability, the TPL8033 requires a ceramic capacitor from 4.7 μF to 100 μF at the regulator output. 3PEAK recommends selecting a 10- μF or greater X7R ceramic capacitor with low ESR range at the OUT pin.

Both input capacitors and output capacitors must be placed as close to the device pins as possible.

Power Dissipation and Thermal Consideration

During the normal operation, the LDO junction temperature should meet the requirement in the [Recommended Operating Conditions](#) table. Use the equations below to calculate the power dissipation and estimate the junction temperature.

The power dissipation can be calculated using below equation.

$$P_D = (V_{IN} - V_{BAT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad (4)$$

The junction temperature can be estimated using below equation. θ_{JA} is the junction-to-ambient thermal resistance.

$$T_J = T_A + P_D \times \theta_{JA} \quad (5)$$

20-V 200-mA Ultra-Low Noise Ultra-High PSRR Low Dropout Linear Regulator

Layout

Layout Guideline

- Both input capacitors and output capacitors must be placed as close to the device pins as possible.
- It is recommended to bypass the IN pin to ground with a 10- μ F capacitor in parallel with a 0.1- μ F small ceramic capacitor. The loop area formed by the bypass capacitor connection, the IN pin, and the GND pin of the system must be as small as possible.
- It is required to place a decoupling 4.7- μ F or greater capacitor at the output. A small 0.1- μ F ceramic capacitor in parallel is recommended to filter the noise and improve the output transient performance.
- It is recommended to use wide and thick trace to minimize $I \times R$ drop and heat dissipation.

Layout Example

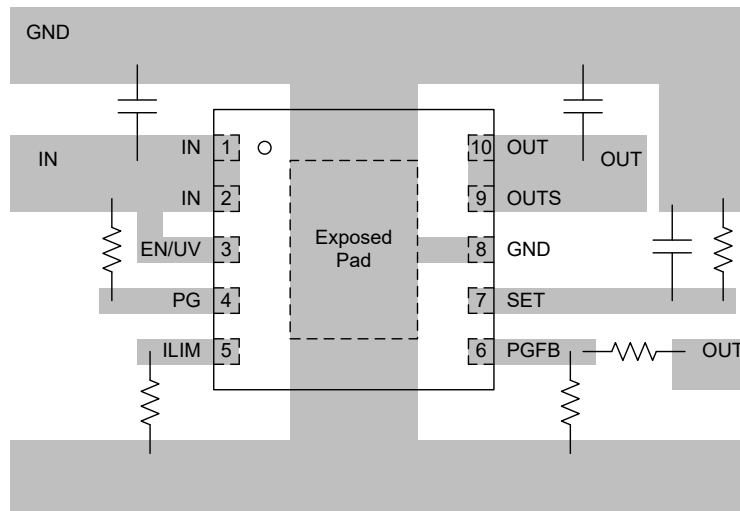
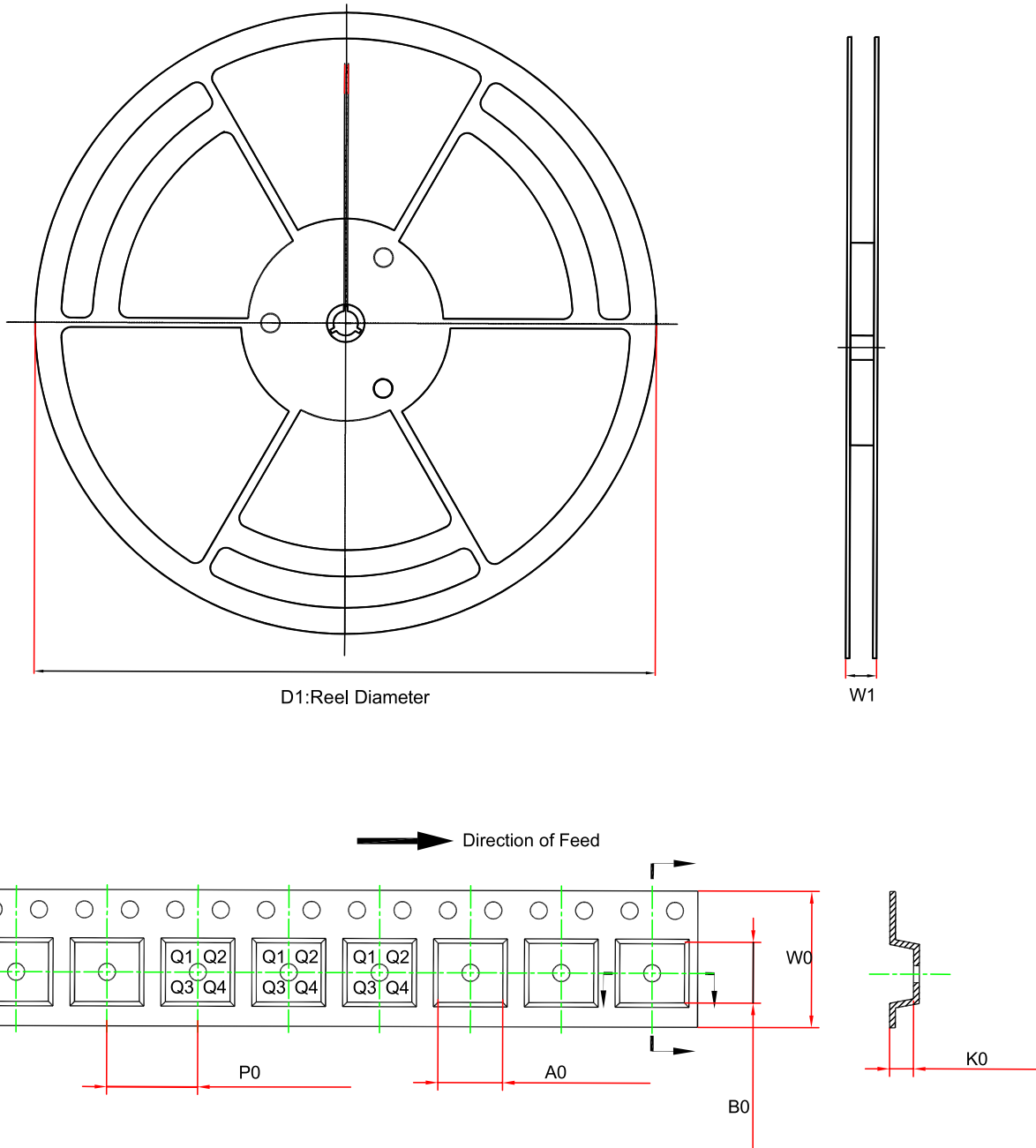


Figure 39. Layout Example

20-V 200-mA Ultra-Low Noise Ultra-High PSRR Low Dropout Linear Regulator

Tape and Reel Information

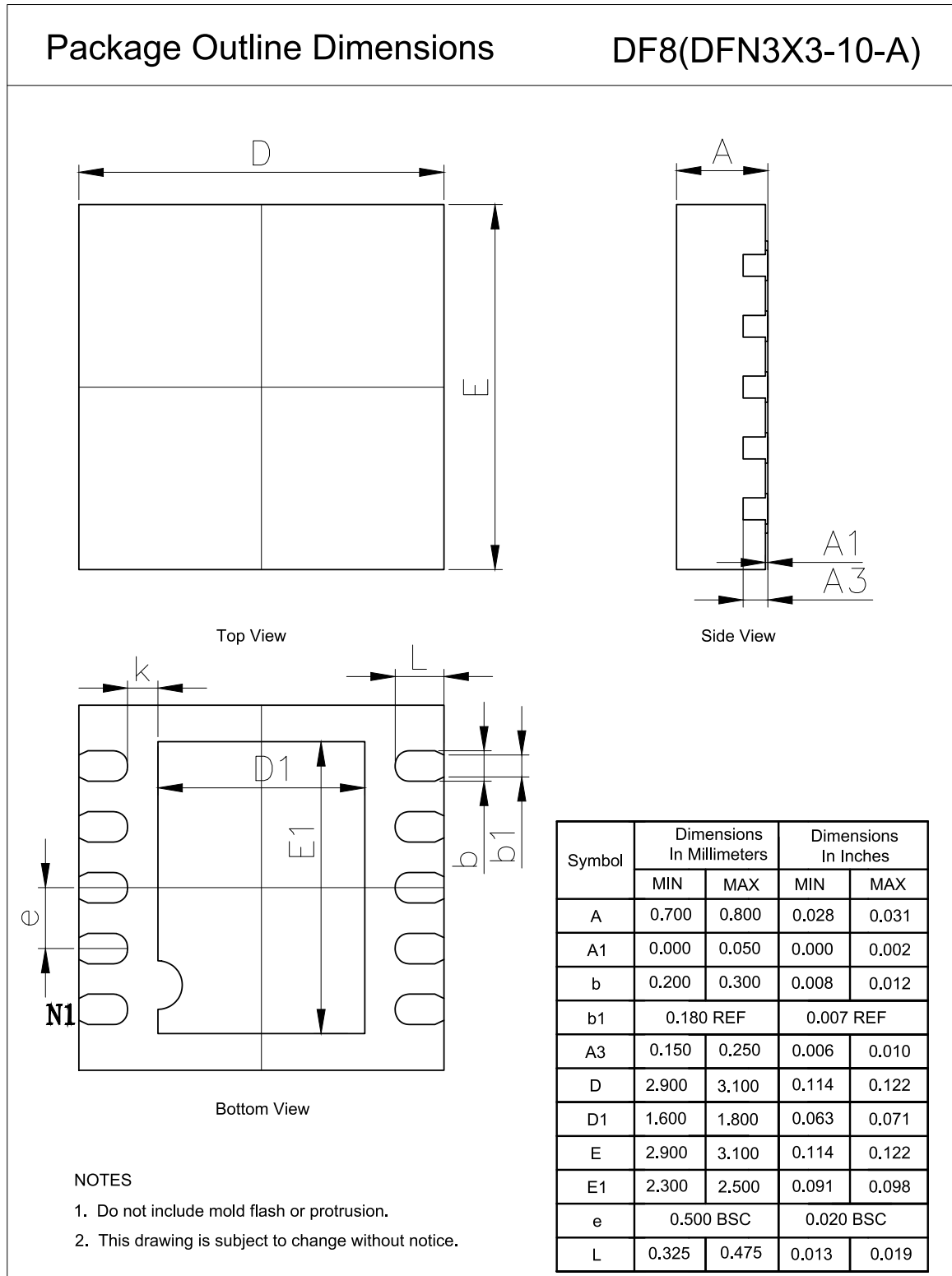


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPL8033AD-DF8R	DFN3X3-10	330	17.6	3.3	3.3	1.1	8	12	Q1

20-V 200-mA Ultra-Low Noise Ultra-High PSRR Low Dropout Linear Regulator

Package Outline Dimensions

DFN3X3-10



20-V 200-mA Ultra-Low Noise Ultra-High PSRR Low Dropout Linear Regulator**Order Information**

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPL8033AD-DF8R	-40°C to +125°C	DFN3X3-10	L83A	MSL3	4,000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

**20-V 200-mA Ultra-Low Noise Ultra-High PSRR Low Dropout Linear
Regulator****IMPORTANT NOTICE AND DISCLAIMER**

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