1-A Output, High-PSRR, Low-Noise, Low-Dropout Linear Regulator

Features

- Qualified for Automotive Applications
  - AEC-Q100 Grade 1, T_A: –40°C to +125°C
  - Junction Temperature, T_J: –40°C to +150°C
- Input Voltage Range: 2.2 V to 5.5 V
- Output Voltage Option:
  - Adjustable Output Voltage: 0.8 V to 5 V
- ±2% Accuracy over Line Regulation, Load Regulation, and Operating Temperature Range
- 1-A Maximum Output Current
- Low Dropout Voltage: 500 mV Maximum at 1 A
- High PSRR:
  - 78 dB at 1 kHz
  - 51 dB at 100 kHz
- 4.9-μV_{RMS} Output Voltage Noise
- Excellent Transient Response
- Stable with a 4.7-µF or Greater Ceramic Output Capacitor
- Protection:
  - Over-Current Protection
  - Over-Temperature Protection
- Package Options:
  - DFN3X3-8

Applications

- Automotive RF Power Supply
- Automotive Telematics Power Supply
- Automotive ECU Power Supply

Description

The TPL910Q series is a 1-A high-current, 4.9-μV_{RMS} low-noise, 78-dB high-PSRR linear regulator with 500-mV maximum ultra-low dropout voltage at 1-A load current. The TPL910Q supports adjustable output voltage ranging from 0.8 V to 5 V with an external resistor divider.

Ultra-low noise, high PSRR, and high output current capabilities make the TPL910Q the ideal power supply for noise-sensitive applications, such as high-speed communication facilities, and high-definition imaging equipment. With accurate output voltage tolerance, excellent transient response, and adjustable soft-start control, the TPL910Q is an optimal power supply for the large-scale processors or digital loads, such as automotive ECUs.

The TPL910Q provides a DFN3X3-8 package with guaranteed operating ambient temperature ranging from –40°C to +125°C.

Typical Application Circuit

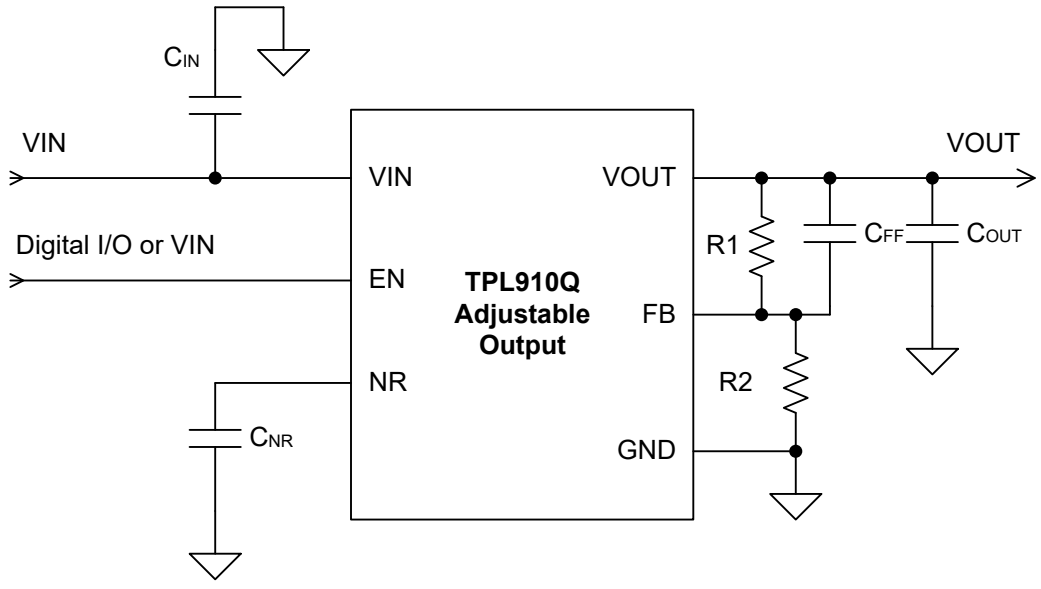


Table of Contents

Product Family Table

Order Number	Output Voltage (V)	Package
TPL910ADJQ-DF6R-S	Adjustable (0.8 V to 5 V)	DFN3X3-8

Revision History

Date	Revision	Notes
2020-12-31	Rev.Pre.0	Preliminary version
2021-12-15	Rev.Pre.1	Updated Electrical Characteristics Table
2022-05-21	Rev.A.0	Initial released
2022-08-31	Rev.A.1	Updated Thermal Information Table
2023-06-15	Rev.A.2	1. Updated Output Accuracy 2. Added Typical Value of Dropout Voltage

Pin Configuration and Functions

TPL910Q-S
DFN3X3-8 Package
Top View

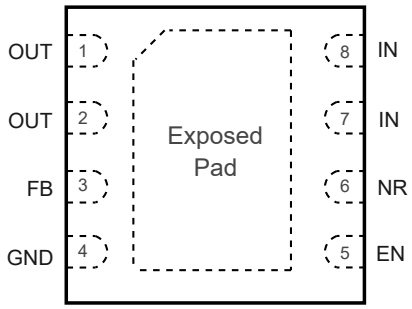


Table 1. Pin Functions: TPL910Q-S

Pin Number	Pin Name	I/O	Description
5	EN	I	Regulator enable pin. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to IN directly. The EN pin must not be left floating.
3	FB	I	Output voltage feedback pin. Connect to an external resistor divider to adjust the output voltage. A 10-nF feed-forward capacitor from FB to OUT (as close as possible to FB pin) is recommended to maximize regulator ac performance.
4	GND	–	Ground reference pin. Connect GND pin to PCB ground plane directly.
7, 8	IN	I	Input voltage pin. Suggest connecting a 10-μF or larger ceramic capacitor from IN to the ground (as close as possible to IN pin) to reduce the jitter from the previous-stage power supply.
6	NR/SS	I	Noise-reduction and soft-start pin. A 10-nF or larger capacitor from NR/SS to GND (as close as possible to NR/SS pin) is recommended to maximize ac performance.
1, 2	OUT	O	Regulated output voltage pin. A 4.7-μF or larger ceramic capacitor from OUT to ground (as close as possible to OUT pin) is required to ensure regulator stability.
–	Exposed Pad	–	Exposed PAD must be connected to a large-area ground plane to maximize the thermal performance.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
IN, EN		−0.3	6	V
OUT		−0.3	V_{IN} + 0.3	V
FB, NR		−0.3	3.6	V
T_J	Maximum Junction Temperature	−40	150	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) All voltage values are with respect to GND.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Max	Unit
IN	Input Voltage	2.2	5.5	V
EN	Enable Voltage	0	5.5	V
OUT	Output Voltage	0.8	5	V
OUT	Output Current	0	1	A
C_{OUT}	Output Capacitor	4.7		μF
T_A	Ambient Temperature Range	−40	125	°C
T_J	Junction Temperature Range	−40	150	°C

Thermal Information

Package Type	θ_{JA}	$\theta_{JC,top}$	θ_{JB}	$\theta_{JC,bottom}$	Unit
DFN3X3-8	60	36.4	28.8	9.3	°C/W

Electrical Characteristics

All test conditions: V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2.2 V, whichever is greater; C_{IN} = C_{OUT} = 4.7 µF, C_{NR} = 10 nF, C_{FF} = open, −40°C ≤ T_A ≤ +125°C, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Supply Input Voltage and Current						
V_{IN}	Input Supply Voltage Range (1)		2.2		5.5	V
UVLO	Input Supply UVLO	V_{IN} rising, R_L = 1 kΩ			2.1	V
	Hysteresis			70		mV
I_{GND}	GND Pin Current	V_{IN} = 5.5 V, I_{OUT} = 1 mA		130	190	µA
		V_{IN} = 5.5 V, I_{OUT} = 1 A		5.4	8	mA
I_{SD}	Shutdown Current	V_{IN} = 5.5 V, V_{EN} = Low		3	10	µA
Device Enable						
$V_{IH(EN)}$	EN Pin High-Level Input Voltage	Device enabled	1.2		5.5	V
$V_{IL(EN)}$	EN Pin Low-Level Input Voltage	Device disabled	0		0.4	V
I_{EN}	EN Pin Current	V_{IN} = 5.5 V, V_{EN} = 0 V to 5.5 V		0.1	1	µA
Regulated Output Voltage and Current						
V_{FB}	Feedback Voltage (2)		0.8 × 98%	0.8	0.8 × 102%	V
I_{FB}	FB Pin Leakage Current (2)	V_{IN} = 5.5 V, stress V_{FB} = 0.8 V		0.1	1	µA
$V_{NR/SS}$	NR/SS Pin Voltage			0.8		V
$I_{NR/SS}$	NR/SS Pin Charging Current	V_{IN} = 5.5 V, V_{NR} = GND		6	9	µA
V_{OUT}	Output Accuracy (3)	V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2.2 V to 5.5 V, V_{OUT} = 0.8 V to 5 V, I_{OUT} = 100 mA to 1 A	−2%		2%	
ΔV_{OUT}	Line Regulation	V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2.2 V to 5.5 V, I_{OUT} = 100 mA		0.03		mV/V
	Load Regulation	I_{OUT} = 100 mA to 1 A		0.07		mV/A
V_{DO}	Dropout Voltage (4)	V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2.2 V to 5.5 V, I_{OUT} = 100 mA, V_{FB} = GND		15	100	mV
		V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2.2 V to 5.5 V, I_{OUT} = 500 mA, V_{FB} = GND		75	250	mV
		V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2.2 V to 5.5 V, I_{OUT} = 1 A, V_{FB} = GND		150	500	mV
Regulated Output Voltage and Current						
I_{LIM}	Output Current Limit	V_{OUT} is forced at 0.9 × $V_{OUT(NOM)}$, V_{IN} ≥ 3.3 V	1.1	1.6		A
I_{SC}	Short-to-Ground Current Limit	V_{OUT} is forced to GND, T_A = 25°C		600		mA

Parameter		Conditions		Min	Typ	Max	Unit
t_{STR}	Start-up Time	$V_{OUT(NOM)}$ = 3.3 V, V_{OUT} = 0% to 90% $V_{OUT(NOM)}$, R_L = 3.3 kΩ, C_{OUT} = 10 µF, C_{NR} = 470 nF			80		ms
PSRR and Noise							
PSRR	Power Supply Ripple Rejection	V_{IN} = 4.3 V, V_{OUT} = 3.3 V, I_{OUT} = 1 A, C_{NR} = 470 nF, C_{FF} = 470 nF,	f = 1 kHz		78		dB
			f = 10 kHz		63		dB
			f = 100 kHz		51		dB
			f = 1 MHz		39		dB
V_N	Output Noise Voltage	BW = 10 Hz to 100 kHz, V_{IN} = 3.8 V, V_{OUT} = 3.3 V, I_{OUT} = 100 mA, C_{NR} = 470 nF, C_{FF} = 470 nF			4.9		μV_{RMS}
Temperature Range							
T_{SD}	Thermal Shutdown Threshold	Temperature increasing			165		°C
	Hysteresis				20		°C

(1) Minimum V_{IN} = $V_{OUT(NOM)}$ + V_{DO} or 2.2 V, whichever is greater.
(2) For adjustable output voltage version only.
(3) Resistor tolerance is not included. Output accuracy is not tested at this condition: V_{OUT} = 0.8 V, 4.5V ≤ V_{IN} ≤ 5.5 V, and 750 mA ≤ I_{OUT} ≤ 1 A, because the power dissipation is out of package limitation.
(4) Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current and measure for VOUT(NOM) ≥ 2.2V. In dropout mode, the output voltage will be equal to V_{IN} – V_{DO}.

Typical Performance Characteristics

All test conditions: V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2.2 V, whichever is greater; C_{IN} = C_{OUT} = 4.7 µF, C_{NR} = 470 nF, C_{FF} = 470 nF, −40°C ≤ T_A ≤ +125°C, unless otherwise noted.

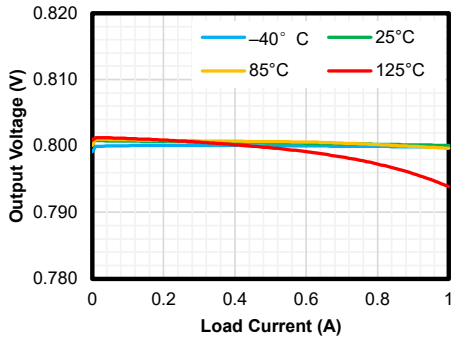


Figure 1. Load Regulation

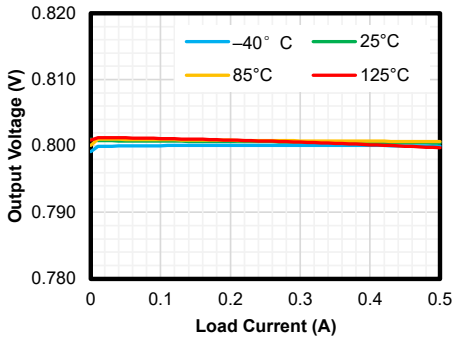


Figure 2. Load Regulation at Light Load

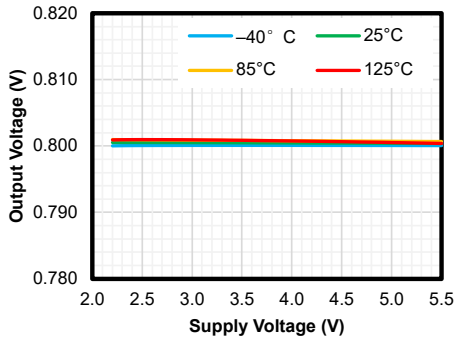


Figure 3. Line Regulation

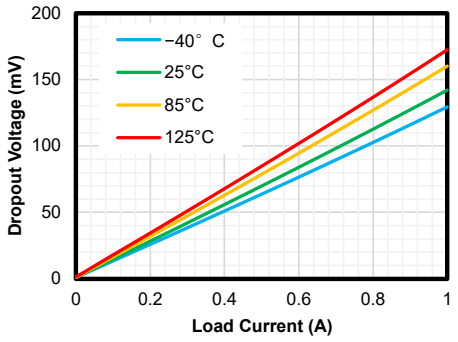


Figure 4. Dropout Voltage vs. Load Current

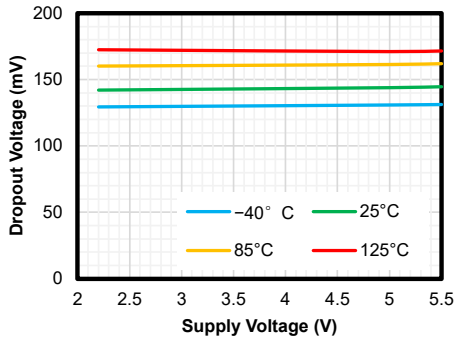


Figure 5. Dropout Voltage vs. Supply Voltage

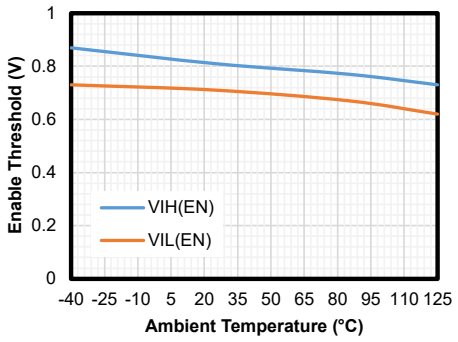


Figure 6. Enable Threshold vs. Temperature

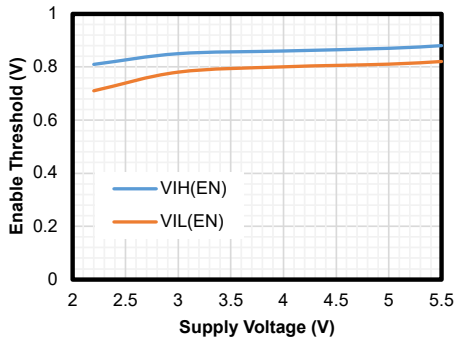


Figure 7. Enable Threshold vs. Supply Voltage

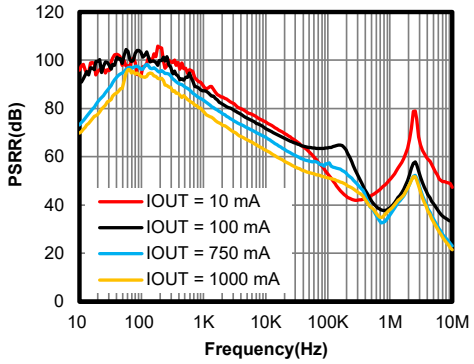


Figure 8. PSRR

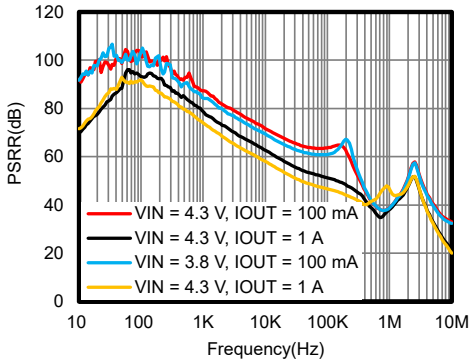


Figure 9. PSRR

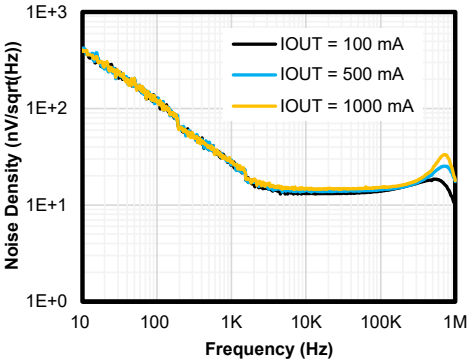
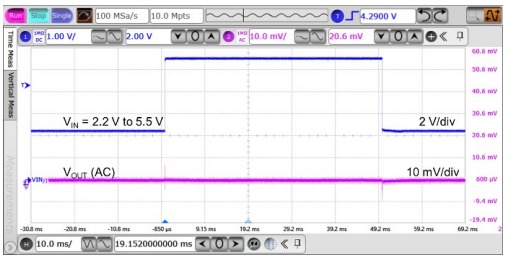


Figure 10. Noise



V_{IN} = 2.2 V to 5.5 V, V_{OUT} = 0.8 V

Figure 11. Line Transient

I_{OUT} = 1 mA to 1 A, V_{OUT} = 0.8 V

Figure 12. Load Transient

Detailed Description

Overview

The TPL910Q series is a 1-A high-current, 4.9-μV_{RMS} low-noise, 78-dB high-PSRR linear regulator with 500-mV maximum ultra-low dropout voltage at 1-A load current. The TPL910Q supports adjustable output voltage ranging from 0.8 V to 5 V with an external resistor divider.

Ultra-low noise, high PSRR, and high output current capabilities make the TPL910Q the ideal power supply for noise-sensitive applications, such as high-speed communication facilities, and high-definition imaging equipment. With accurate output voltage tolerance, excellent transient response, and adjustable soft-start control, the TPL910Q is an optimal power supply for the large-scale processors or digital loads, such as automotive ECUs.

Functional Block Diagram

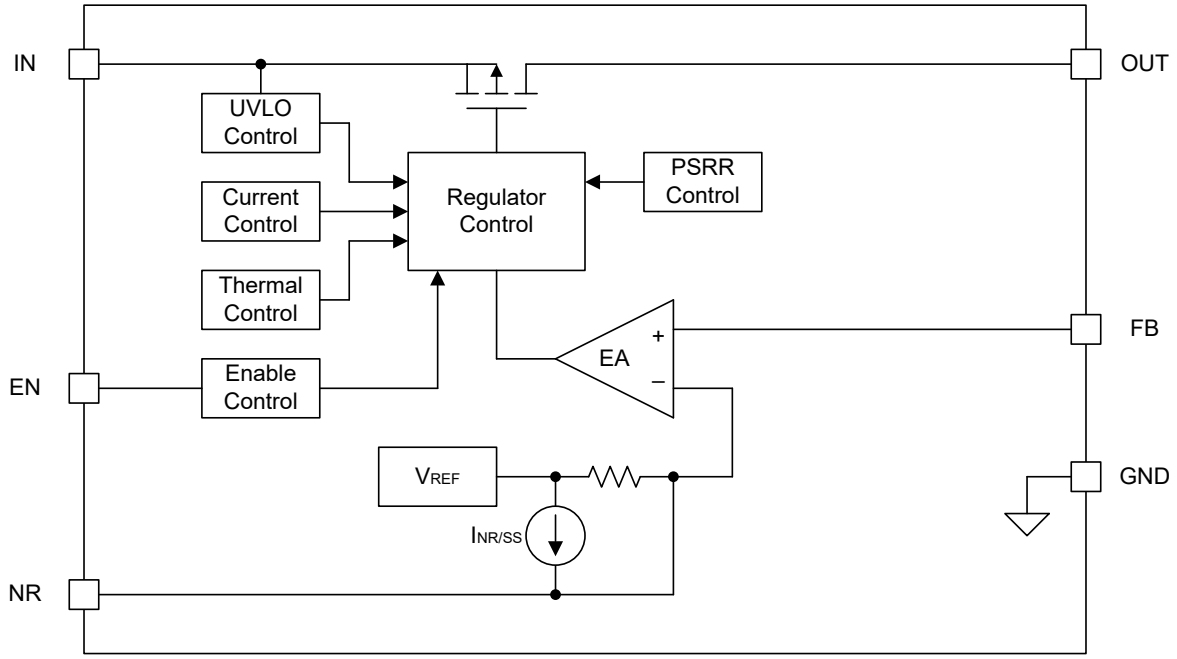


Figure 13. Functional Block Diagram

Feature Description

Enable (EN)

The TPL910Q series provides a device enable pin (EN) to enable or disable the device. Connect this pin to the GPIO of an external digital logic control circuit to control the device. When the VEN voltage falls below $V_{IL(EN)}$, the LDO device turns off. When the V_{EN} ramps above $V_{IH(EN)}$, the LDO device turns on.

Under-Voltage Lockout (IN and UVLO)

The TPL910Q series uses an under-voltage lockout circuit to shut off the output until the internal circuitry operates properly. Refer to the Electrical Characteristics table for UVLO threshold and hysteresis.

Adjustable Output Voltage (OUT and FB)

The TPL910Q series is also available in adjustable voltage versions of 0.8 V to 5 V. Using external resistors divider, the output voltage of the TPL910Q series is determined by the value of the resistors R1 and R2 in Figure 14. Use Equation 1 to calculate the output voltage.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

Where the feedback voltage VFB is 0.8 V.

Table 2 provides a list of recommended resistor combinations to achieve the common output voltage values.

Table 2. External Resistor Combinations

Target Output Voltage (V)	External Resistors Divider		Calculated Output Voltage (V)
	R1 (kΩ)	R2 (kΩ)	
0.8	0	Open	0.800
1.0	12.4	49.9	0.999
1.2	12.4	24.9	1.198
1.5	12.4	14.3	1.494
1.8	12.4	10	1.792
2.5	12.4	5.9	2.481
3.3	11.8	3.74	3.324
5.0	12.4	2.37	4.986

Programmable Soft Start

The TPL910Q series integrates a programmable soft-start function to control the output voltage ramp-up slew rate and start-up time. By selecting the external capacitor at the NR/SS pin, the output start-up time can be calculated with Equation 2.

$$t_{Start-Up} = 1.25 \times \frac{V_{NR/SS} \times C_{NR/SS}}{I_{NR/SS}} \quad (2)$$

Where, the typical value of VNR/SS is 0.8 V, the typical value of INR/SS is 6 μA, and CNR/SS is the external capacitor at the NR/SS pin.

Over-Current Protection and Short-to-Ground Protection

The TPL910Q series integrates an internal current limit that helps to protect the regulator during fault conditions.

- When the output voltage is pulled down below the regulated voltage, over-current protection starts to work and limits the output current to I_{LIM}.
- When the output voltage is pulled down below the short-to-ground threshold, or shorted to the ground directly, short-to-ground protection starts to work and limits the output current to I_{SC}.
- During startup, the output current is limited to I_{SC} before the output voltage ramps higher than the short-to-ground threshold.

Under the over-current conditions, the internal junction temperature ramps up quickly. When the junction temperature is high enough, it will cause over-temperature protection.

Over-Temperature Protection

The over-temperature protection starts to work when the junction temperature exceeds the thermal shutdown (TSD) threshold, which turns off the regulator immediately. The regulator turns on again when the device cools down and the junction temperature falls below the value which equals to thermal shutdown threshold minus thermal shutdown hysteresis.

According to the Recommended Operating Conditions table, the junction temperature range should be limited; continuously operating above the junction temperature range will reduce the device's lifetime.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPL910Q series products is a 1-A high-current, 4.9-μV_{RMS} low-noise, 78-dB high-PSRR linear regulator with 500-mV maximum ultra-low dropout voltage. The following application schematic shows a typical usage of the TPL910Q.

Typical Application

Figure 14 shows the typical application schematic.

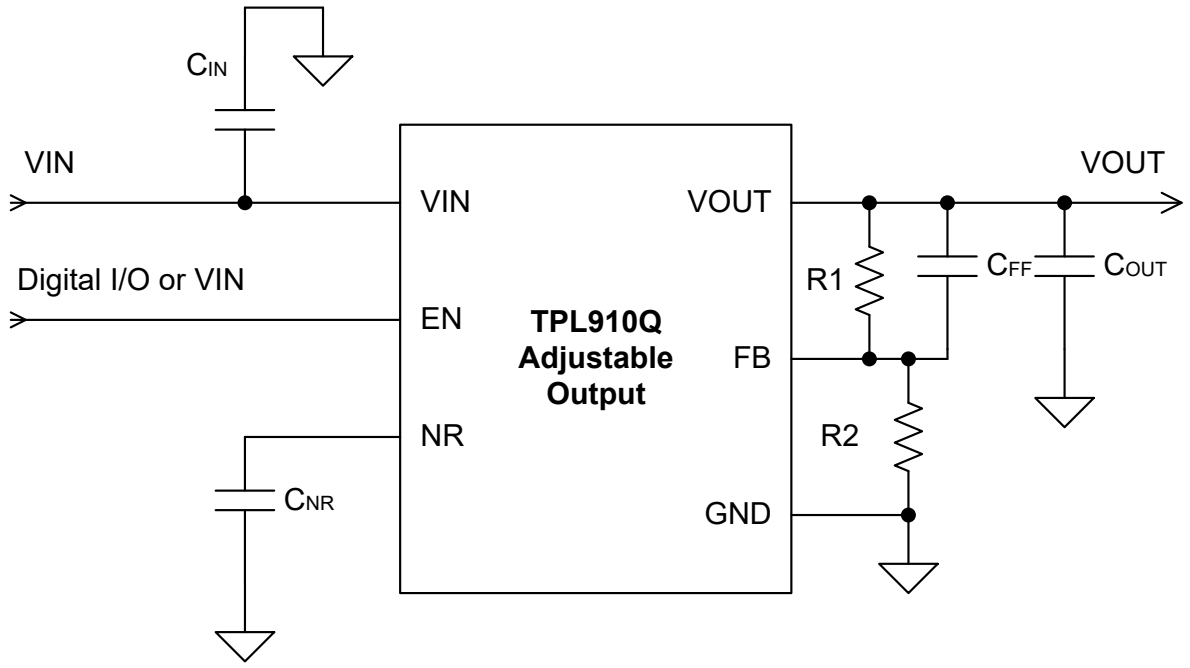


Figure 14. Typical Application Circuit

Input Capacitor and Output Capacitor

The TPL910Q series is designed to be stable with low equivalent series resistance (ESR) ceramic capacitors at the input, output, and noise-reduction pin (NR/SS). It is recommended to use ceramic capacitors with X7R-, X5R-, and COG-rated dielectric materials to get good capacitive stability across the temperature range.

3PEAK recommends adding a 10-µF or greater capacitor with a 0.1-µF bypass capacitor in parallel at the IN pin to keep the input voltage stable. The voltage rating of the capacitors must be greater than the maximum input voltage.

To ensure loop stability, the TPL910Q requires a minimum 4.7-µF low ESR output capacitor. 3PEAK recommends selecting an X7R-type 10-µF ceramic capacitor with low ESR over temperature.

Both input capacitors and output capacitors must be placed as close to the device pins as possible.

Power Dissipation and Thermal Consideration

During normal operation, LDO junction temperature should meet the requirement in the Recommended Operating Conditions table. Using Equation 3 and Equation 4 to calculate the power dissipation and estimate the junction temperature.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad (3)$$

The junction temperature can be estimated using Equation 4. θ_{JA} is the junction-to-ambient thermal resistance.

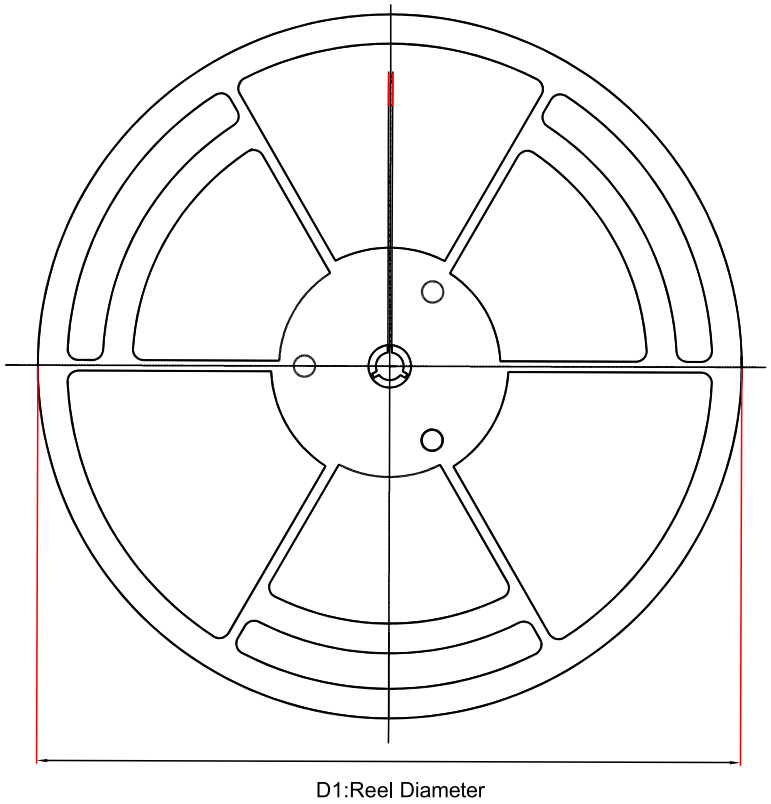
$$T_J = T_A + P_D \times \theta_{JA} \quad (4)$$

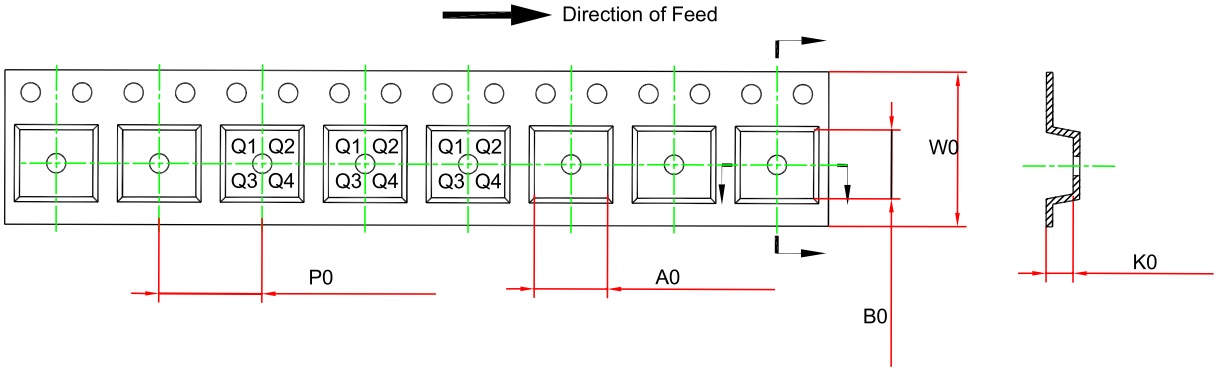
Layout

Layout Guideline

- Both input capacitors and output capacitors must be placed as close to the device pins as possible, and vias between capacitors and device power pins must be avoided.
- It is recommended to bypass the input pin to the ground with a 0.1-μF bypass capacitor. The loop area formed by the bypass capacitor connection, the IN pin, and the GND pin of the system must be as small as possible.
- It is recommended to use wide and thick copper to minimize I×R drop and heat dissipation.

Tape and Reel Information



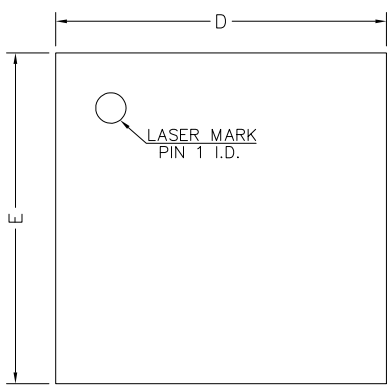


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPL910ADJQ-DF6R-S	DFN3X3-8	330.0	17.6	3.4	3.4	1.1	8.0	12.0	Q2

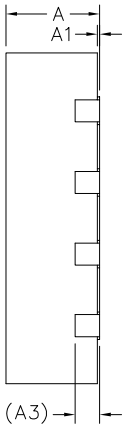
Package Outline Dimensions

DFN3X3-8

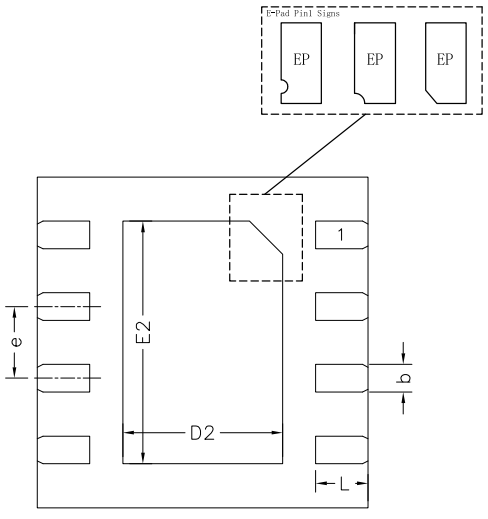
Package Outline Dimensions DFC(DFN3X3-8-F)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	0.900	0.031	0.035
A1	0.000	0.050	0.000	0.002
b	0.200	0.300	0.008	0.012
A3	0.150	0.250	0.006	0.010
D	2.900	3.100	0.114	0.122
D2	1.350	1.600	0.053	0.063
E	2.900	3.100	0.114	0.122
E2	2.100	2.350	0.083	0.093
e	0.650 BSC		0.026 BSC	
L	0.425	0.525	0.017	0.021

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPL910ADJQ-DF6R-S	−40 to 150°C	DFN3X3-8	L91AQ	MSL3	4,000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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