Features

- AEC-Q100 Grade-1 Qualified (TPM2025Q Only)
- Dual Independent Channels
- 5-V Single Supply with Optimized Output Damping for Gan Reliability
- 7-A Peak Source And 5-A Sink-Drive Current
- 0.69-ns Minimum Input Pulse Width (Typical)
- Low Propagation Delay (2-ns Typical)
- Optimized Pinout for nanosecond-pulse-width
- Fast Rise and Fall Times (0.45-ns and 0.45-ns Typical)
- <0.61-ns Typical Delay Matching Between Two Channels
- ESD Protection Exceeds JESD 22 – 6-kV HBM, 1.5-kV CDM
- Available in Flip-Chip QFN2X2-10 Package

Applications

- Laser Distance Measuring System
- Automotive Lidar
- Driver Monitoring System
- GaN DC/DC Conversion System

Description

The TPM2025 / TPM2025Q family are low-side dual-channel ultra-highspeed gate drivers for GaN and logic-level MOSFETs. It is optimized for high-speed applications such as Lidar and high-density power convertors with enhanced low propagation delay design. The TPM2025's 2-mm×2-mm flip-chip QFN package minimizes parasitic inductance in the gate driver power loop and achieves state-of-the-art narrow pulse width as short as 0.69 ns. Channel independent transient suppressors ensure reliable operation with ultra-fast high-current output pulses.

Typical Application Diagram

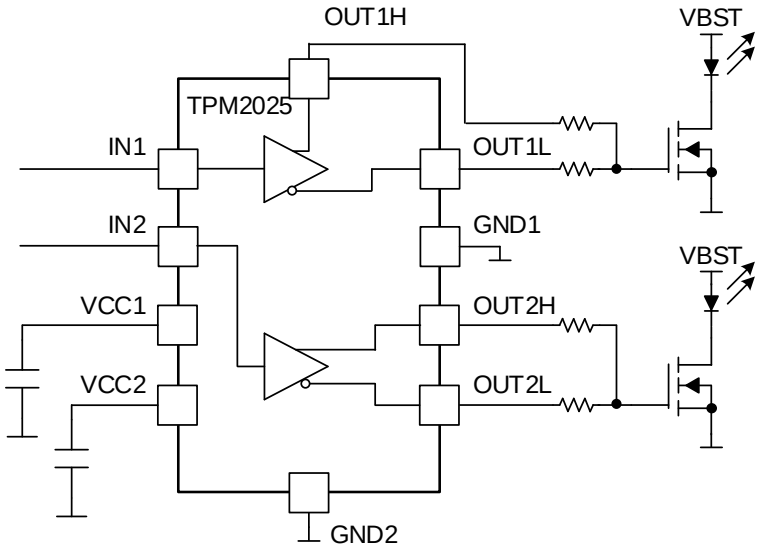


Figure 1 Typical Application Diagram

Table of Contents

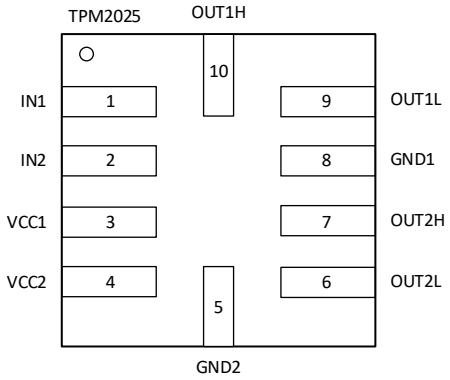
Revision History

Date	Revision	Notes
2021/07/15	Rev. A.0	Initial release
2023/02/28	Rev. A.1	Updated TPM2025Q orderable part number. Updated electrical characteristics on timing footnotes.
2023/07/10	Rev. A.2	Added transient voltage rating
2023/08/07	Rev. A.3	Added ground description and truth table. Block diagram amendment on signal polarity.

Pin Configuration and Functions

QFN2X2-10

Top View



Pin Functions

Pin		I/O	Description
No.	Name		
1	IN1	Input	Channel 1 Input, Active High
2	IN2	Input	Channel 2 Input, Active High
3	VCC1	Supply	Device Supply for Channel 1
4	VCC2	Supply	Device Supply for Channel 2
5	GND2	Ground	Device Ground for Channel 2
6	OUT2L	Output	Channel 2 Pull-down Output
7	OUT2H	Output	Channel 2 Pull-up Output
8	GND1	Ground	Device Ground for Channel 1
9	OUT1L	Output	Channel 1 Pull-down Output
10	OUT1H	Output	Channel 2 Pull-up Output

Specifications

Absolute Maximum Ratings

Parameters	Rating
Power Supply Voltage, VCC1, VCC2	−0.3 V to 6 V
Power Supply Voltage Difference，VCC1 – VCC2	−6 V to 6 V
Ground Difference, GND1 – GND2	–0.3V to 0.3V
Output Voltage Range OUT1H, OUT1L	–0.3V to VCC1+0.3V
Output Voltage Range OUT1H, OUT1L, 5-ns Transient	–5V to VCC1+5V
Output Voltage Range OUT1H, OUT1L, 10-ns Transient	–2V to VCC1+2V
Output Voltage Range OUT2H, OUT2L	–0.3V to VCC2+0.3V
Output Voltage Range OUT2H, OUT2L, 5-ns Transient	–5V to VCC2+5V
Output Voltage Range OUT2H, OUT2L, 10-ns Transient	–2V to VCC2+2V
Input Voltage Range IN1, IN2	−0.3 V to 6 V
Continuous Output Channel Current OUT1H, OUT2H, OUT1L, OUT2L	–500 mA to 500 mA
Pulsed Output Channel Sourcing Current OUT1H, OUT1H (500 ns)	7 A
Pulsed Output Channel Sourcing Current OUT1H, OUT1H (500 ns)	5 A
Operating Junction Temperature Range	–40 °C to 150 °C
Storage Temperature Range	–65 °C to 150 °C
Lead Temperature (Soldering, 10 sec)	260 °C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
Note 2: The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 300 mV beyond the power supply, the input current should be limited to less than 10mA.
Note 3: Power dissipation and thermal limits must be observed.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001，per AEC Q100-002	±6	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002, per AEC Q100-011	±1.5	kV

Recommended Operation Conditions

Parameters	Rating

Power Supply Voltage, VCC1, VCC2	4.75 V to 5.25 V
Power Supply Voltage Difference VCC1 – VCC2, GND1 – GND2	0 V
Input Voltage IN1, IN2	0 V to VCC
Output Voltage VOUT1H, VOUT1L, VOUT2H, VOUT2L	0 V to VCC
Operating Ambient Temperature Range	–40 °C to 125 °C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
QFN2X2-10	87.54	119.32	°C/W

Electrical Characteristics

All test condition is V_{CC} = 5 V, T_J = −40 °C – 150 °C, 1-µF capacitor between V_{CC} and GND, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_Q	VCC Quiescent Current	IN1 = H, IN2 = H		105	200	µA
		IN1 = L, IN2 = L		105	200	
I_{OP}	VCC Operating Current	f_{SW} =30 MHz, no load, R_{OUTH} = 2 Ω, R_{OUTL}= 2 Ω		40		mA
		f_{SW} =30 MHz, 100-pF load, R_{OUTH} = 2 Ω, R_{OUTL}= 2 Ω		51		mA
V_{UVLO_rising}	Supply Under Voltage Lock Out rising threshold		4	4.18	4.35	V
V_{UVLO_hys}	Supply Under Voltage Lock Out falling hysteresis			85		mV
T_{OTP}	Over temperature shutdown, turn-off			170		°C
ΔT_{OTP}	Over temperature hysteresis			20		°C
V_{IN_H}	Input signal high threshold	Input high threshold	1.7	2.15	2.6	V
V_{IN_L}	Input signal low threshold	Input low threshold	1.1	1.45	1.8	V
V_{IN_HYS}	Input hysteresis		0.38		1	V
$R_{IN\_pulldown}$	Input pull-down resistance		100	150	250	kΩ
C_{IN}	Input capacitance				1.5	pF
V_{OL}	Output low voltage. OUTxL	I_{OUTxL} = 100 mA, INx = 0 V			36	mV
$V_{CCx} – V_{OHx}$	Output high voltage, OUTxH	I_{OUTxH} = 100 mA, INx = 5 V			50	mV
I_{OH}	Output Peak Sourcing Current	V_{OUTxH} = 0 V, INx = 5 V		7		A
I_{OL}	Output Peak Sinking Current	V_{OUTxL} = 5 V, INx = 0 V		5		A
T_{start}	Startup Time, VDD rising above UVLO	INx = 5 V ,VDD rising above UVLO to OUTH rising		40	78	us
$T_{shut-off}$	ULVO falling	INx = 5 V ,VDD falling below UVLO V to OUTH falling	0.7	2.5	3.5	us
$T_{pd,r}$ (1)	Propagation delay, turn on	INx to OUTH, 100-pF load		2	4	ns
$T_{pd,f}$ (1)	Propagation delay, turn off	INx to OUTL, 100-pF load		2	4	ns
Δt_{pd}	Pulse positive distrortion, ($t_{pd,f}$ - $t_{pd,r}$)			300	610	ps
t_R	Output rise-time	0Ω series 220 pF load		450		ps
t_F	Output fall-time	0Ω series 220 pF load		450		ps
t_{PW}	Minimum input pulse width that changes output state	0Ω series 220 pF load		0.69		ns

(1) Guranteed by design.

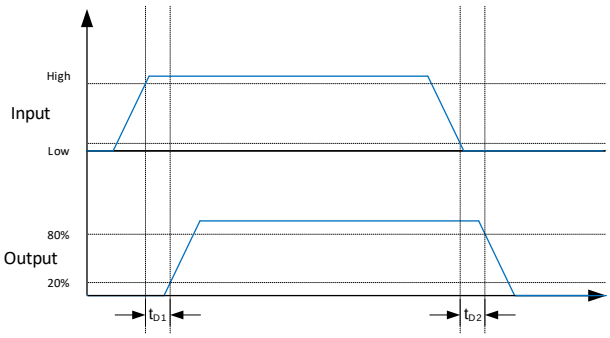


Figure 2 Input Timing Diagram

Typical Performance Characteristics

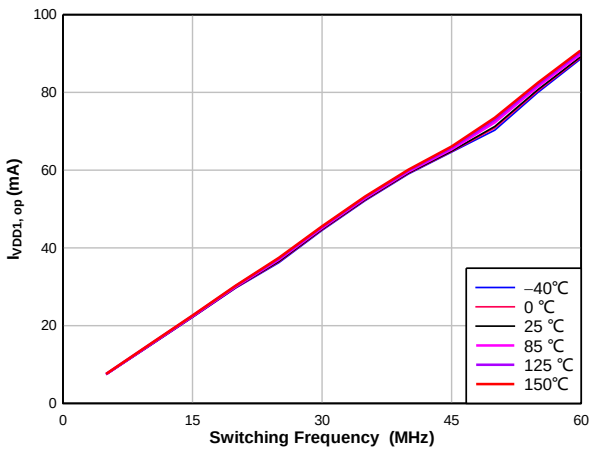


Figure 3. Operating current vs Temperature

2Ω in series with 100pF Load

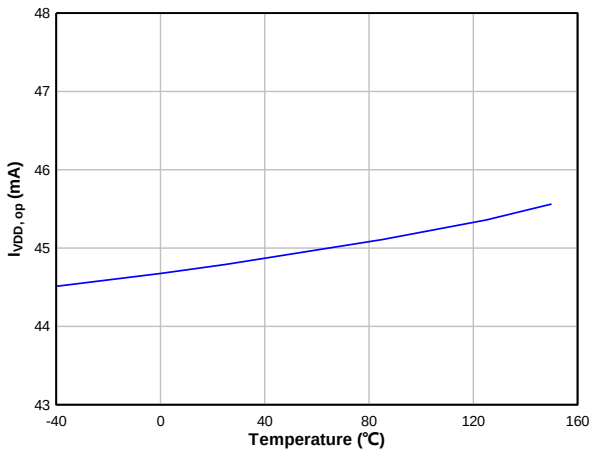


Figure 4. Operating Current vs Temperature

2Ω in series with 100pF Load, f = 30 MHz

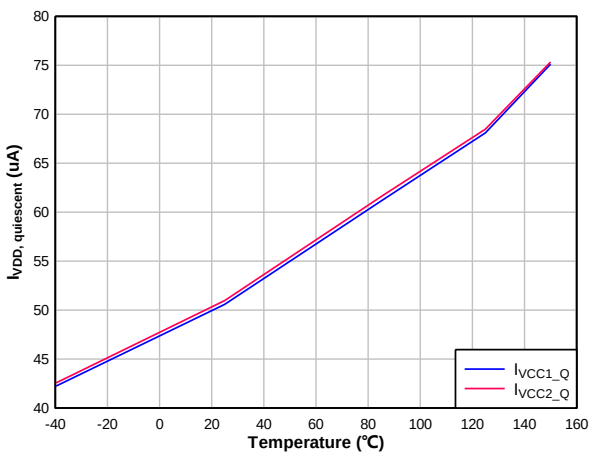


Figure 5. Quiescent current vs Temperature

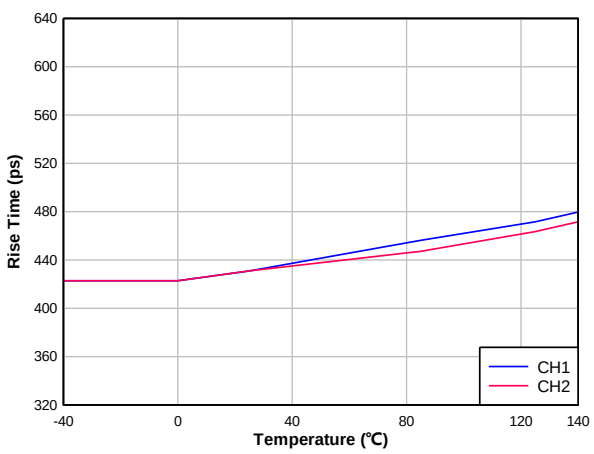


Figure 6. Rise time vs Temperature, load = 1.8nC

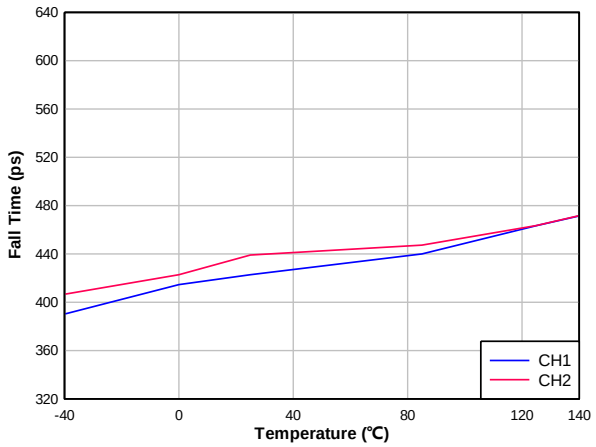


Figure 7. Fall time vs Temperature, load = 1.8nC

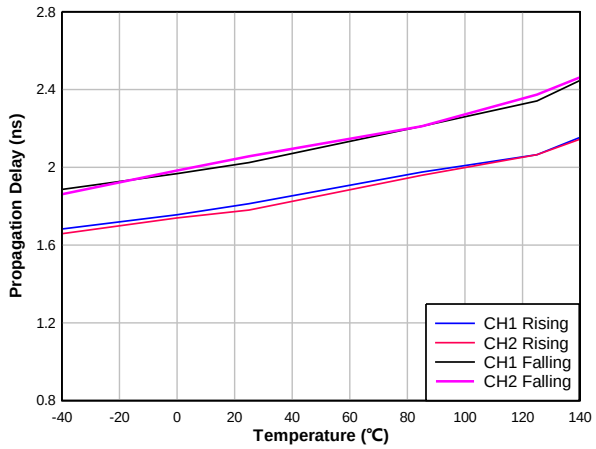


Figure 8. Propagation Delay vs Temperature, load = 1.8nC

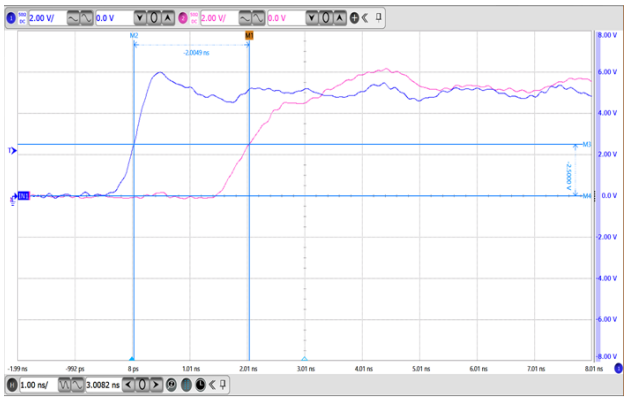


Figure 9. Rising Edge

CH1: Input; CH2: GaN Transistor Gate

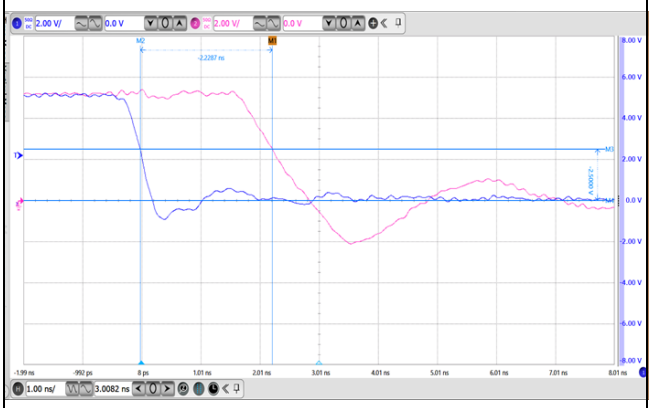


Figure 10. Falling Edge

CH1: Input; CH2: GaN Transistor Gate

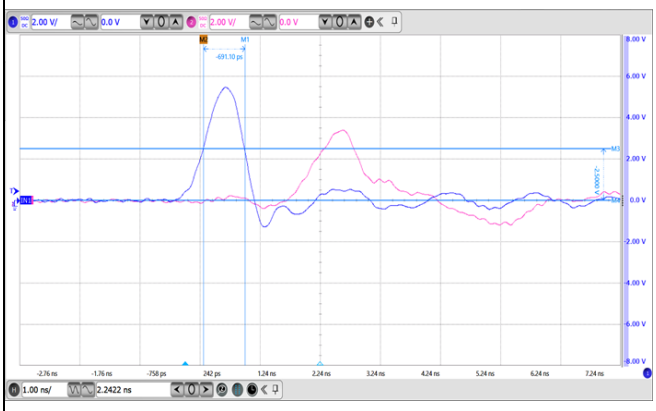


Figure 11. 0.69-ns Minimal Pulse Width

CH1: Input; CH2: GaN gate; GaN = EPC2122; C_{ISS} = 339pF

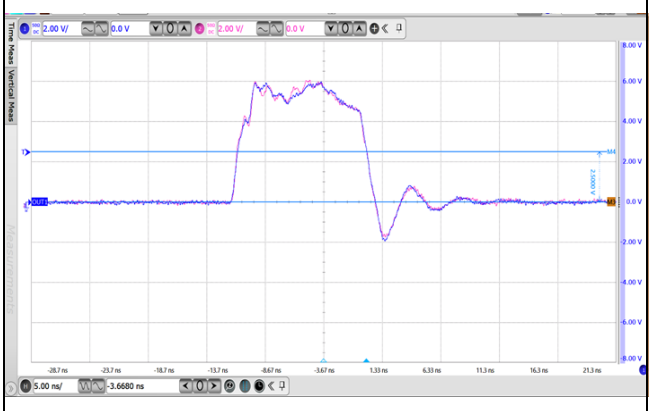


Figure 12. Channel Mismatch

CH1: Channel 1 Output; CH2: Channel 2 Output; GaN = EPC2122; C_{ISS} = 339pF

Detailed Description

Overview

The TPM2025 is a low-side dual-channel ultra-highspeed gate driver for GaN and logic-level MOSFETs. It is optimized for high-speed applications such as Lidar and high-density power convertors with enhanced low propagation delay design. The TPM2025's 2-mm×2-mm flip-chip QFN package minimizes parasitic inductance in the gate driver power loop and achieves state-of-the-art narrow pulse width as low as 0.69 ns. Channel independent transient suppressors ensure reliable operation with ultra-fast high-current output pulse.

Functional Block Diagram

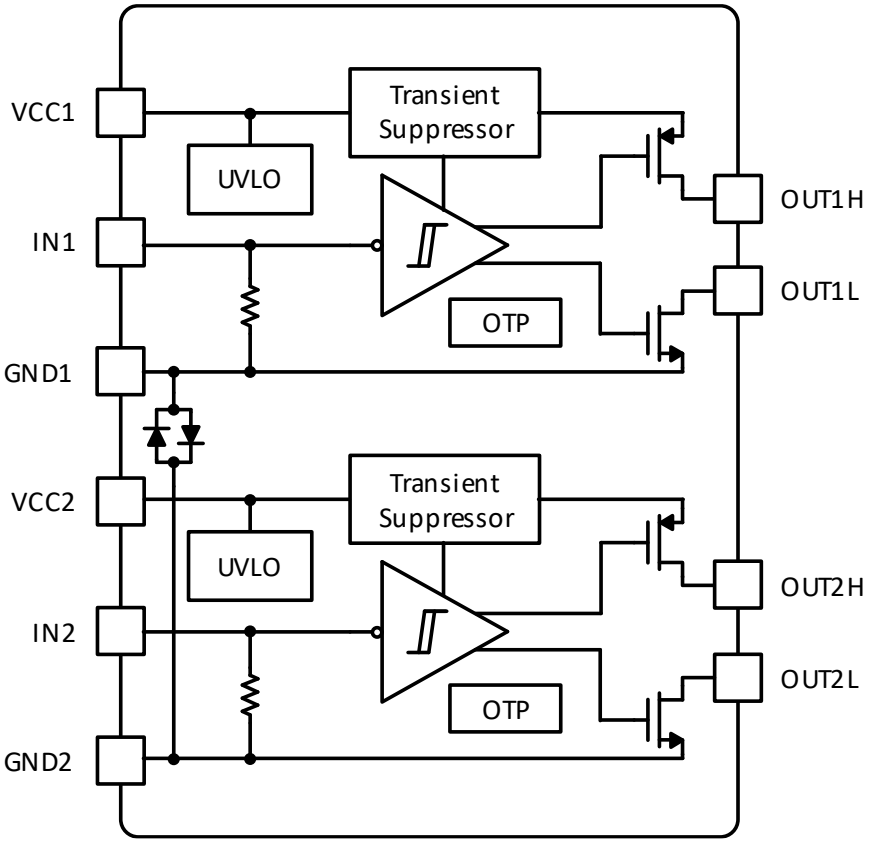


Figure 13 Functional Block Diagram

Feature Description

Supply and Under-Voltage-Lock-Out (UVLO)

The device has dual supply inputs that are dedicated for each channel independently, to avoid interferences between channels during operations. The two ground paths for the dual channels are connected via back-to-back diodes.

Each channel has its own under-voltage-lock-out (UVLO) monitors. When supply voltage is above its rising threshold, the outputs are functional. When supply voltage is below its falling threshold, the device pulls OUTxL to GND. A short deglitch timer is inserted to avoid oscillations on power supply.

Due to ultra-fast turn-on speed, channel output may drain high current on supply nodes within nanoseconds.

3PEAK recommends placing 3-terminal capacitors close to device supply pins as low as possible. Parasitic inductance may prevent external capacitors from supplying current in such short time, the TPM2025 has built in transient suppressor circuitry to avoid sudden drop which may trigger UVLO and cause output malfunction.

TPM2025 provides dual device ground connection with back-to-back diodes to minimize channel-to-channel interference via internal ground connections. 3PEAK recommends connect GND1 and GND2 externally together with low impedance.

Channel Input and Output

The channel inputs are connected to a low-latency Schmitt trigger. It can cut propagation delay without additional gates. The inputs are pulled low via internal resistors.

The TPM2025 provides dual outputs with split pull-up and pull-down paths. The split outputs allow users to independently configure pull-up and pull-down slew-rate via external resistors. The maximum current the output can sink/source is +7 / −5 A. Configuring slew rates may reduce ringing on GaN gate node due to parasitic inductance/capacitance, thus it can improve reliability of GaN transistors.

Table 1 Output Truth Table

Inputs (INx)	OUTxH	OUTxL
H	H	High-Impedance
L	High-Impedance	L
Floating (Internal Pull Down)	High-Impedance	L

Channel Output in Parallel

To achieve higher pull-up current while still maintain short current path, the TPM2025 could support driving highside outputs together, as depicted in below diagram. OUT1L could be left floating in this case.

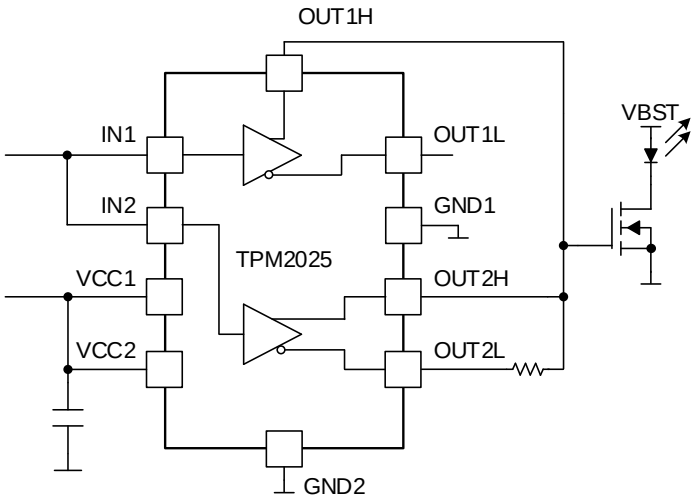


Figure 14 Parallel Output Pull-up

Over Temperature Protection (OTP)

The TPM2025 provides independent over temperature protection function to independently disable each channel. When junction temperature rises above rising threshold, the channel outputs are disabled; when junction temperature falls below falling threshold, the channel outputs are enabled.

Application and Implementation

NOTE

Information in the following applications sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

In modern Time-of-Flight (ToF) LiDAR system, it is necessary to ensure a narrow laser pulse. Gallium nitride (GaN) transistors are widely used in the industry due to its high switching frequency. As depicted in below schematic, it is required to keep gate driver output loop as small as possible to minimize parasitic inductance.

Typical Application

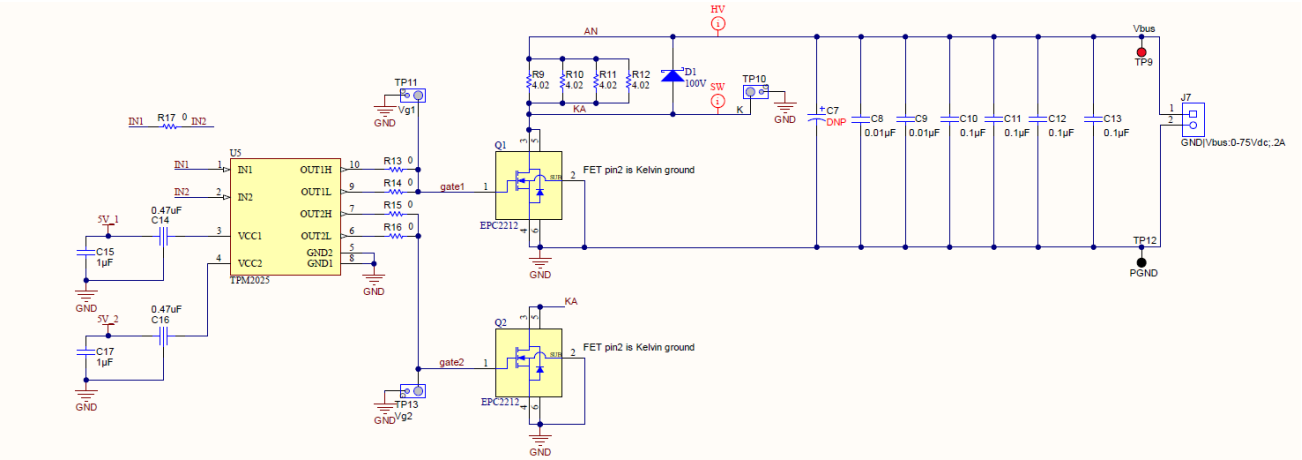
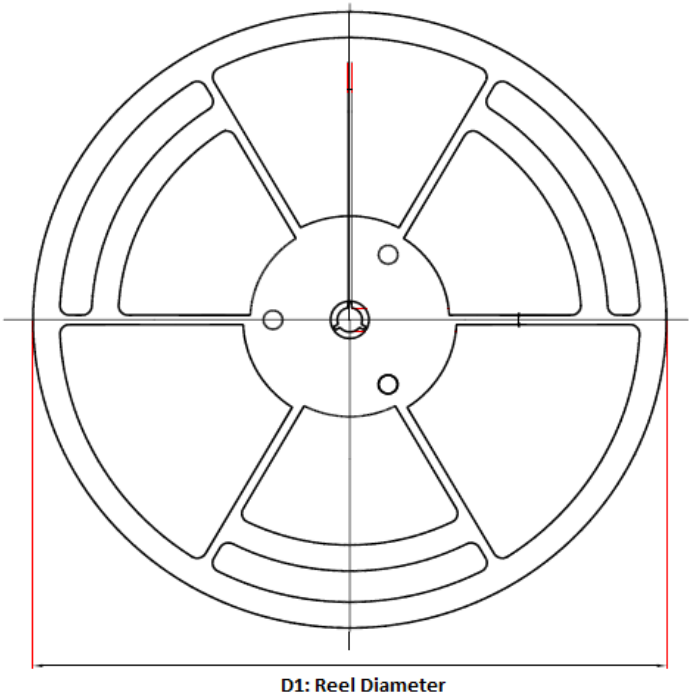


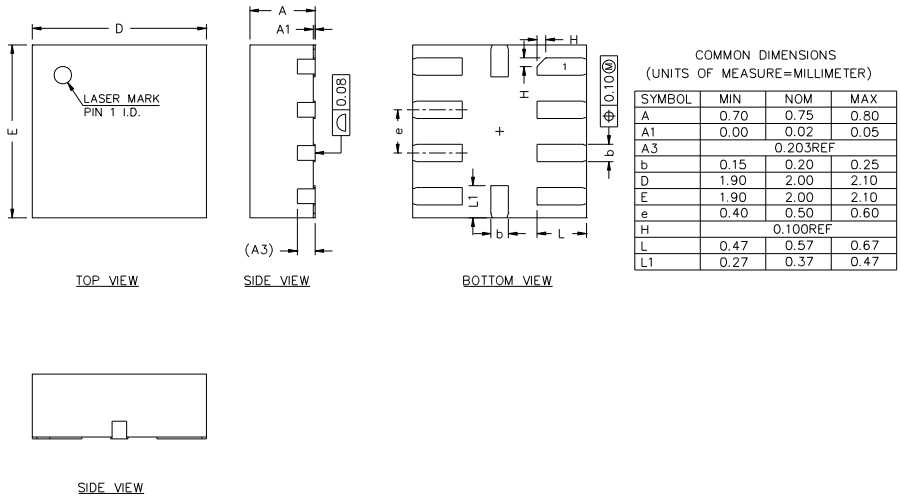
Figure 15 Typical Lidar Application Schematic

Tape and Reel Information



Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPM2025Q-FC1R-S	QFN2X2-10	178	11.1	2.3	2.3	1.0	4	8	Q1
TPM2025-FC1R	QFN2X2-10	178	11.1	2.3	2.3	1.0	4	8	Q1

Package Outline Dimensions



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203REF	
b	0.15	0.20	0.25
D	1.90	2.00	2.10
E	1.90	2.00	2.10
e	0.40	0.50	0.60
H		0.100REF	
L	0.47	0.57	0.67
L1	0.27	0.37	0.47

Order Information

Order Number	Operating Ambient Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity
TPM2025Q-FC1R-S	–40 °C to 125 °C	QFN2X2-10	Q25	MSL3	3000
TPM2025-FC1R	–40 °C to 125 °C	QFN2X2-10	M25	MSL3	3000

Note: Ambient temperature indicates device operation condition range. Application thermal behavior needs to be taken care of when operating in high temperature scenarios.

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