48-V 8-Ch Smart Low-side Driver Array with Diagnostics and CRC

Features

- 8-Channel Smart Low-side Driver Array
  - 500-mΩ Low-$R_{DS(ON)}$ with Maximum 1.5-A Driver Capability
  - 40-V Max Recommended Operating Voltage, 48-V Absolute Max Voltage
  - Integrated Free-wheeling Diodes for Inductive Loads
  - Parallel Channel Driving Capability
  - Dual Supply VM and VCLAMP for Inductive Loads
- 10-MHz High-speed 16-bit Serial Interface with CRC
  - Input Noise Filtering with Daisy-chain Communication
  - 4 Independent PWM Input with PWM Mapping
  - Cyclic Redundancy Check (CRC) for Serial Communication and Registers
  - Register Content Protection Lock
  - Register Map ReadBack Capability
- Enhanced Diagnostics and Protection
  - Power-on Reset
  - Over-Current Protection
  - Short-Circuit Protection
  - Channel Individual Open and Short Diagnostics with Fault Masking
  - Over-Temperature Protection
  - Open-Drain Fault Alarm with Forced Fault

Applications

- Relays, Solenoids, Unipolar Stepper Motors
- Electric Expansion Valves, Linear Valves
- LEDs and Heaters
- PLC Digital Outputs
- Electromagnetic Loads

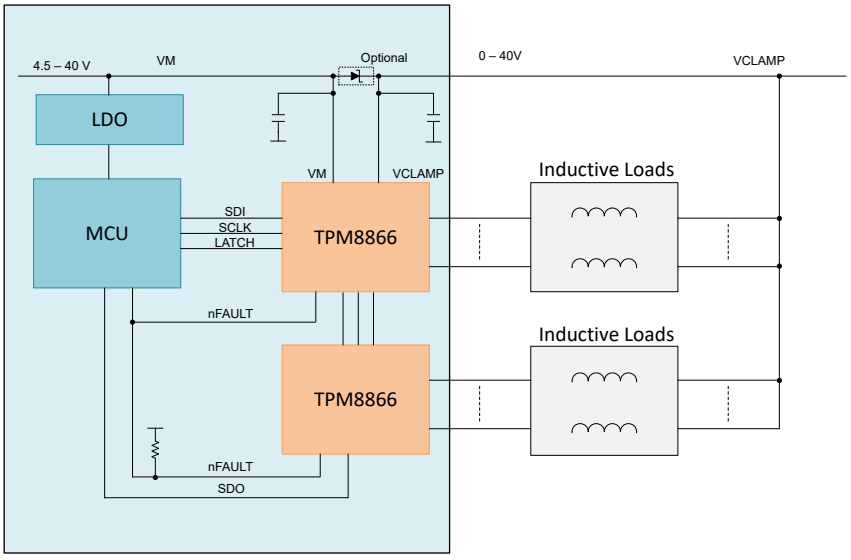
Description

The TPM8866 provides an 8-ch low-side driver with channel-independent protection and diagnostics. It has a low a $R_{DS(ON)}$ MOSFET array with free-wheeling diodes to support all kinds of loads, resistive, inductive, and capacitive. It supports dual high-voltage supplies, VM, and VCLAMP.

It supports a high-speed serial interface with a daisy chain and CRC to individually control and diagnose each channel. Over-current protection, short circuit, and open circuit allow the controller to protect the system and identify faulty loads. Open-drain fault output allows the controller to respond to fault senario with interrupt input.

Communication CRC, register map CRC and register lock feature can prevent accidental changes by noises in the industrial environment and improve system reliability. Multiple devices can be connected in daisy-chain configuration to save MCU I/Os. The device also provides undervoltage lockout and over-temperature shutdown protection.

Typical Application Circuit



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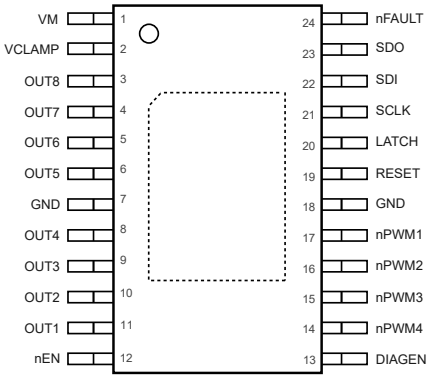
Revision History

Date	Revision	Notes
2024-02-01	Rev.A.0	Initial release

Pin Configuration and Functions

TPM8866-TSDR
ETSSOP24 Package
Top View



TPM8866-TS5R
TSSOP24 Package
Top View

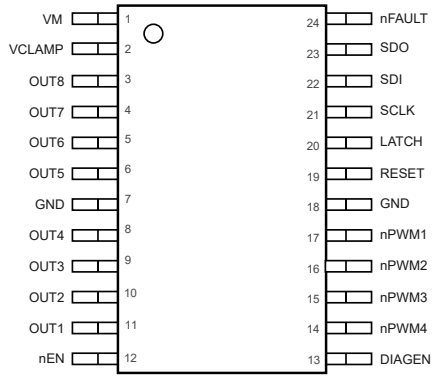


Table 1. Pin Functions: TPM8866

Pin	Name	I/O	Description
1	VM	P	Motor power supply, connect to a 10-μF capacitor with a 0.1-μF capacitor close to the VM pin.
2	VCLAMP	P	Connect directly or through a zener diode to VM, recommended to add clamp zener to GND for inductive energy.
3	OUT8	O	Output channel 8.
4	OUT7	O	Output channel 7.
5	OUT6	O	Output channel 6.
6	OUT5	O	Output channel 5.
7	GND	G	Device ground.
8	OUT4	O	Output channel 4.
9	OUT3	O	Output channel 3.
10	OUT2	O	Output channel 2.
11	OUT1	O	Output channel 1.
12	nEN	I	Internal pull-down, active-low output enable. Logic 1: all outputs disabled. Logic 0: all outputs enabled
13	DIAGEN	I	Internal pull-down, active-high diagnostics enable. Logic 1: diagnostics enabled, Logic 0: diagnostics disabled with fault flag cleared.
14	nPWM4	I	Internal pull-down, active-low PWM4 input.
15	nPWM3	I	Internal pull-down, active-low PWM3 input.
16	nPWM2	I	Internal pull-down, active-low PWM2 input.
17	nPWM1	I	Internal pull-down, active-low PWM1 input.
18	GND	G	Device ground.

Pin	Name	I/O	Description
19	RESET	I	Internal pull-down active-high device reset. Logic 1: internal logic reset; Logic 0: device normal operation.
20	LATCH	I	Serial interface device selection LATCH input.
21	SCLK	I	Serial interface serial clock SCLK input.
22	SDI	I	Serial interface serial clock data input.
23	SDO	O	Serial interface data output, push-pull output.
24	nFAULT	OD	Open-drain active-low fault output, connect a 10-kΩ pull-up resistor to MCU supply voltage.

Specifications

Absolute Maximum Ratings

Parameter		Min	Max	Max
VM, VCLAMP	Power Supply Voltage	−0.3	48	V
	Power Supply Voltage (100-ns Pulse)	−0.3	50	V
nEN, nPWMx, DIAGEN, RESET, LATCH, SCLK, SDI	Input Voltage	−0.3	5.75	V
SDO, nFAULT	Logic Output Voltage	-0.3	5.75	V
V_{OUTx}	Output Voltage	−0.3	+48	V
	Output Voltage (100-ns Pulse)	−0.3	+50	V
I_{OUT}	DC Current		1.5	A
	Peak Current	Internally Limited		
I_{CLAMP}	Total Clamp Current		4	A
I_{GND}	Total GND Current		4	A
T_J	Maximum Junction Temperature		150	°C
T_A	Operating Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	4	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	1	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Max	Unit
VM, VCLAMP	Power Supply Voltage	5	40	V
INx, PWMx, SDI, SCLK, LATCH	Logic Input Voltage	0	5	V
SDO, nFAULT	Open Drain Output Voltage	0	5	V
V_{OUTx}	Output Voltage	0	40	V
I_{OUTx}	Continuous Output Current		1.5	A
	Peak Output Current	Internally Limited		
I_{CLAMP}	Clamp Current		4	A
I_{GND}	Ground Current		4	A
T_J	Maximum Junction Temperature		150	°C
T_A	Operating Temperature Range	−40	125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
ETSSOP24	30.2	18.5	°C/W

Electrical Characteristics

All test conditions: V_M = 12 V, V_{CLAMP} = 12 V, T_A = −40°C to +125°C, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Power Supply						
I_{VM}	VM Operating Supply Current	VM = 24 V		1	4	mA
V_{UVLO_rising}	VM Under-voltage-lock-out Rising Edge	VM rising edge			4.4	V
$V_{UVLO\_falling}$	VM Under-voltage-lock-out Falling Edge	VM falling edge			4.4	V
Logic Inputs / Outputs (nEN, nPWMx, LATCH, SDI, SCLK, RESET, DIAGEN, nFAULT, SDO)						
V_{IL}	Input Low Voltage	IN = L			0.7	V
V_{IH}	Input High Voltage	IN = H	1.5			V
I_{IL}	Input Low Current	V_{IN} = 0 V	-20		20	μA
I_{IH}	Input High Current	V_{IN} = 3.3 V			100	μA
R_{PD}	Input Pull-down Resistance		60	100	130	kΩ
V_{OL}	Output Low Voltage, SDO, nFAULT	I_O = 5 mA			0.5	V
$I_{OH(nFAULT)}$	nFAULT Output High Leakage Current	V_O = 3.3 V	-1		1	uA
V_{SDO_H}	Output High Voltage	I_O = 0.1 mA, VM = 5 V - 40 V, steady state	2.5		5.9	V
I_{SDO_SRC}	SDO Source Current	VM = 24V, V_{SDO} = V_{SDO_H} - 0.5V		10		mA
I_{SDO_SINK}	SDO Sink Current	VM = 24V, V_{SDO} = 0.3V		50	250	mA
Outputs						
$R_{ds(ON)}$	Output Low-side MOSFET on-resistance	VM = 24 V, I_O= 500 mA, T_J= 25°C		0.5		Ω
$R_{ds(ON)}$	Output Low-side MOSFET on-resistance	VM = 24 V, I_O= 500 mA, T_J= 150°C		0.8	1.2	Ω
V_F	Highside Diode Forward Voltage	VM = 24 V, I_{SINK}= 500 mA, T_J = 25°C		0.9		V
I_{HSD_lkg}	Highside Diode Leakage Current	VM = 24 V, T_J = 25°C	-50		50	μA
$t_{OUT\_risetime}$	Output Rise time	VM = 24 V, T_J = 25°C, Resistive load		80		ns
$t_{OUT\_falltime}$	Output Fall time	VM = 24 V, T_J = 25°C, Resistive load		90		ns
Diagnostics and Protection						
$I_{(OCP\_TH)}$	Over-current Protection Threshold		1.65		2.8	A

Parameter		Conditions	Min	Typ	Max	Unit
$t_{(OCP\_deg)}$	Over-current Protection Deglitch Time			3.5		μs
$V_{(OL\_TH)}$	Open Load Detection Threshold			1.2		V
$t_{(OL\_deg)}$	Open Load Detection Deglitch Time		7		17	μs
$I_{(OL\_off)}$	Off-time Open-Load Source Current			30	50	μA
t_{RETRY}	Over-current Retry Timer			100		ms
t_{TSD}	Thermal Shutdown Threshold		150	175		°C
t_{TSD_HYS}	Thermal Shutdown Threshold Hysteresis			15		°C

Table 2. Register Map

RegName	ADDR [3:0]	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	DEFAULT
READ0	0h	DOUT8	DOUT7	DOUT6	DOUT5	DOUT4	DOUT3	DOUT2	DOUT1	00h
READ1	1h	MASK_OCP8	MASK_OCP7	MASK_OCP6	MASK_OCP5	MASK_OCP4	MASK_OCP3	MASK_OCP2	MASK_OCP1	00h
READ2	2h	MASK_OPEN8	MASK_OPEN7	MASK_OPEN6	MASK_OPEN5	MASK_OPEN4	MASK_OPEN3	MASK_OPEN2	MASK_OPEN1	00h
READ3	3h	FORCE_FAULT	CONF_EXTOCP	CONF_PWMMAP	CONF_AUTORETRY	CONF_COMMCRC	RESERVED			00h
READ4	4h	FLAG_FAULT	FLAG_COMMCRC	FLAG_OPEN	FLAG_OCP	RESERVED	FLAG_TSD	FLAG_REGLOCK	FLAG_POR	81h
READ5	5h	FLAG_OPEN8	FLAG_OPEN7	FLAG_OPEN6	FLAG_OPEN5	FLAG_OPEN4	FLAG_OPEN3	FLAG_OPEN2	FLAG_OPEN1	X
READ6	6h	FLAG_OCP8	FLAG_OCP7	FLAG_OCP6	FLAG_OCP5	FLAG_OCP4	FLAG_OCP3	FLAG_OCP2	FLAG_OCP1	00h
READ7	7h	FLAG_PWM4	FLAG_PWM3	FLAG_PWM2	FLAG_PWM1	CALC_REGCRC				X

RegName	ADDR [3:0]	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	DEFAULT
WRITE0	8h	DOUT8	DOUT7	DOUT6	DOUT5	DOUT4	DOUT3	DOUT2	DOUT1	00h
WRITE1	9h	MASK_OCP8	MASK_OCP7	MASK_OCP6	MASK_OCP5	MASK_OCP4	MASK_OCP3	MASK_OCP2	MASK_OCP1	00h
WRITE2	Ah	MASK_OPEN8	MASK_OPEN7	MASK_OPEN6	MASK_OPEN5	MASK_OPEN4	MASK_OPEN3	MASK_OPEN2	MASK_OPEN1	00h
WRITE3	Bh	FORCE_FAULT	CONF_EXTOCP	CONF_PWMMAP	CONF_AUTORETRY	CONF_COMMCRC	RESERVED			00h
WRITE4	Ch	CLR_REG								00h
WRITE5	Dh	RESERVED								00h
WRITE6	Eh	REG_LOCK								00h
WRITE7	Fh	RESERVED	RESERVED	RESERVED	CLR_TSD	CLR_OCP	CLR_OPEN	CLR_FAULT	CLR_POR	00h

Typical Performance Characteristics

All test conditions: V_{IN} =12 V, T_A =+ 25°C, unless otherwise noted.

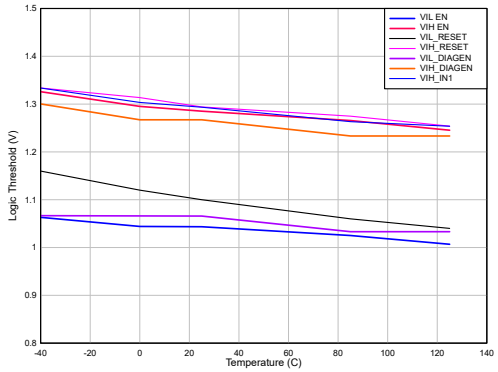


Figure 1. Logic Input Threshold vs. Temperature

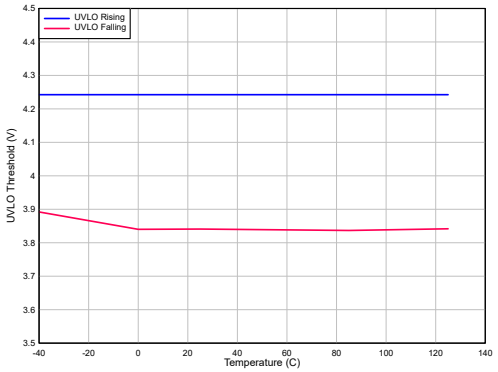


Figure 2. UVLO Threshold vs. Temperature

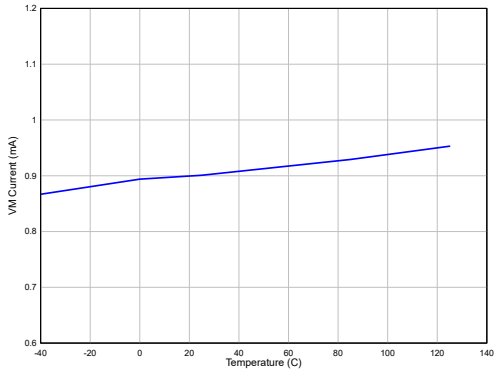


Figure 3. Quiescent Current vs. Temperature

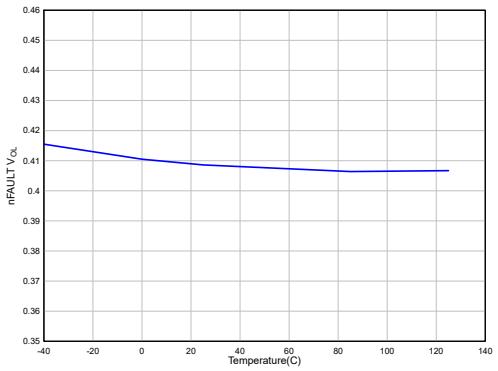


Figure 4. nFAULT V_{OL} vs. Temperature

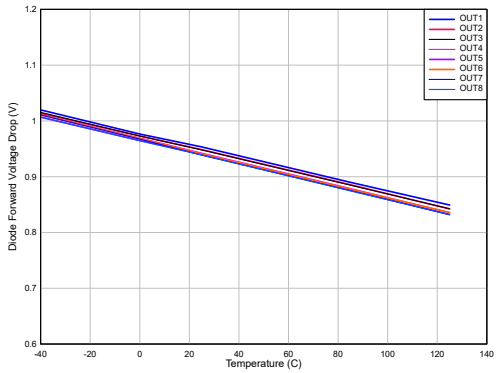


Figure 5. Forward Diode Drop vs. Temperature

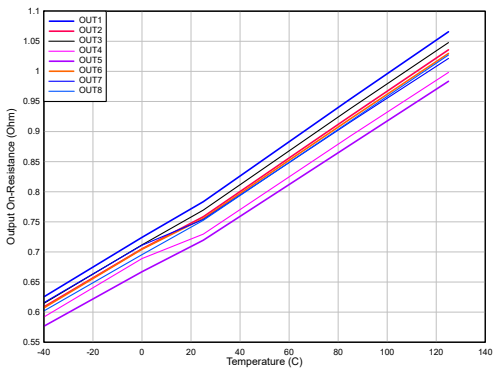


Figure 6. On-resistance vs. Temperature

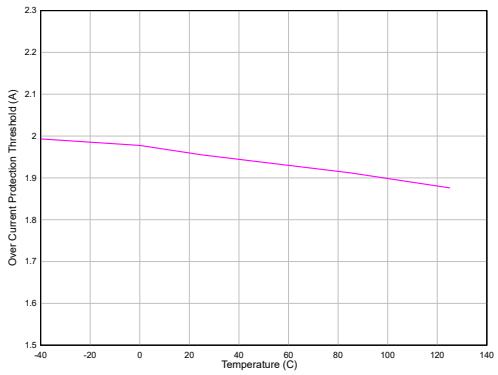


Figure 7. Over Current Protection Threshold vs. Temperature

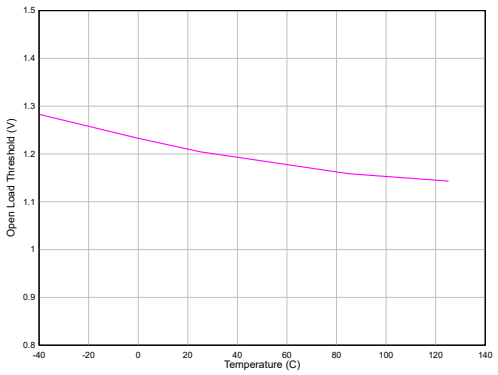


Figure 8. Open-Load Protection Threshold vs. Temperature

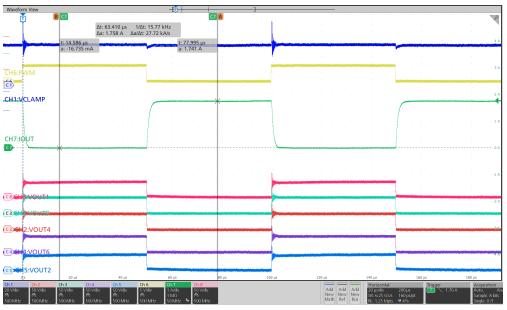


Figure 9. Inductive Load Driving

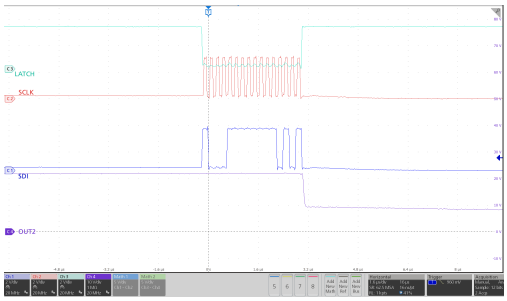


Figure 10. Serial Interface

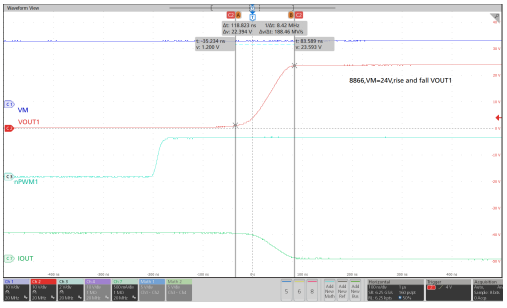


Figure 11. Output Rising Edge

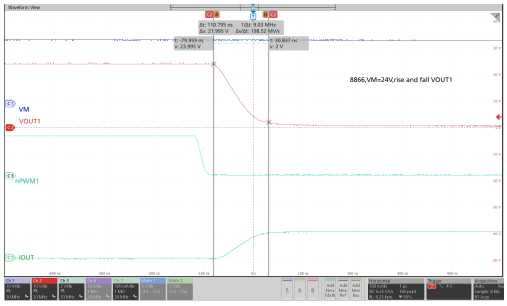


Figure 12. Output Falling Edge

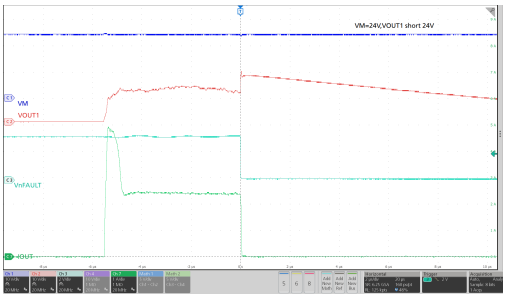


Figure 13. Short Circuit Protection

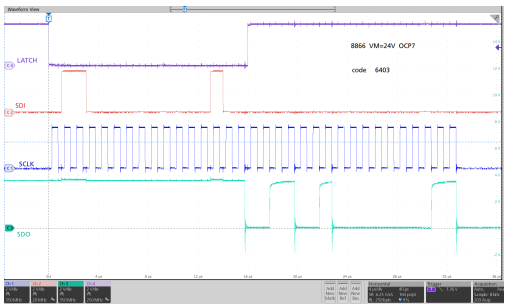


Figure 14. Output Fault Readback

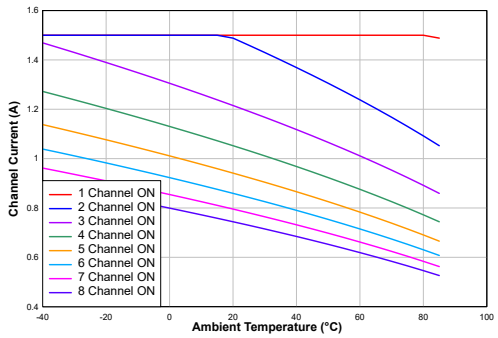


Figure 15. Output Current Capability

T_A = 25 °C

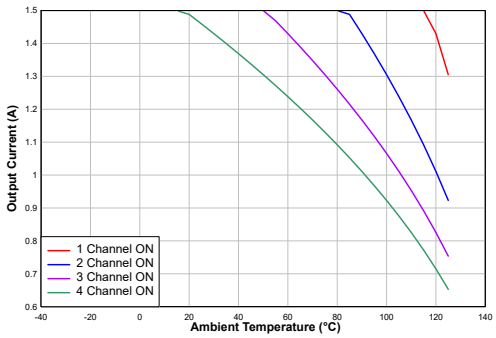


Figure 16. Output Current Capability - Parallel Mode

T_A = 25 °C, 2-channel in parallel

Detailed Description

Overview

The TPM8866 is a smart high-voltage high-current low-side driver array with full diagnostics and protection. The device supports maximum 40-V separated supply and driver voltage. 8-Ch low-side driver can be controlled individually via serial interface and direct PWM input. Each output channel has an integrated free-wheeling diode path for inductive loads such as solenoids, motors, electric expansion valves and relays. The device has protection features including supply under-voltage monitoring, over-current protection, load open-circuit and short-circuit diagnostics, and over-temperature protection. Its serial interface has CRC for both communication and register map to prevent unintended changes. Open-drain fault bus allows hardware interrupt for MCU to handle fault scenarios easily.

The device supports daisy-chain connection of multiple devices together as well as an isolated interface with 3PEAK digital isolators.

Functional Block Diagram

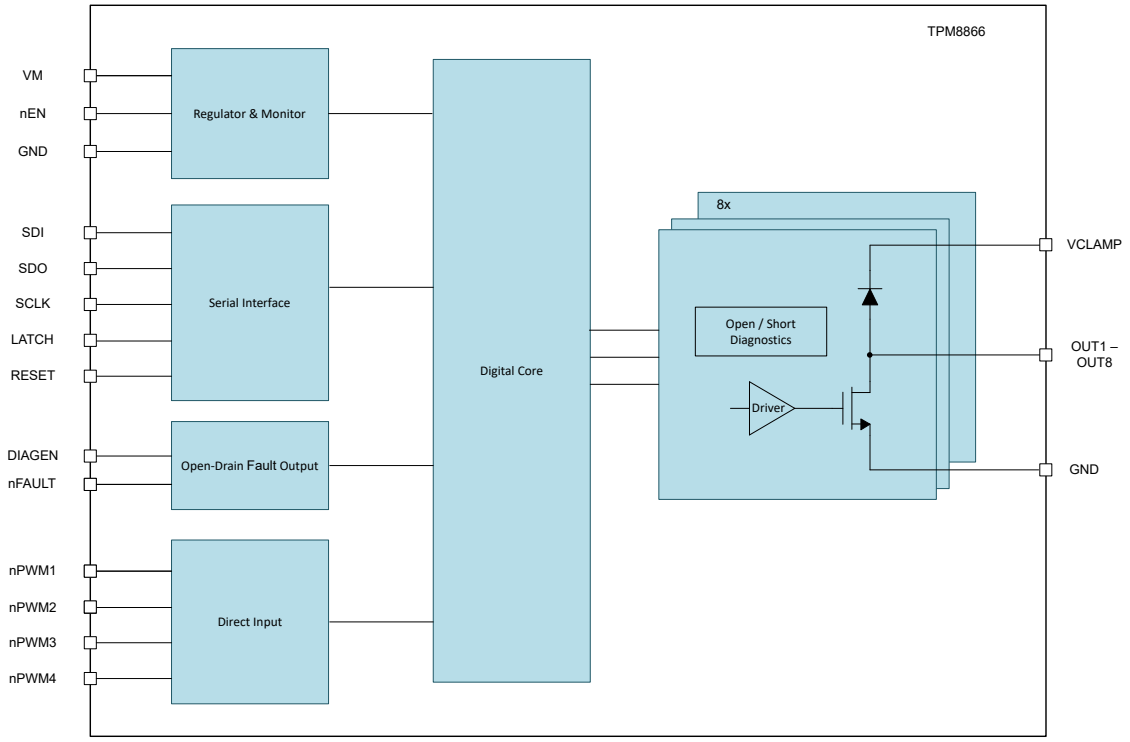


Figure 17. Functional Block Diagram

Feature Description

Supply and Reference

The TPM8866 supports two voltage rails: VM and VLCAMP. VM includes an undervoltage lockout (UVLO) monitor to prevent issues at low supply voltages. VCLAMP operates independently from VM and can range from 0 V to 40 V. The internal control circuit is powered by VM, while the driver is powered by VCLAMP. Separating these rails helps prevent reverse currents from inductive loads. However, VM and VCLAMP can also be connected if needed. It is recommended to use 10-μF capacitors on each rail to suppress voltage transients when driving inductive loads.

The device has a RESET input with an internal pull-down. When RESET is high, the device is in a reset state, clearing register maps and tri-stating the SDO pin. When RESET is low, the device is in normal operation and can communicate via the serial interface.

Upon power-up, the FLAG_POR bit is set to 1 to indicate a power-up without initialization.

Output Enable

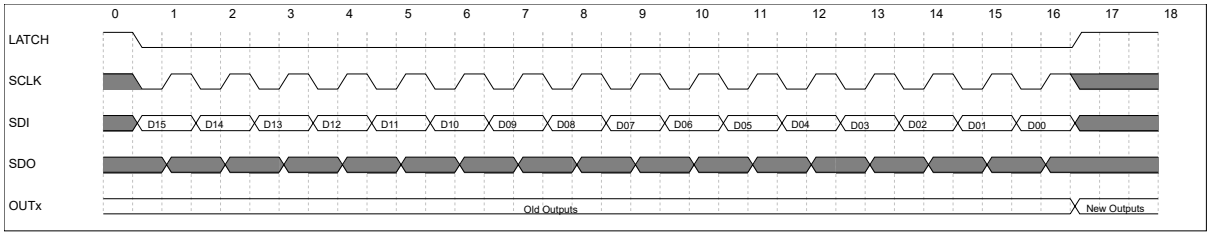
The TPM8866 provides an active low output enable, nEN, to control the device outputs. When nEN is high, the outputs are disabled, and when nEN is low, the outputs are enabled. It's important to note that nEN does not reset internal registers. It has an internal pull-down resistor and can be left unconnected or connected to the ground for desired functionality.

Serial Communication & CRC

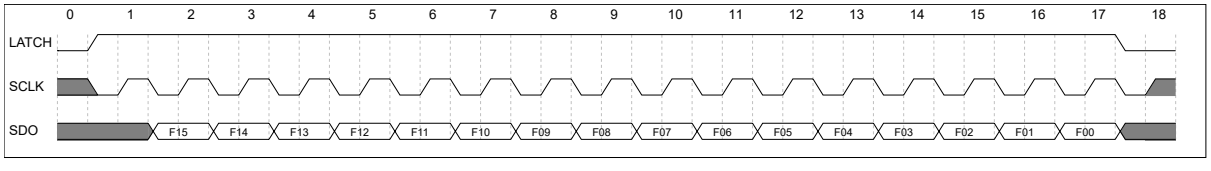
Serial Interface

The TPM8866 device supports a high-speed SPI-compatible serial interface with a Cyclic Redundancy Check (CRC) feature and daisy-chain capability. The Serial Data Output (SDO) pin is configured as a push-pull output, connected to the internal 3.3-V voltage rail to enable high-speed communication.

During a write operation, when the device selection LATCH is low, on each rising edge of the serial clock (SCLK), the device shifts the Serial Data Input (SDI) into the internal shift register and updates the Serial Data Output (SDO) with the last bit of the shift register. Upon the rising edge of LATCH, the shift registered data is analyzed, and if the CONF_COMMCRC is set to 1, the Cyclic Redundancy Check (CRC) is performed to verify the data integrity. The CONF_COMMCRC is reset to 0 upon power-up or device reset to ignore CRC errors.



During a read operation, the microcontroller should first issue a write command with the address, and then send out the serial clock when the device selection is high. On each falling edge of SCLK, the device shifts out the data from the internal register to SDO.



Each serial interface frame consists of 16 bits, with a 4-bit address, an 8-bit data segment, and a 4-bit CRC, transmitted with the Most Significant Bit (MSB) first.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ADDR[3:0]				DATA[7:0]								CRC[3:0]			

Register Lock

The TPM8866 device includes a register lock mechanism to prevent accidental modifications to the register map. By default, upon power-up, the register lock is disabled. To modify the register values, the registers need to be unlocked by writing a specific value to the REG_LOCK (Eh) register.

To disable the write protection and unlock the registers, the value 0x95 should be written to the REG_LOCK register. Conversely, to enable write protection and lock the registers, the value 0x31 should be written to the REG_LOCK register.

The FLAG_REGLOCK is a status indicator that reflects the state of the register lock. When the register lock is enabled, the FLAG_REGLOCK is set to 1, indicating that modifications to the register map are not allowed. Conversely, when the register lock is disabled, the FLAG_REGLOCK is 0, indicating that the register map can be modified.

This mechanism provides control over register modifications and helps prevent unintended changes to the configuration of the device.

Clear Register

To clear the register map of the TPM8866 device and restore it to its initial state, the user can write a specific value to the CLR_REG register (Ch). By writing the value 0xA6 to the CLR_REG register, the register map will be reset, removing any previous configurations and returning all registers to their default values.

Once the register map is cleared, the FLAG_POR (Power-On Reset) bit will not reset to 1.

Clearing the register map can be useful in scenarios where a fresh start or a known initial state is required for proper device operation.

Communication CRC

The TPM8866 device includes a CRC (Cyclic Redundancy Check) error detection mechanism for communication integrity. The behavior of CRC error detection depends on the value of the CONF_COMMCRC register.

If CONF_COMMCRC is set to 0, the device will not examine the CRC result of the shift registers during communication. In this case, CRC errors will not be detected or reported. The register values will be interpreted regardless of the CRC result.

However, if CONF_COMMCRC is set to 1, the device will examine the CRC result of the shift registers upon each rising edge of the latch signal. If a CRC failure occurs, indicating a communication error, the register values will be considered invalid and will not be interpreted. It's important to note that communication CRC faults will not be reported through the nFAULT open-drain output.

To indicate the detection of a communication CRC error, the FLAG_COMMCRC bit will be set to 1. The user can use the CLR_CRCERR command to clear CRC errors and reset the FLAG_COMMCRC bit.

By enabling communication CRC error detection, users can ensure the integrity of the data being transmitted and received, helping to identify and handle potential communication errors.

Register Map CRC

The TPM8866 device features a 4-bit REGCRC[3:0] input that facilitates the calculation of CRC (Cyclic Redundancy Check) values for specific registers. The WRITE0 (8h), WRITE1 (9h), WRITE2 (Ah), WRITE3 (Bh), and WRITE7 (Fh) registers are computed using a 4-bit CRC algorithm, and the resulting CRC value is stored in the CALC_REGCRC register.

To ensure data integrity and avoid unintended changes to the registers, the user can read back the value stored in the CALC_REGCRC register and verify its content with the MCU (Microcontroller Unit). This verification process allows for content validation without the need to read back and check the entire set of registers individually.

By using the CRC calculation and verification mechanism, users can efficiently validate the correctness of register data, reducing the efforts required for data validity checks and ensuring the integrity of the device's configuration.

Cyclic Redundancy Check Algorithm

The TPM8866 device employs a 4-bit CRC (Cyclic Redundancy Check) algorithm with a polynomial of 10011. This polynomial represents the mathematical calculations performed by the CRC algorithm to generate a checksum for data verification.

The 4-bit CRC algorithm takes the data being checked and performs bitwise calculations using the polynomial 10011. These calculations generate a 4-bit CRC value, which is used for data integrity verification.

By utilizing the 4-bit CRC check algorithm with the polynomial 10011, the TPM8866 device ensures reliable and accurate data validation, helping to detect and prevent errors during data transmission and storage.

$x^4 + x + 1$

Here's the corrected CRC process explanation using the example of a random 40-bit data and the polynomial 10011:

Example: Random 40-bit Data (in hexadecimal): 0x7B35D81A9C

1. Start with the data sequence: 0x7B35D81A9C.
2. Append four zero bits to the end of the data sequence, resulting in an 11-digit hexadecimal sequence: 0x7B35D81A9C0.
3. Initialize the CRC register to all zeros: CRC = 0x0.
4. Iterate through each bit of the 44-bit data sequence from the MSB to the LSB:
   For each bit:
   - If the current bit is 1, perform the XOR operation between the polynomial (0x13) and the current value of the CRC register. Shift the CRC register one bit to the left.
   - If the current bit is 0, proceed to the next bit without any XOR operation.
5. After iterating through all 44 bits, the resulting value in the CRC register is 0x7.

Output Driver

The device features an array of 8 low-side drivers, each consisting of a low-side MOSFET and a high-side recirculation diode. Each channel is capable of handling a maximum current of 1.5 A, although the total device current should also consider thermal effects. The drivers can accommodate both inductive and resistive loads.

When a channel is turned on, the low-side MOSFET conducts, allowing current to flow from the external load through the low-side MOSFET to the device ground. When the channel is turned off, the inductive current will continue to flow, but it will be recirculated through the internal diode to the VCLAMP pin.

It is crucial to ensure that the VCLAMP pin can handle the inductive energy. To protect against overvoltage, we recommend using an external clamp diode connected to the VCLAMP pin. The other side of the external clamp diode can be connected to either the VM or GND, depending on the specific application requirements.

Output Control by Register

Each channel of the device can be individually enabled or disabled. This can be achieved through both the serial interface using the DOUTx signal and the parallel I/O using the PWM1x to PWM4x signals. When DOUTx is set to 1, the corresponding channel is turned on, and when it is set to 0, the channel is turned off.

In addition to individual channel control through the DOUTx register, the device also supports a 4-channel PWM (Pulse Width Modulation) feature with mapping selection. This allows for more advanced control of the output channels. The specific configuration and mapping of the PWM channels can be determined through the registers of the device.

PWM Input and Mapping

To provide direct PWM control for applications like motor control or LED dimming, the device offers 4 active-low PWM inputs. The mapping of the PWM inputs to the output channels can be configured based on the value of the CONF_PWMMAP register.

When CONF_PWMMAP is set to 0, only OUT1 to OUT4 are mapped to the corresponding nPWM1 to nPWM4 signals. The channels OUT5 to OUT8 are solely controlled by the DOUT5 to DOUT8 signals.

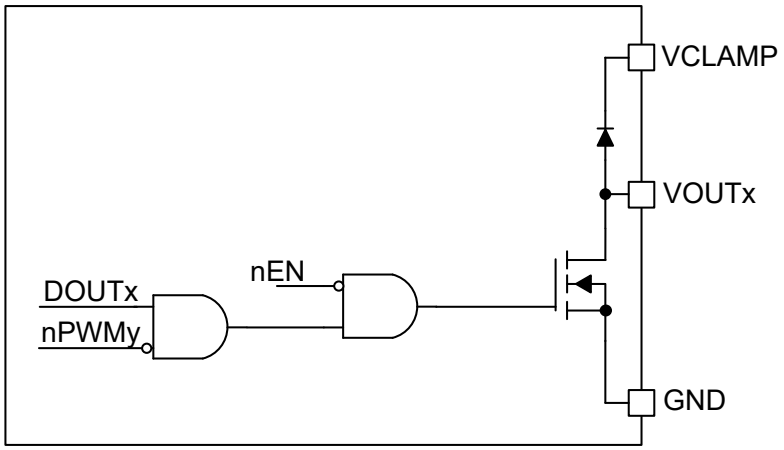
In cases where a higher current is required, the TPM8866 supports parallel driving.

By setting CONF_PWMMAP to 1:

- The nPWM1 signal controls both OUT1 and OUT2
- The nPWM2 signal controls both OUT3 and OUT4.
- The nPWM3 signal controls both OUT5 and OUT6.
- The nPWM4 signal controls both OUT7 and OUT8.

This parallel configuration allows for increased current handling capability while maintaining synchronized control of the corresponding output channels.

The state of the nPWMy signals can be read from the corresponding FLAG_PWMy bits. These bits provide information about the current state of the PWM inputs. By checking the value of the FLAG_PWMy bits, the user can determine whether the corresponding nPWMy signal is active or inactive. This allows for monitoring and synchronization of the PWM control signals with the device's operation.



Output Diagnostics

Open-drain Fault

The TPM8866 features an open-drain output called nFAULT. This output is used to indicate the occurrence of a fault. When a fault condition occurs, the nFAULT pin is pulled down, signaling the fault status to the external circuitry. The microcontroller can also force the nFAULT pin low by setting the FORCE_FAULT bit to 1. This allows the microcontroller to actively monitor the fault feedback loop by simulating a fault condition and observing the corresponding response through the nFAULT pin.

Open Diagnostics

During the off time of each channel, the TPM8866 can to detect open loads. This is done by applying a small current of 30 μA to the OUTx pin and comparing the voltage at OUTx with an internal threshold called Vth_open. If the output is open (no load connected), the small current will pull down the voltage at OUTx to ground, triggering the open comparator.

It's important to note that an open load condition will not prevent the channel from turning on. The open load flag, FLAG_OPENx, can be cleared by using either the MASK_OPENx bit, CLR_FAULT command, or CLR_OPEN command.

Each channel has an independent open fault mask bit, MASK_OPENx. When MASK_OPENx is set to 1, the channel will ignore open load detection and disable the pull-down current. This effectively clears the open fault.

If any of the channels trigger an open load fault, both the FLAG_OPEN and FLAG_FAULT will be set, and the nFAULT pin will be pulled low, indicating the occurrence of a fault.

In applications where a leakage current of 30 μA is not acceptable, such as LED drivers, the open-load diagnostics can be disabled by setting the MASK_OPENx bit. By setting MASK_OPENx to 1, the channel will ignore open-load detection and disable the 30-μA pull-down current. This allows for the elimination of the leakage current in situations where it is not desirable.

Short & Over Current Protection Diagnostics

Each channel of the device is equipped with a short-circuit protection circuit to limit the output current and shut down the channel if an overcurrent fault is detected. If an output channel is shorted to the supply, the output current will be internally clamped to protect the channel.

During the on-time of the channel, it continuously monitors the output current. If the current exceeds a predefined threshold for a duration longer than the deglitch timer, an overcurrent fault is triggered. This triggers the FLAG_OCPx and the channel is turned off to prevent further damage.

By default, the overcurrent protection is set to latch off, meaning the FLAG_OCPx remains set until it is manually cleared using CLR_FAULT, CLR_OCP, or by setting MASK_OCPx.

To support applications with large capacitive loads, the device offers an extended OCP deglitch timer mode by setting CONF_EXTOCP to 1, increasing the deglitch timer from 3.5 μs to 10 μs. This helps to prevent false OCP triggers when dealing with high-output current demands.

Each channel has an independent fault mask bit, MASK_OCPx. When this bit is set to 1, the channel will ignore overcurrent protection, allowing it to remain on even if an overcurrent event occurs. However, if the current exceeds the short-circuit protection threshold, the current will be clamped at the short-circuit protection level.

In the event of an OCP fault on any channel, the FLAG_OCP and FLAG_FAULT will be set, and the nFAULT pin will be pulled low to indicate the fault condition.

By default, the overcurrent protection is latched off, meaning it remains active until manually cleared. To clear the overcurrent fault, the user can use commands like CLR_FAULT, CLR_OCP, or set the MASK_OCPx bit.

To enhance system reliability, the TPM8866 offers an auto-retry feature. When CONF_AUTORECOVERY is set to 1, a channel that experiences an overcurrent fault will automatically retry after a 100-ms delay. During the retry time, the overcurrent flags (FLAG_OCPx and FLAG_FAULT) remain set. The retry timer is synchronized between channels, eliminating the need for separate timers for each channel.

Each channel has an independent overcurrent protection fault mask bit, MASK_OCPx. If MASK_OCPx is set to 1, the channel will mask the overcurrent protection, allowing the channel to remain on even if an overcurrent condition occurs. If the current exceeds the short protection threshold, the current will be clamped at the short protection threshold.

The extended OCP deglitch timer, enabled by setting CONF_EXTOCP to 1, is specifically designed to support capacitive loads in situations where an overcurrent protection (OCP) event may occur. Capacitive loads can cause a momentary surge in current when initially connected, which might trigger the OCP fault detection mechanism.

By increasing the deglitch timer from the standard duration of 3.5 μs to 10 μs in the extended mode, the device allows for a longer duration to evaluate the current waveform before considering it as an overcurrent condition. This extended timer helps prevent false triggering of the OCP fault due to capacitive loads and allows the device to operate effectively with such loads.

In the event of an OCP fault in any of the channels, the FLAG_OCP and FLAG_FAULT will be set, and the nFAULT pin will be pulled low to indicate the fault condition.

Thermal Protection

The TPM8866 device includes thermal protection to prevent damage from excessive temperatures. When the junction temperature surpasses a certain threshold, the thermal shutdown (FLAG_TSD) feature is triggered, turning off all output channels. Once the temperature drops below the threshold, normal operation resumes. The FLAG_TSD can be cleared using

commands like CLR_FAULT or CLR_TSD. Thermal protection ensures safe operation by monitoring and reacting to high temperatures.

Offset	RegName	Width	Bit	FieldName	R/W	Reset Value	Description
00h	READ0	8	0	DOUT1	R	0	Output channel control. 0: output off, 1: output on
			1	DOUT2	R	0	Output channel control. 0: output off, 1: output on
			2	DOUT3	R	0	Output channel control. 0: output off, 1: output on
			3	DOUT4	R	0	Output channel control. 0: output off, 1: output on
			4	DOUT5	R	0	Output channel control. 0: output off, 1: output on
			5	DOUT6	R	0	Output channel control. 0: output off, 1: output on
			6	DOUT7	R	0	Output channel control. 0: output off, 1: output on
			7	DOUT8	R	0	Output channel control. 0: output off, 1: output on
01h	READ1	8	0	MASK_OCP1	R	0	Channel over current fault mask control. 0: over current detection enabled. 1: over current detection disabled
			1	MASK_OCP2	R	0	Channel over current fault mask control. 0: over current detection enabled. 1: over current detection disabled
			2	MASK_OCP3	R	0	Channel over current fault mask control. 0: over current detection enabled. 1: over current detection disabled
			3	MASK_OCP4	R	0	Channel over current fault mask control. 0: over current detection enabled. 1: over current detection disabled
			4	MASK_OCP5	R	0	Channel over current fault mask control. 0: over current detection enabled. 1: over current detection disabled
			5	MASK_OCP6	R	0	Channel over current fault mask control. 0: over current detection enabled. 1: over current detection disabled
			6	MASK_OCP7	R	0	Channel over current fault mask control. 0: over current detection enabled. 1: over current detection disabled
			7	MASK_OCP8	R	0	Channel over current fault mask control. 0: over current detection enabled. 1: over current detection disabled
02h	READ2	8	0	MASK_OPEN1	R	0	Channel open fault mask control. 0: open detection enabled. 1: open detection disabled
			1	MASK_OPEN2	R	0	Channel open fault mask control. 0: open detection enabled. 1: open detection disabled
			2	MASK_OPEN3	R	0	Channel open fault mask control. 0: open detection enabled. 1: open detection disabled

Offset	RegName	Width	Bit	FieldName	R/W	Reset Value	Description
			3	MASK_OPEN4	R	0	Channel open fault mask control. 0: open detection enabled. 1: open detection disabled
			4	MASK_OPEN5	R	0	Channel open fault mask control. 0: open detection enabled. 1: open detection disabled
			5	MASK_OPEN6	R	0	Channel open fault mask control. 0: open detection enabled. 1: open detection disabled
			6	MASK_OPEN7	R	0	Channel open fault mask control. 0: open detection enabled. 1: open detection disabled
			7	MASK_OPEN8	R	0	Channel open fault mask control. 0: open detection enabled. 1: open detection disabled
03h	READ3	8	[2:0]	RESERVED	R	0	Reserved
			3	CONF_COMM CRC	R	0	Configure communication CRC check. 0: Communication CRC ignore. 1: Report communication error and discard communication frame when CRC check fails.
			4	CONF_AUTOR ETRY	R	0	Configure over current protection auto recovery. 0: latched. 1: auto retry after 100ms
			5	CONF_PWMM AP	R	0	Configure PWM mapping input. 0: PWM1-4 map to OUT1-4, 1: PWM1-4 map to OUT 1-8
			6	CONF_EXTOC P	R	0	Configure OCP deglitch timer 0: 3.5us. 1:10us.
			7	FORCE_FAUL T	R	0	Force fault control. 0: normal nFault. 1: nFault pulled low
04h	READ4	8	0	FLAG_POR	R	1	Power-on-reset flag. 0: POR cleared. 1: POR flag is set.
			1	FLAG_REGLO CK	R	0	Register map write lock flag. 0: register map can be modified. 1: register map can not be modified.
			2	FLAG_TSD	R	0	Thermal shutdown protection flag. 0: TSD cleared. 1: TSD flag is set
			3	RESERVED	R	0	Reserved
			4	FLAG_OCP	R	0	Output over current protection flag. 0: No OCP. 1: At least 1 channel has OCP
			5	FLAG_OPEN	R	0	Output open-circuit detection flag. 0: No open-circuit fault 1: At least 1 channel has open-circuit fault.
			6	FLAG_COMM CRC	R	0	Communication CRC fault flag. 0: Communication CRC matches. 1: Communication CRC had mismatch.
			7	FLAG_FAULT	R	1	Fault flag. 0: No fault has been triggered. At least one fault has been triggered.
05h	READ5	8	0	FLAG_OPEN1	R	X	Channel open fault flag. 0: No open fault.

Offset	RegName	Width	Bit	FieldName	R/W	Reset Value	Description
							1: Open fault has been triggered.
			1	FLAG_OPEN2	R	X	Channel open fault flag. 0: No open fault. 1: Open fault has been triggered.
			2	FLAG_OPEN3	R	X	Channel open fault flag. 0: No open fault. 1: Open fault has been triggered.
			3	FLAG_OPEN4	R	X	Channel open fault flag. 0: No open fault. 1: Open fault has been triggered.
			4	FLAG_OPEN5	R	X	Channel open fault flag. 0: No open fault. 1: Open fault has been triggered.
			5	FLAG_OPEN6	R	X	Channel open fault flag. 0: No open fault. 1: Open fault has been triggered.
			6	FLAG_OPEN7	R	X	Channel open fault flag. 0: No open fault. 1: Open fault has been triggered.
			7	FLAG_OPEN8	R	X	Channel open fault flag. 0: No open fault. 1: Open fault has been triggered.
06h	READ6	8	0	FLAG_OCP1	R	0	Channel over current fault flag. 0: No over current fault. 1: Short fault has been triggered.
			1	FLAG_OCP2	R	0	Channel over current fault flag. 0: No over current fault. 1: Short fault has been triggered.
			2	FLAG_OCP3	R	0	Channel over current fault flag. 0: No over current fault. 1: Short fault has been triggered.
			3	FLAG_OCP4	R	0	Channel over current fault flag. 0: No over current fault. 1: Short fault has been triggered.
			4	FLAG_OCP5	R	0	Channel over current fault flag. 0: No over current fault. 1: Short fault has been triggered.
			5	FLAG_OCP6	R	0	Channel over current fault flag. 0: No over current fault. 1: Short fault has been triggered.
			6	FLAG_OCP7	R	0	Channel over current fault flag. 0: No over current fault. 1: Short fault has been triggered.
			7	FLAG_OCP8	R	0	Channel over current fault flag. 0: No over current fault. 1: Short fault has been triggered.
07h	READ7	8	3:0	CALC_REGCRC	R	X	Calculated register map CRC.
			4	FLAG_PWM1	R	X	PWM input status flag. 0: Input PWM = L. 1: Input PWM = H
			5	FLAG_PWM2	R	X	PWM input status flag. 0: Input PWM = L. 1: Input PWM = H
			6	FLAG_PWM3	R	X	PWM input status flag. 0: Input PWM = L. 1: Input PWM = H
			7	FLAG_PWM4	R	X	PWM input status flag. 0: Input PWM = L. 1: Input PWM = H

Offset	RegName	Width	Bit	FieldName	R/W	Reset Value	Description
08h	WRITE0	8	0	DOUT1	W	0	Output channel control. 0: output off, 1: output on
			1	DOUT2	W	0	Output channel control. 0: output off, 1: output on
			2	DOUT3	W	0	Output channel control. 0: output off, 1: output on
			3	DOUT4	W	0	Output channel control. 0: output off, 1: output on
			4	DOUT5	W	0	Output channel control. 0: output off, 1: output on
			5	DOUT6	W	0	Output channel control. 0: output off, 1: output on
			6	DOUT7	W	0	Output channel control. 0: output off, 1: output on
			7	DOUT8	W	0	Output channel control. 0: output off, 1: output on
09h	WRITE1	8	0	MASK_OCP1	W	0	Channel over current fault mask control. 0: over current detection enabled. 1: over current detection disabled
			1	MASK_OCP2	W	0	Channel over current fault mask control. 0: over current detection enabled. 1: over current detection disabled
			2	MASK_OCP3	W	0	Channel over current fault mask control. 0: over current detection enabled. 1: over current detection disabled
			3	MASK_OCP4	W	0	Channel over current fault mask control. 0: over current detection enabled. 1: over current detection disabled
			4	MASK_OCP5	W	0	Channel over current fault mask control. 0: over current detection enabled. 1: over current detection disabled
			5	MASK_OCP6	W	0	Channel over current fault mask control. 0: over current detection enabled. 1: over current detection disabled
			6	MASK_OCP7	W	0	Channel over current fault mask control. 0: over current detection enabled. 1: over current detection disabled
			7	MASK_OCP8	W	0	Channel over current fault mask control. 0: over current detection enabled. 1: over current detection disabled
0Ah	WRITE2	8	0	MASK_OPEN1	W	0	Channel open fault mask control. 0: open detection enabled. 1: open detection disabled
			1	MASK_OPEN2	W	0	Channel open fault mask control. 0: open detection enabled. 1: open detection disabled
			2	MASK_OPEN3	W	0	Channel open fault mask control. 0: open detection enabled. 1: open detection disabled
			3	MASK_OPEN4	W	0	Channel open fault mask control. 0: open detection enabled. 1: open detection disabled

Offset	RegName	Width	Bit	FieldName	R/W	Reset Value	Description
			4	MASK_OPEN5	W	0	Channel open fault mask control. 0: open detection enabled. 1: open detection disabled
			5	MASK_OPEN6	W	0	Channel open fault mask control. 0: open detection enabled. 1: open detection disabled
			6	MASK_OPEN7	W	0	Channel open fault mask control. 0: open detection enabled. 1: open detection disabled
			7	MASK_OPEN8	W	0	Channel open fault mask control. 0: open detection enabled. 1: open detection disabled
0Bh	WRITE3	8	[2:0]	RESERVED	W	0	Reserved
			3	CONF_COMM CRC	W	0	Configure communication CRC check. 0: Communication CRC ignore. 1: Report communication error and discard communication frame when CRC check fails.
			4	CONF_AUTOR ETRY	W	0	Configure over current protection auto retry. 0: latched. 1: auto retry after 100ms
			5	CONF_PWMM AP	W	0	Configure PWM mapping input. 0: PWM1-4 map to OUT1-4, 1: PWM1-4 map to OUT 1-8
			6	CONF_EXTOC P	W	0	Configure OCP deglitch timer 0: 3.5us. 1:10us.
			7	FORCE_FAUL T	W	0	Force fault control. Auto return to zero and latched fault. The fault will be cleared by CLR_FAULT.
0Ch	WRITE4	8	[7:0]	CLR_REG	W	0	Register map clear command. Write 0xA6 to reset all registers.
0Dh	WRITE5	8	0	RESERVED	W	0	Reserved
0Eh	WRITE6	8	[7:0]	REG_LOCK	W	0	Register map lock protection. Write 0X31 to write protect. Write 0X95 to disable write protect.
0Fh	WRITE7	8	0	CLR_POR	W	0	Power-on-reset flag clear. Set to 1 to clear POR flag. Auto return to 0 after cleared.
			1	CLR_FAULT	W	0	All fault flag clear. Set to 1 to clear all fault flags. Auto return to 0 after cleared.
			2	CLR_OPEN	W	0	Output open fault flag clear. Set to 1 to clear open fault flag. Auto return to 0 after cleared.
			3	CLR_OCP	W	0	Output over current fault flag clear. Set to 1 to clear over current fault flag. Auto return to 0 after cleared.
			4	CLR_TSD	W	0	Thermal shutdown fault clear. Set to 1 to clear TSD flag. Auto return to 0 after cleared.
			5	RESERVED	W	0	Reserved
			6	RESERVED	W	0	Reserved

Offset	RegName	Width	Bit	FieldName	R/W	Reset Value	Description
			7	RESERVED	W	0	Reserved

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

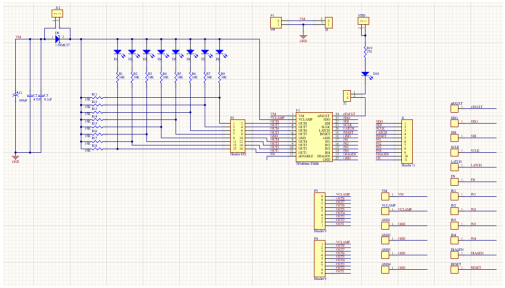
Application Information

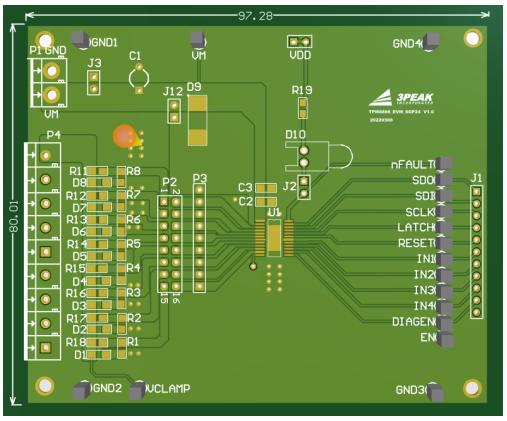
PLC Digital Output

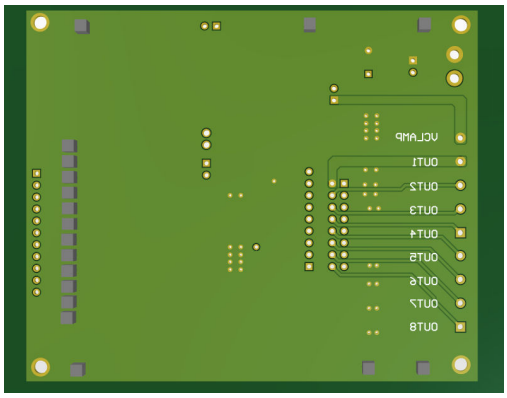
Serial Communication

The TPM8866 is designed for digital output control in industrial PLC (Programmable Logic Controller) applications. It features an SPI communication interface and integration with digital isolators to provide reliable output control.

In industrial PLC applications, digital outputs are commonly used to control various external devices such as motors, valves, lights, etc. The TPM8866 offers an 8-channel low-side driver array, with each channel capable of independent switching control. Through the SPI interface, the main controller can send commands to TPM8866 to control the on/off state of each channel.







Commonly used serial commands are as follows:

- OUT1 open - Register: 08, Hex Code: 8012, Binary Code: 1000,0000,0001,0010
  This command opens channel OUT1.
- OUT1-8 open - Register: 08, Hex Code: 8FF5, Binary Code: 1000,1111,1111,0101
  This command opens channels OUT1 to OUT8 simultaneously.
- OUT1-8 close - Register: 08, Hex Code: 8001, Binary Code: 1000,0000,0000,0001

This command closes channels OUT1 to OUT8 simultaneously.

- Read DOUT - Register: 00, Hex Code: 0000, Binary Code: 0000,0000,0000,0000
  This command reads the status of the DOUT register.
- Read Open fault register - Register: 05, Hex Code: 5006, Binary Code: 0101,0000,0000,0110
  This command reads the open fault register to check for any open circuit faults.
- Read OCP fault register - Register: 06, Hex Code: 6004, Binary Code: 0110,0000,0000,0100
  This command reads the over-current protection (OCP) fault register to check for any over-current faults.
- Wmask OCP fault - Register: 09, Hex Code: 9FFA, Binary Code: 1001,1111,1111,1010
  This command writes a mask to the OCP fault register to enable/disable OCP fault detection for specific channels.
- Rmask OCP fault - Register: 01, Hex Code: 100F, Binary Code: 0001,0000,0000,1111
  This command reads the OCP fault mask register to check the OCP fault detection mask for each channel.
- Wmask Open fault - Register: 0A, Hex Code: AFF8, Binary Code: 1010,1111,1111,1000
  This command writes a mask to the open fault register to enable/disable open circuit fault detection for specific channels.
- Rmask Open fault - Register: 02, Hex Code: 200D, Binary Code: 0010,0000,0000,1101
  This command reads the open fault mask register to check the open circuit fault detection mask for each channel.
- CONF OCP Autoretry - Register: 0B, Hex Code: B106, Binary Code: 1011,0001,0000,0110
  This command configures the automatic retry feature for over-current protection (OCP). Setting the bit enables auto retry after 100ms.
- CONF PWMMAP - Register: 0B, Hex Code: B209, Binary Code: 1011,0010,0000,1001
  This command configures the PWM mapping selection for the channels. The specific channel-to-PWM mapping is determined by the bits in this register.
- Read CONF - Register: 03, Hex Code: 3002, Binary Code: 0011,0000,0000,0010
  This command reads the CONF register to check the configuration settings.
- Read fault flag - Register: 04, Hex Code: 4009, Binary Code: 0100,0000,0000,1001
  This command reads the fault flag register to check for any fault flags.
- CLR register - Register: 0C, Hex Code CA66，Binary Code：1100,1010,0110,0110
  This command clears the register map of the TPM8866 device and restore it to its initial state.

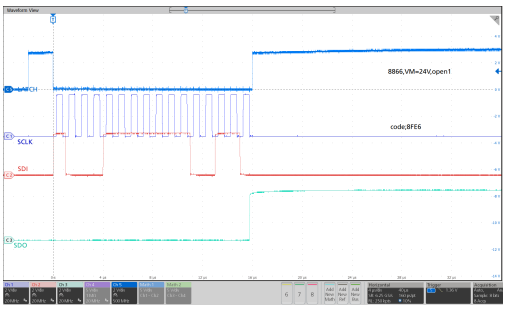


Figure 18. Serial Communication Write

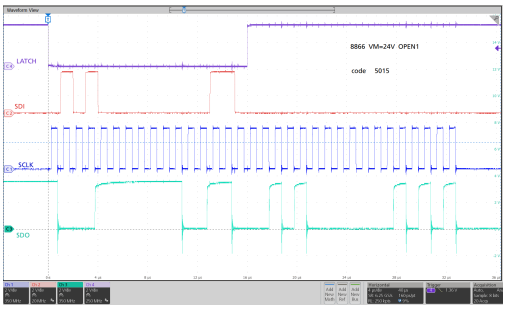


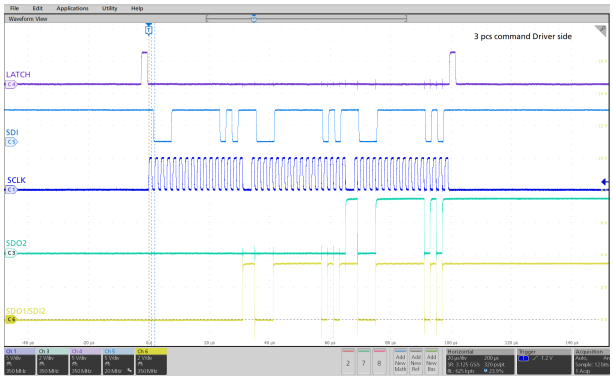
Figure 19. Serial Communication Read

Multiple Devices in Daisy Chain with Digital Isolator

To ensure reliability and safety, digital isolators are incorporated into the system. These isolators provide signal isolation between the main controller and the TPM8866, protecting the signal transmission from noise, electromagnetic interference, and other detrimental factors. This isolation design enhances system stability and reliability, while safeguarding the main controller from external disturbances.

By combining SPI communication with digital isolators, the TPM8866 delivers a robust solution for digital output control in industrial PLC applications. It enables precise output control and shields the main controller from external interference. Whether in factory automation, machinery control, or other industrial domains, the TPM8866 provides reliable digital output control capabilities for industrial PLCs.

The figure below shows an example of 3pcs of devices in daisy-chain communication:



Typical Application

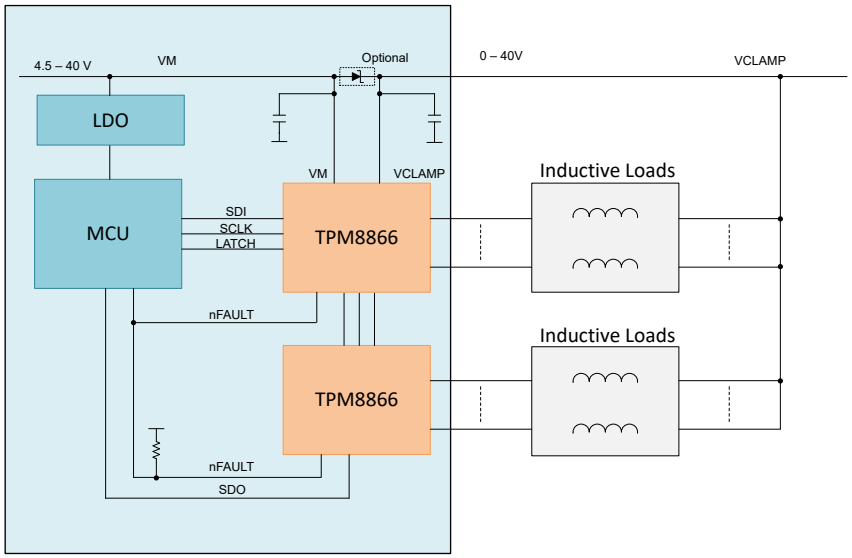


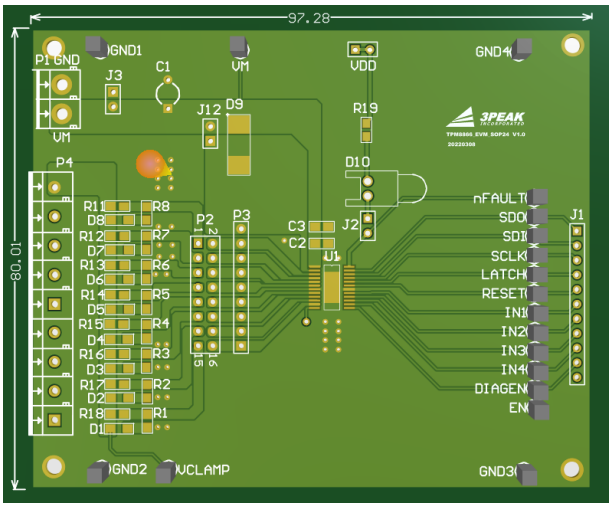
Figure 20. Typical Application Circuit

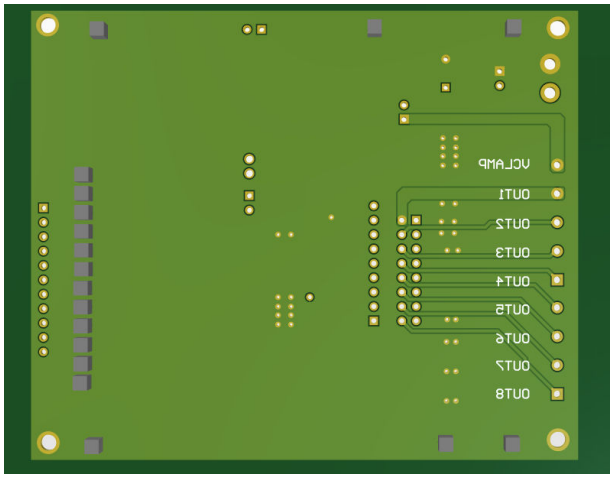
Layout

Layout Guideline

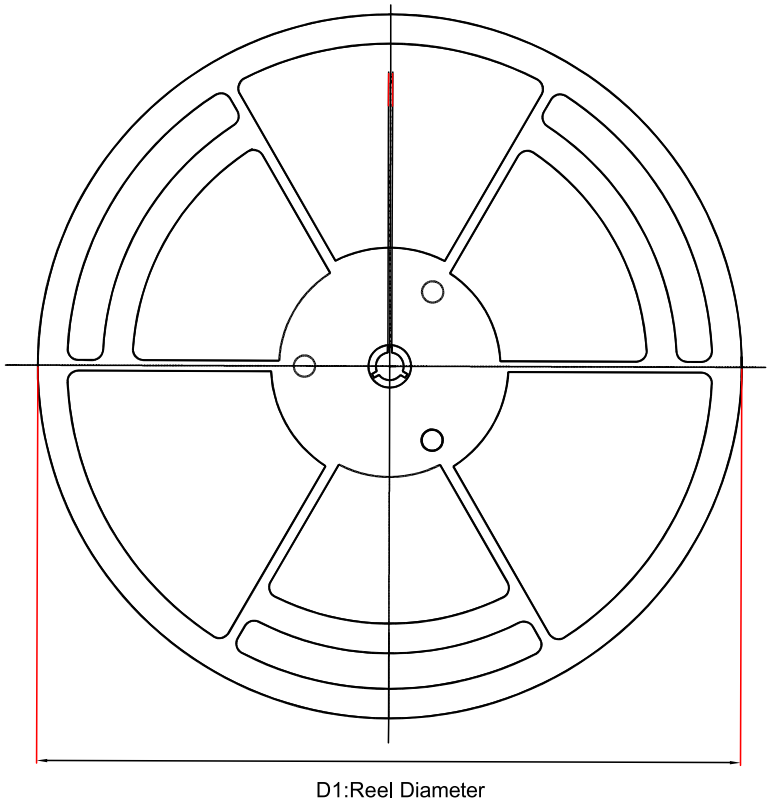
- Both input capacitors and output capacitors must be placed to the device pins as close as possible.
- It is recommended to bypass the input pin to ground with a 0.1-μF bypass capacitor.
- It is recommended to use wide and thick copper to minimize I×R drop and heat dissipation.
- Exposed pad must be connected to the PCB ground plane directly, the copper area must be as large as possible.

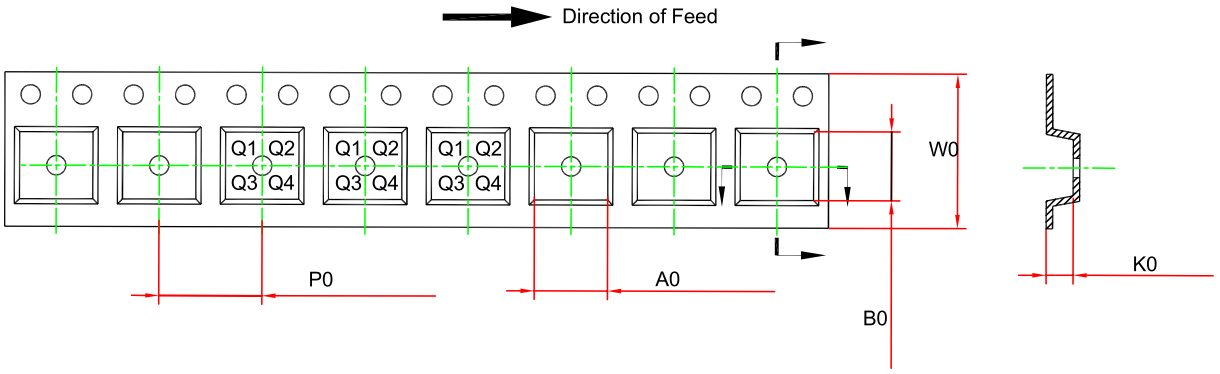
Layout Example





Tape and Reel Information



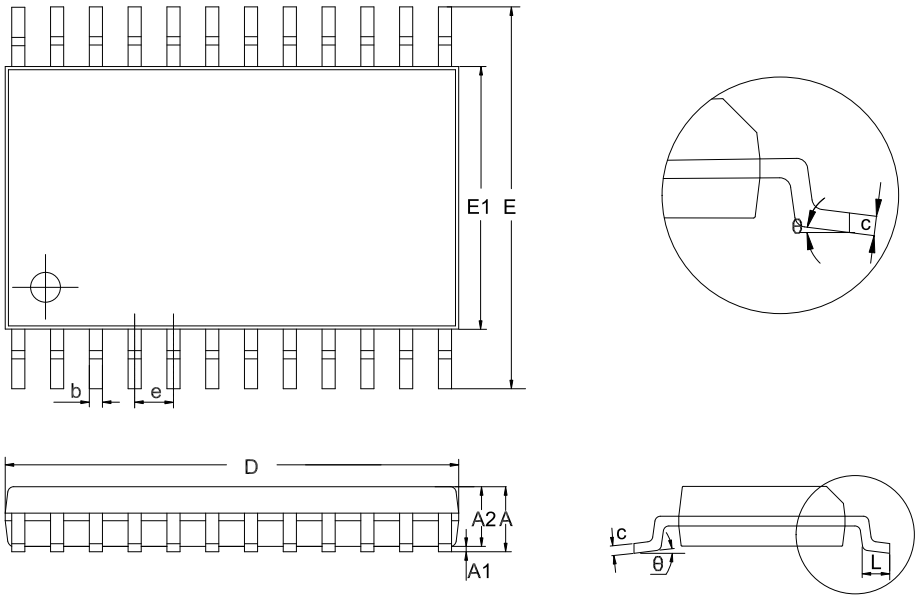


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPM8866-TSDR	ETSSOP2 4	330	21.6	6.9	8.3	1.6	8.0	16.0	Q1
TPM8866-TS5R	TSSOP24	330	21.6	6.8	8.3	1.6	8.0	16.0	Q1

Package Outline Dimensions

TSSOP24

Package Outline Dimensions TS5(TSSOP-24-A)



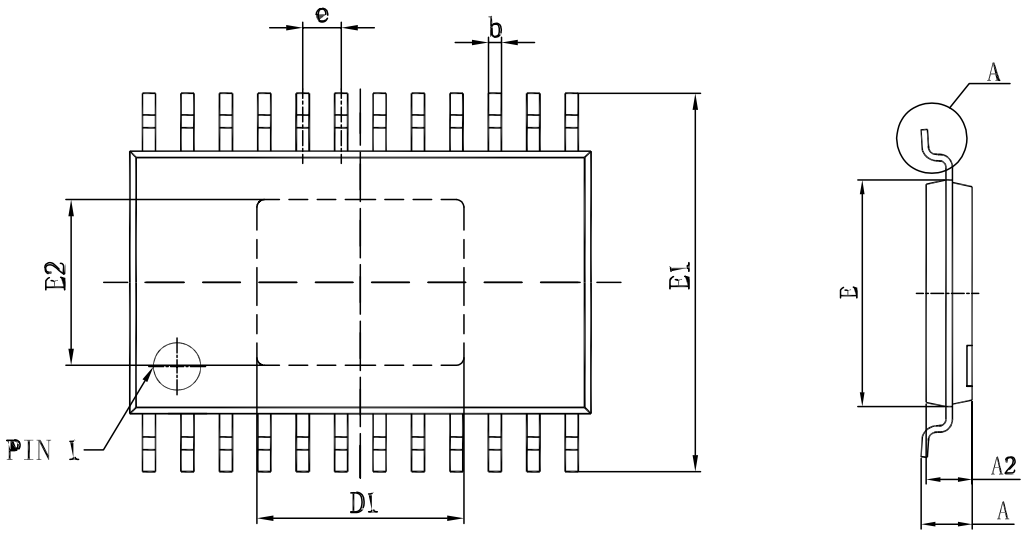
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.200	0.035	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	7.700	7.900	0.303	0.311
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
θ	0	8°	0	8°

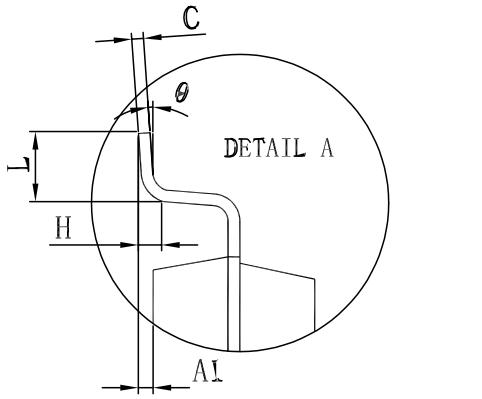
NOTES

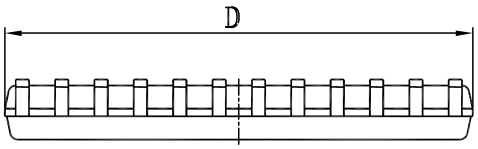
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

ETSSOP-24

Package Outline Dimensions TSD(ETSSOP-24-C)







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	---	1.100	---	0.043
A1	0.020	0.150	0.001	0.006
A2	0.800	1.000	0.031	0.039
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	7.700	7.900	0.303	0.311
E	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
D1	3.400	3.600	0.134	0.138
E2	2.700	2.900	0.106	0.122
e	0.650 BSC		0.026 BSC	
L	0.500	0.700	0.020	0.028
θ	1°	7°	1°	7°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPM8866-TSDR	−40 to 125°C	ETSSOP24	M8866	3	Tape and Reel, 4000	Green
TPM8866-TS6R (1)	−40 to 125°C	TSSOP24	M8866	3	Tape and Reel, 4000	Green

(1) For future products, contact the 3PEAK factory for more information and samples.

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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