8-Channel I²C Switch with Reset

Features

- Bidirectional Translator of 1:8 I²C Switch
- Active-Low Reset Input
- Three Address Terminals, Allowing up to 8 Devices on the I²C Bus
- Operating Power-Supply Voltage Range: 2.3 V ~ 5.5 V
- Allows Voltage-Level Translation between 2.5 V, 3.3 V, and 5 V Buses
- Support Standard Mode and Fast Mode I²C Devices，0 to 400-kHz Clock Frequency
- Low RON Switches
- Latch-Up Performance Exceeds 200 mA per JESD 78
- ESD Protection Exceeds JESD 22
  - 3.5 kV Human-Body Model
  - 1.5 kV Charged-Device Model
- AEC-Q100 Qualified

Applications

- Servers/Storages
- Routers (Telecom Switching Equipment)
- Factory Automation
- Products With I²C Slave Address Conflicts (e.g., Multiple, Identical Temp Sensors)

Description

The TPT29548T is a 1:8 bidirectional translating I²C switch, and Q100 qualified. The SCL/SDA upstream pair fans out to eight downstream channels. Any single SCn/SDn channel or combination of channels can be selected, determined by the programmable control register.

If one of the downstream I²C buses is stuck in a low state, then an active-low reset ($\overline{\text{RESET}}$) input helps the TPT29548T to recover. Pulling $\overline{\text{RESET}}$ low resets the I²C state machine and causes all the channels to be deselected, as does the internal power-on reset function.

The pass gates of the switches are constructed such that the VCC terminal can be used to limit the maximum high voltage, which will be passed by the TPT29548T. This allows the use of different bus voltages on each pair, so that 2.5-V, or 3.3-V parts can communicate with 5-V parts, without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O terminals are 5.5 V tolerant.

TPT29548T is available in the QFN24L package and is characterized from −40°C to +125°C.

Functional Block Diagram

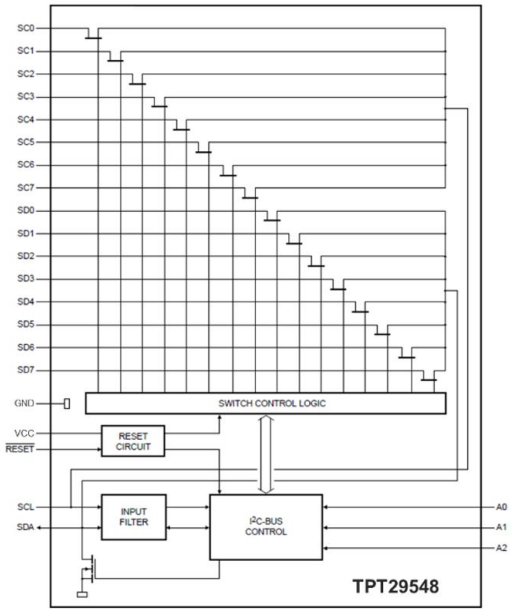


Table of Contents

Revision History

Date	Revision	Notes
2024-04-15	Rev. A0	Released Version

Pin Configuration and Functions

TPT29548T
QFN4X4-24 Package
Top View

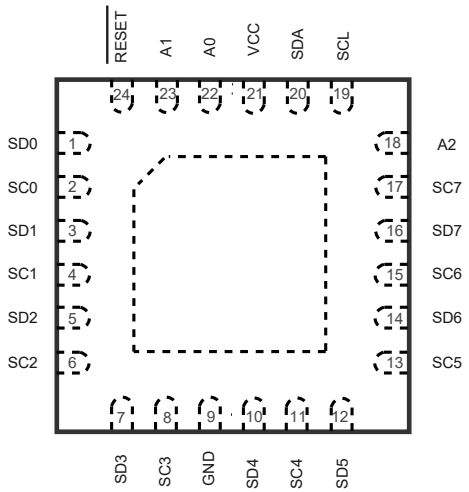


Table 1. Pin Functions: TPT29548T

Pin	Name	I/O	Description
22	A0	Input	Address input 0. Connect directly to VCC or ground
23	A1	Input	Address input 1. Connect directly to VCC or ground
24	$\overline{\text{RESET}}$	Input	Reset input, active LOW. Connect to VCC or pull up the power of the master side through a pull-up resistor, if not used
1	SD0	I/O	Data 0. Connect to the power of slave channel 0 through a pull-up resistor
2	SC0	I/O	Clock 0. Connect to the power of slave channel 0 through a pull-up resistor
3	SD1	I/O	Data 1. Connect to the power of slave channel 1 through a pull-up resistor
4	SC1	I/O	Clock 1. Connect to the power of slave channel 1 through a pull-up resistor
5	SD2	I/O	Data 2. Connect to the power of slave channel 2 through a pull-up resistor
6	SC2	I/O	Clock 2. Connect to the power of slave channel 2 through a pull-up resistor
7	SD3	I/O	Data 3. Connect to the power of slave channel 3 through a pull-up resistor
8	SC3	I/O	Clock 3. Connect to the power of slave channel 3 through a pull-up resistor
9	GND	GND	Ground
10	SD4	I/O	Data 4. Connect to the power of slave channel 4 through a pull-up resistor
11	SC4	I/O	Clock 4. Connect to the power of slave channel 4 through a pull-up resistor
12	SD5	I/O	Data 5. Connect to the power of slave channel 5 through a pull-up resistor
13	SC5	I/O	Clock 5. Connect to the power of slave channel 5 through a pull-up resistor
14	SD6	I/O	Data 6. Connect to the power of slave channel 6 through a pull-up resistor
15	SC6	I/O	Clock 6. Connect to the power of slave channel 6 through a pull-up resistor

Pin	Name	I/O	Description
16	SD7	I/O	Data 7. Connect to the power of slave channel 7 through a pull-up resistor
17	SC7	I/O	Clock 7. Connect to the power of slave channel 7 through a pull-up resistor
18	A2	Input	Address input 2. Connect directly to VCC or ground
19	SCL	Input	Clock bus. Connect to VCC through a pull-up resistor
20	SDA	Input	Data bus. Connect to VCC through a pull-up resistor
21	VCC	Supply	Supply voltage

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
V_{CC}	Supply Voltage	−0.5	7	V
V_I	Input Voltage	−0.5	7	V
I_{IK}	Input Clamp Current, V_I< 0		±20	mA
I_{OK}	Output Clamp Current, V_O< 0		±25	mA
I_{CC}	Maximum Junction Temperature		±100	mA
T_J	Operating Temperature Range		125	°C
T_A	Operating Temperature Range	−45	125	°C
T_{stg}	Storage Temperature	−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) This data was taken with the JEDEC low effective thermal conductivity test board.
(3) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Value	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	3.5	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter			Min	Max	Unit
V_{CC}	Supply Voltage		2.3	5.5	V
V_{IH}	High-Level Input Voltage	SCL, SDA	0.7 × V_{CC}	5.5	V
		A2 ~ A0, $\overline{RESET}$	0.7 × V_{CC}	5.5	V
V_{IL}	Low-Level Input Voltage	SCL, SDA	−0.5	0.3 × V_{CC}	V
		A2 ~ A0, $\overline{RESET}$	−0.5	0.3 × V_{CC}	V

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
QFN24	65	28	°C/W

Electrical Characteristics - DC Parameters

All test conditions: V_{CC} = 2.3 V ~ 3.6 V, T_A = −40°C ~ +125°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
I_{DD}	Supply Current in Operating Mode	V_{CC} = 2.3~3.6 V; no load; V_I = V_{CC} or GND; f_{SCL} = 100 kHz		10	20	μA
		V_{CC} = 2.3~3.6 V; no load; V_I = V_{CC} or GND; f_{SCL} = 400 kHz		20	30	μA
Istb	Standby Current	V_{CC} = 2.3~3.6 V; no load; V_I = V_{CC} or GND		1.8	3	μA
V_{POR}	Power-on Reset Voltage， V_{CC} Rising	no load; V_I = V_{CC} or GND		1.25	1.45	V
	Power-on Reset Voltage， V_{CC} Falling		0.8	1.2		V
Input SCL; Input/Output SDA						
V_{IL}	Low-level Input Voltage	V_{CC} = 2.3~3.6 V			0.3V_{CC}	V
V_{IH}	High-level Input Voltage	V_{CC} = 2.3~3.6 V	0.7V_{CC}			V
I_{OL}	Low-level Output Current, SDA	V_{CC} = 2.3~3.6 V, V_{OL} = 0.4 V	3			mA
	Low-level Output Current, SDA	V_{CC} = 2.3~3.6 V, V_{OL} = 0.6 V	6			mA
I_L	Leakage Current	V_I = V_{CC} or GND	−1	0.1	1	μA
C_i	Input Capacitance (1)	V_I = GND		15		pF
Select Inputs A0 to A2, RESET						
V_{IL}	Low-level Input Voltage	V_{CC} = 2.3~3.6 V			0.3V_{CC}	V
V_{IH}	High-level Input Voltage	V_{CC} = 2.3~3.6 V	0.7V_{CC}			V
I_{LI}	Input Leakage Current	pin at V_{CC} or GND	−1	0.1	1	μA
C_i	Input Capacitance (1)	V_I = GND		3		pF
Pass Gate						
R_{on}	ON-state Resistance	V_{CC} = 2.3 V to 2.7 V; V_O = 0.4 V; I_O = 10 mA	7	30	45	Ω
		V_{CC} = 3.0 V to 3.6 V; V_O = 0.4 V; I_O = 15 mA	5	20	35	Ω
Vo(sw)	Switch Output Voltage (1)	Vi(sw) = V_{CC} = 2.5 V; Io(sw) = −100 μA		1.6		V
		Vi(sw) = V_{CC} = 2.3 V to 2.7 V; Io(sw) = −100 μA	1.1		2.0	V
		Vi(sw) = V_{CC} = 3.0 V; Io(sw) = −100 μA		2.0		V
		Vi(sw) = V_{CC} = 3.0 V to 3.6 V; Io(sw) = −100 μA	1.6		2.8	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_L	Leakage Current	V_I = VCC or GND	−1	0.1	1	μA
C_{io}	Input/Output Capacitance (1)	V_I = GND		3		pF

(1) Parameters are provided by lab bench tests and design simulation. Not tested in production.

Electrical Characteristics - DC Parameters (continuned)

All test conditions: V_{CC} = 4.5 V ~ 5.5 V, T_A = −40°C ~ +125°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
I_{DD}	Supply Current in Operating Mode	V_{CC} = 5.5 V; no load; V_I = V_{CC} or GND; f_{SCL} = 100 kHz		5	35	μA
		V_{CC} = 5.5 V; no load; V_I = V_{CC} or GND; f_{SCL} = 400 kHz		14	45	μA
Istb	Standby Current	V_{CC} = 5.5 V; no load; V_I = V_{CC} or GND		1.8	3	μA
V_{POR}	Power-on Reset Voltage， V_{CC} Rising	no load; V_I = V_{CC} or GND		1.25	1.45	V
	Power-on Reset Voltage， V_{CC} Falling		0.8	1.2		V
Input SCL; Input/Output SDA						
V_{IL}	Low-level Input Voltage	V_{CC} = 5.5 V			0.3V_{CC}	V
V_{IH}	High-level Input Voltage	V_{CC} = 5.5 V	0.7V_{CC}			V
I_{OL}	Low-level Output Current, SDA	V_{CC} = 5.5 V, V_{OL} = 0.4 V	3			mA
	Low-level Output Current, SDA	V_{CC} = 5.5 V, V_{OL} = 0.6 V	6			mA
I_L	Leakage Current	V_I = V_{CC} or GND	−1	0.1	1	μA
C_i	Input Capacitance (1)	V_I = GND(1)		15		pF
Select Inputs A0 to A2, RESET						
V_{IL}	Low-level Input Voltage	V_{CC} = 5.5 V			0.3V_{CC}	V
V_{IH}	High-level Input Voltage	V_{CC} = 5.5 V	0.7V_{CC}			V
I_{LI}	Input Leakage Current	pin at V_{CC} or GND	−1	0.1	1	μA
C_i	Input Capacitance (1)	V_I = GND(1)		3		pF
Pass Gate						
R_{on}	ON-state Resistance	V_{CC} = 4.5 V to 5.5 V; V_O = 0.4 V; I_O = 15 mA	4	7	20	Ω
Vo(sw)	Switch Output Voltage (1)	Vi(sw) = V_{CC} = 5.0 V; Io(sw) = −100 μA		3.55		V
		Vi(sw) = V_{CC} = 4.5 V to 5.5 V; Io(sw) = −100 μA	2.6		4.5	V
I_L	Leakage Current	V_I = VCC or GND	−1	0.1	1	μA
C_{io}	Input/Output Capacitance (1)	V_I = GND		3		pF

(1) Parameters are provided by lab bench tests and design simulation. Not tested in production.

I²C Interface Timing Requirements (1)

Over recommended operating free-air temperature range, unless otherwise noted.

Symbol	Description	Condition	I²C Normal mode		I²C BUS-Fast mode		Unit
			Min	Max	Min	Max	
f_{scl}	I²C clock frequency		0	100	0	400	kHz
t_{sch}	I²C clock high time		4		0.6		μs
t_{scl}	I²C clock low time		4.7		1.3		μs
t_{sp}	I²C spike time			50		50	ns
t_{sds}	I²C serial-data setup time		250		100		ns
t_{sdh}	I²C serial data hold time		0		0		ns
t_{icr}	I²C input rise time			1000	20	300	ns
t_{icf}	I²C input fall time(1)			300	20 + 0.1Cb	300	ns
t_{ocf}	I²C output fall time(1)	10-pF to 400-pF bus		300	20 + 0.1Cb	300	ns
t_{buf}	I²C bus free time between stop and start		4.7		1.3		μs
t_{sts}	I²C start or repeated start condition setup		4.7		0.6		μs
t_{sth}	I²C start or repeated start condition hold		4		0.6		μs
t_{sps}	I²C stop condition setup		4		0.6		μs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid		3.5		0.9	μs
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		3.5		0.9	μs
t_{PD}	Propagation delay(2)	from SDA to SDx, or SCL to SCx		0.3		0.3	ns
C_b	I²C bus capacitive load(1)			400		400	pF

(1) Cb is the total capacitance of one bus line in pF.
(2) The propagation delay is calculated from the 20 typical Ron and the 15-pF load capacitance.
(3) The parameter refers I²C standard, NOT tested in the production.

Switching Characteristics

Over recommended operating free-air temperature range, C_L ≦ 100 pF, unless otherwise noted.

Symbol	Description	Condition	Min	Max	Unit
$t_{w(rst)L}$	Low-level reset time		4		ns
t_{rst}	Reset time	SDA clear		500	ns
$t_{REC;STA}$	Recovery time to START condition		0		ns

Parameter Measurement Waveforms

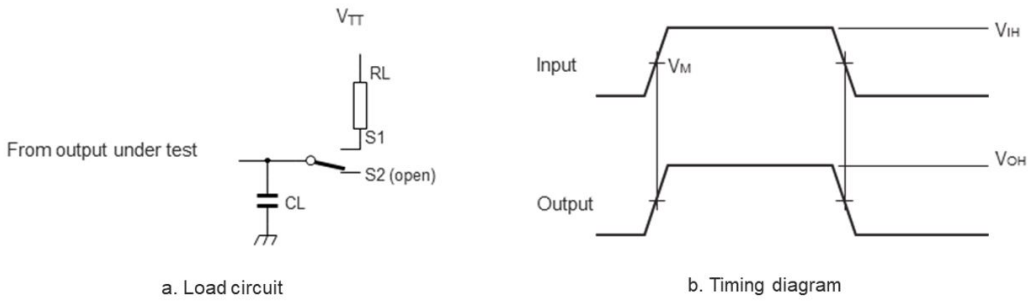


Figure 1. Load Circuit for Outputs

Detailed Description

Overview

The TPT29548T is a 1:8 bidirectional translating I²C switch, and Q100 qualified. The SCL/SDA upstream pair fans out to eight downstream channels. Any single SCn/SDn channel or combination of channels can be selected, determined by the programmable control register.

If one of the downstream I²C buses is stuck in a low state, then an active-low reset ($\overline{\text{RESET}}$) input helps the TPT29548T to recover. Pulling $\overline{\text{RESET}}$ low resets the I²C state machine and causes all the channels to be deselected, as does the internal power-on reset function.

The pass gates of the switches are constructed such that the VCC terminal can be used to limit the maximum high voltage, which will be passed by the TPT29548T. This allows the use of different bus voltages on each pair, so that 2.5-V, or 3.3-V parts can communicate with 5-V parts, without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O terminals are 5.5-V tolerant.

TPT29548T removed the reserved register 0X0C, and QFN4X4-24 pin1 is in the Q2 quadrant.

Functional Block Diagram

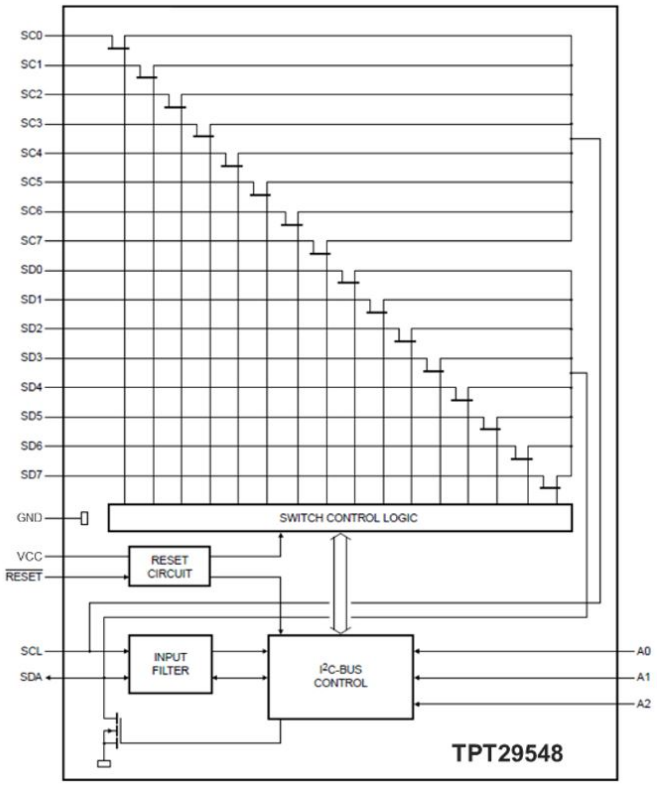


Figure 2. Functional Block Diagram

Feature Description

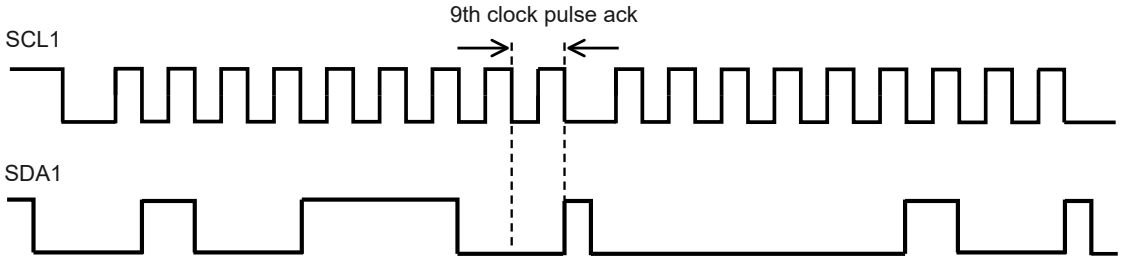


Figure 3. I²C BUS (2.3 V ~ 5.5 V) Waveform

Device Address

Following a START condition, the bus master must output the address of the slave it is accessing. To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW. The address of the TPT29548T is shown below.

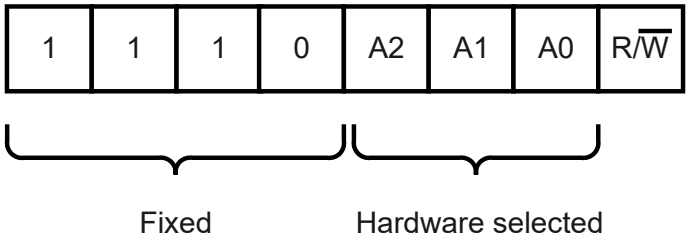


Figure 4. Slave Device Address

Control Register

Following the successful acknowledgment of the slave address, the bus master will send a byte to the TPT29548T, which will be stored in the control register. If multiple bytes are received by the TPT29548T, it will save the last byte received. This register can be written and read via the I²C bus.

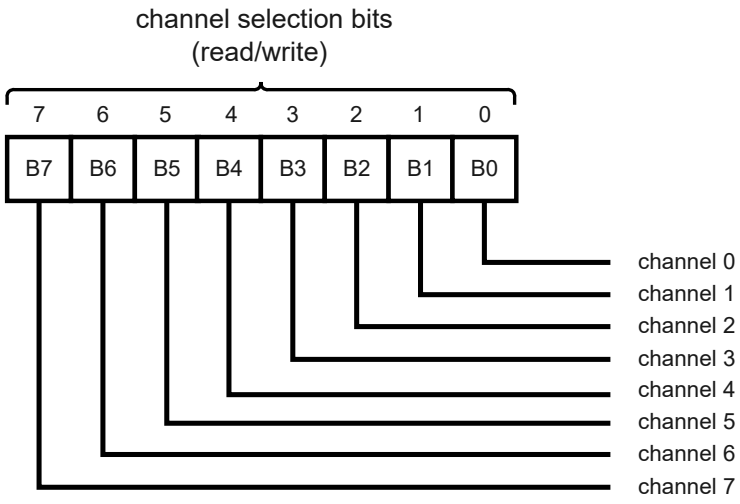


Figure 5. Control Register

Control Register Definition

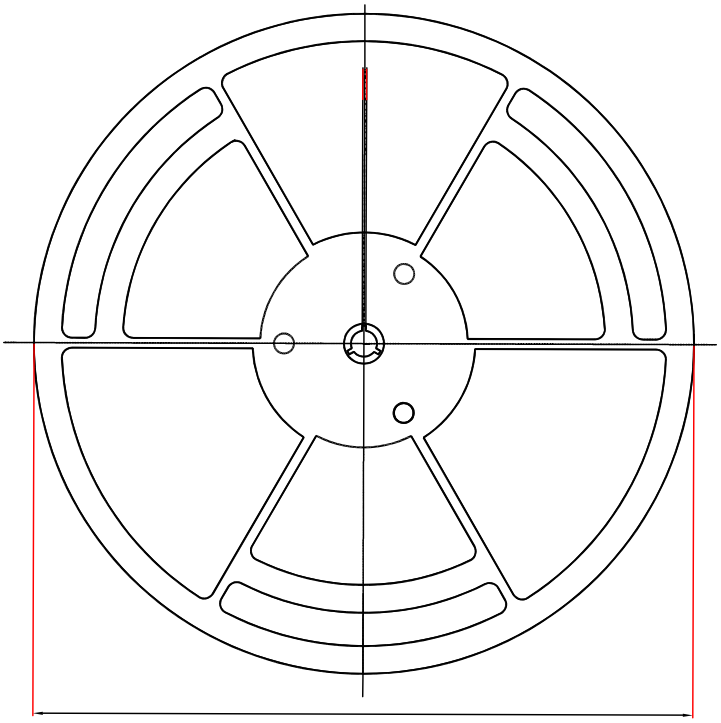
One or several SCx/SDx downstream pairs, or channels, are selected by the contents of the control register. This register is written after the TPT29548T has been addressed. The 2 LSBs of the control byte are used to determine which channel is to be selected. When a channel is selected, the channel will become active after a STOP condition has been placed on the I²C bus. This ensures that all SCx/SDx lines will be in a HIGH state when the channel is made active so that no false conditions are generated at the time of connection.

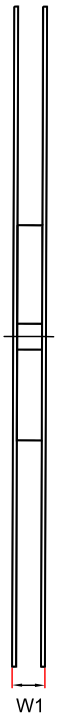
Table 2. Control Register: Write-Channel Selection; Read-Channel Status

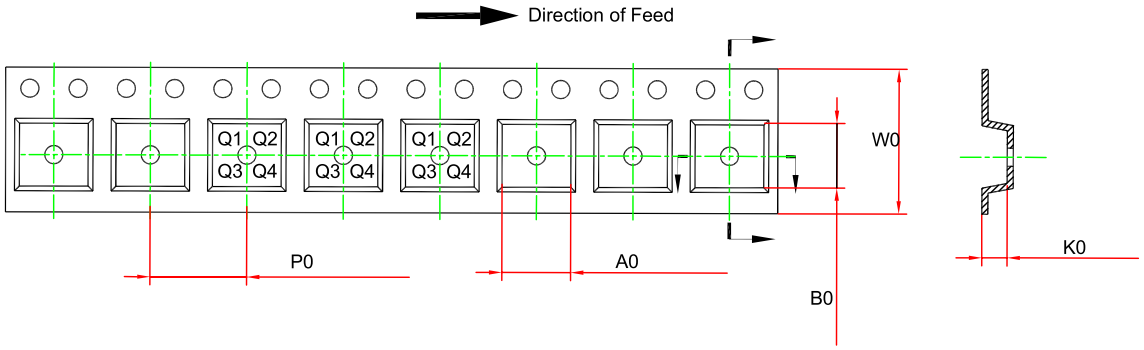
B7	B6	B5	B4	B3	B2	B1	B0	Command
x	x	x	x	x	x	x	0	Channel 0 disable
x	x	x	x	x	x	x	1	Channel 0 enable
x	x	x	x	x	x	0	x	Channel 1 disable
x	x	x	x	x	x	1	x	Channel 1 enable
x	x	x	x	x	0	x	x	Channel 2 disable
x	x	x	x	x	1	x	x	Channel 2 enable
x	x	x	x	0	x	x	x	Channel 3 disable
x	x	x	x	1	x	x	x	Channel 3 enable
x	x	x	0	x	x	x	x	Channel 4 disable
x	x	x	1	x	x	x	x	Channel 4 enable
x	x	0	x	x	x	x	x	Channel 5 disable
x	x	1	x	x	x	x	x	Channel 5 enable
x	0	x	x	x	x	x	x	Channel 6 disable
x	1	x	x	x	x	x	x	Channel 6 enable
0	x	x	x	x	x	x	x	Channel 7 disable
1	x	x	x	x	x	x	x	Channel 7 enable

(1) Multiple channels can be enabled at the same time. Example: B7 = 0, B6 = 1, B5 = 0, B4 = 0, B3 = 1, B2 =1, B1 = 0, B0 = 0, which means that channels 7, 5, 4, 1, and 0 are disabled and channels 6, 3, and 2 are enabled. Care should be taken not to exceed the maximum bus capacitance. The default condition is all zeroes.

Tape and Reel Information





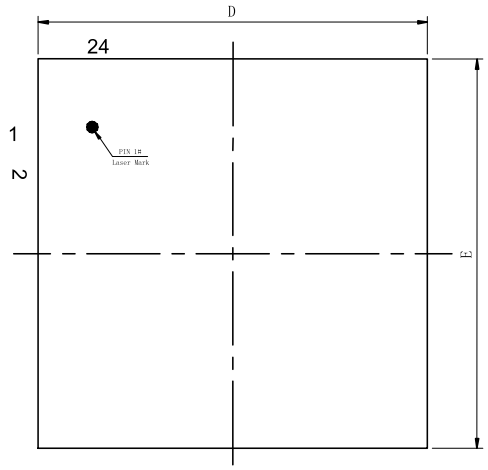


Order Number	Package	D1 (mm)	A0 (mm)	K0 (mm)	W0 (mm)	W1 (mm)	B0 (mm)	P0 (mm)	Pin1 Quadrant
TPT29548T-QF8R-S	24-Pin QFN	330	4.3	1.1	12	17.6	4.3	8	Q2

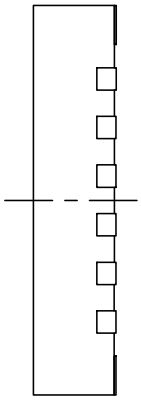
Package Outline Dimensions

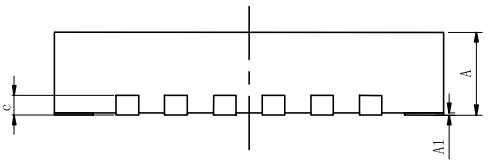
QFN4X4-24

Package Outline Dimensions QF8(QFN4X4-24-B)

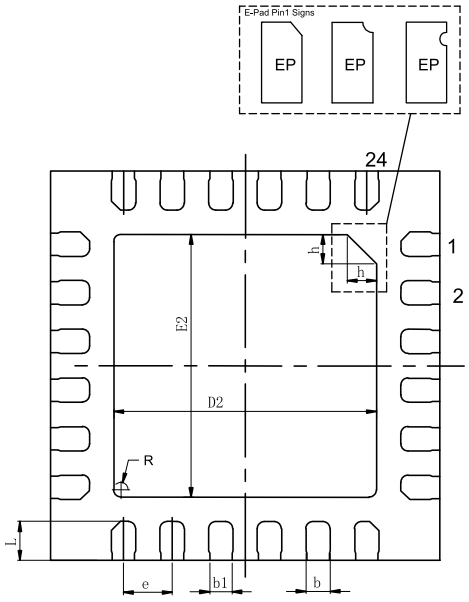


TOP VIEW





SIDE VIEW



BOTTOM VIEW

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	0.900	0.031	0.035
A1	0.000	0.050	0.000	0.002
b	0.200	0.300	0.008	0.012
b1	0.160 REF		0.006 REF	
c	0.180	0.250	0.007	0.010
D	3.900	4.100	0.154	0.161
E	3.900	4.100	0.154	0.161
e	0.500 BSC		0.020 BSC	
L	0.350	0.450	0.014	0.018
D2	2.150	2.350	0.085	0.093
E2	2.150	2.350	0.085	0.093
h	0.300	0.400	0.008	0.016

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT29548T-QF8R-S	−40 to 125°C	QFN4X4-24	9548T	MSL3	3,000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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