UCx854 High-Power Factor Preregulator

1 Features

- Control Boost PWM to 0.99 Power Factor
- Limit Line-Current Distortion to < 5%
- World-Wide Operation Without Switches
- Feedforward Line Regulation
- Average Current-Mode Control
- Low Noise Sensitivity
- Low Startup Supply Current
- Fixed-Frequency PWM Drive
- Low-Offset Analog Multiplier and Divider
- 1-A Totem-Pole Gate Driver
- Precision Voltage Reference

2 Applications

- Offline AC-to-DC Converters
- Medical, Industrial, Telecom, and IT Power Supplies
- Uninterruptible Power Supplies (UPS)
- Appliances and White Goods

3 Description

The UC1854 provides active-power factor correction for power systems that otherwise would draw non-sinusoidal current from sinusoidal power lines. This device implements all the control functions necessary to build a power supply capable of optimally using available power-line current while minimizing line-current distortion. To do this, the UC1854 contains a voltage amplifier, an analog multiplier and divider, a current amplifier, and a fixed-frequency PWM.

In addition, the UC1854 contains a power MOSFET-compatible gate driver, 7.5-V reference, line anticipator, load-enable comparator, low-supply detector, and overcurrent comparator.

The UC1854 uses average current-mode control to accomplish fixed-frequency current control with stability and low distortion. Unlike peak current-mode, average current control accurately maintains sinusoidal line current without slope compensation and with minimal response to noise transients.

The high reference voltage and high oscillator amplitude of the UC1854 minimize noise sensitivity while fast PWM elements permit chopping frequencies above 200 kHz. The UC1854 is used in single-phase and three-phase systems with line voltages that vary from 75 V to 275 V and line frequencies across the 50-Hz to 400-Hz range. To reduce the burden on the circuitry that supplies power to this device, the UC1854 features low starting supply current.

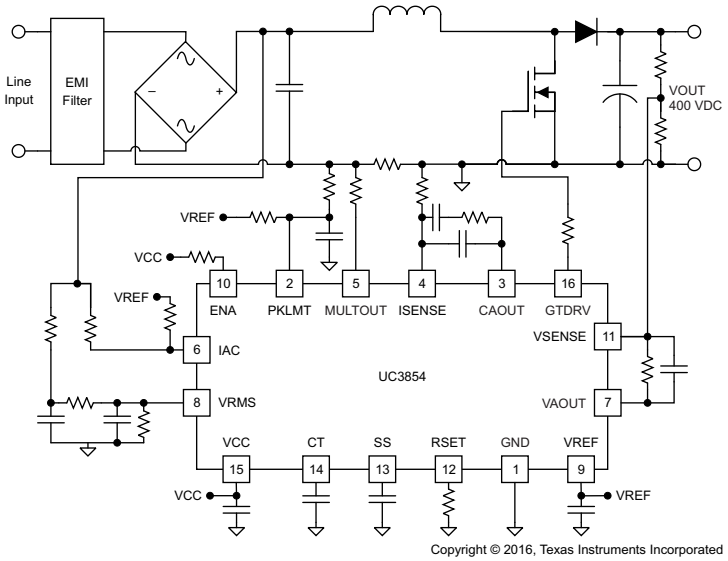
These devices are available packaged in 16-pin plastic and ceramic dual in-line packages, and a variety of surface-mount packages.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UC1854, UC2854, UC3854	SOIC (16)	7.50 mm × 10.30 mm
	PLCC (20)	8.96 mm × 8.96 mm
	CDIP (16)	6.92 mm × 19.56 mm
	PDIP (16)	6.35 mm × 19.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

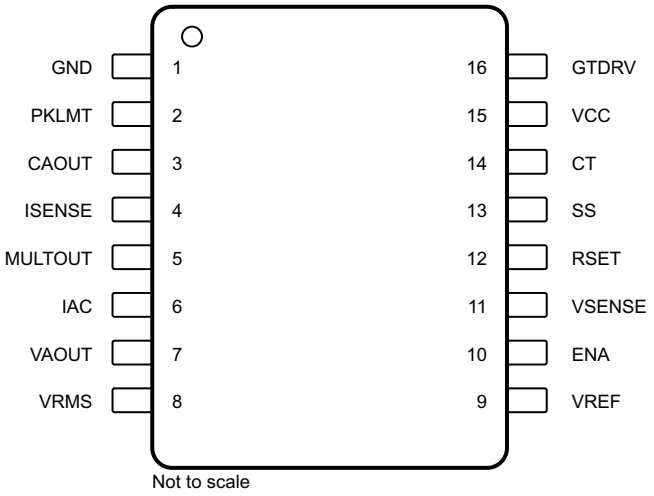
Changes from Original (June 1998) to Revision A	Page
• Added *Applications* section, *Device Information* table, *Pin Configuration and Functions* section, *Specifications* section, *ESD Ratings* table, *Recommended Operating Conditions* table, *Detailed Description* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Added *Thermal Information* table	6
• Changed IAC value in both Multiplier Output vs Multiplier Inputs images from mA to µA.	8

5 Device Comparison Table

PARAMETER	UC3854	UC3854A	UC3854B
Supply current, OFF	2-mA maximum	400-µA maximum	400-µA maximum
Supply voltage (V_{CC})	35-V maximum	22-V maximum	22-V maximum
VCC turn-on threshold	16-V typical	16-V typical	10.5-V typical
VCC UVLO hysteresis	6-V typical	6-V typical	0.5-V typical
Current amplifier bandwidth	1-MHz typical	5-MHz typical	5-MHz typical
Current amplifier offset	4-mV, –4-mV maximum	0-mV, –4-mV maximum	0-mV, –4-mV maximum
MULTOUT voltage (high)	2.5-V typical	5-V typical	5-V typical
Multiplier gain tolerance	Not specified	–0.9 to –1.1	–0.9 to –1.1
ENABLE propagation delay	Not specified	300-ns typical	300-ns typical
VSENSE input	7.5 V	3 V	3 V
IAC voltage	6-V typical	0.5-V typical	0.5-V typical
Voltage amplifier clamp	—	Internal	Internal
Current amplifier clamp	—	Internal	Internal
VREF good circuitry	—	Internal	Internal

6 Pin Configuration and Functions

DW, J, and N Packages
16-Pin SOIC, CDIP, and PDIP
Top View



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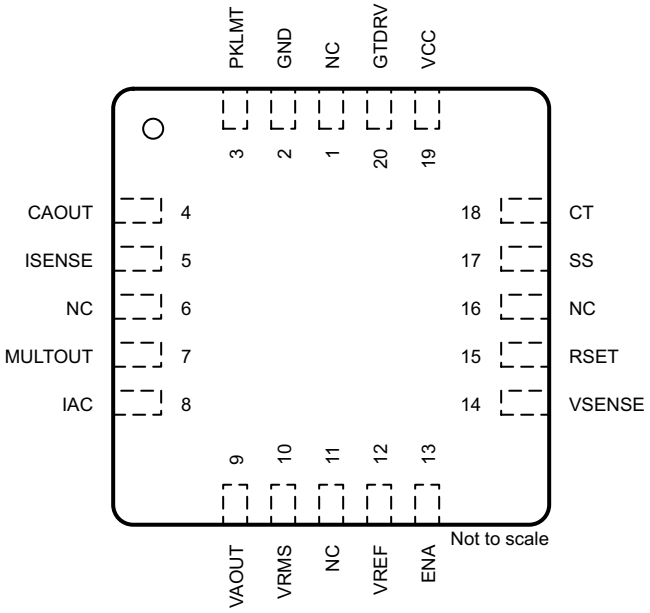
FN Package
20-Pin PLCC
Top View



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Pin Functions

PIN			I/O	DESCRIPTION
NAME	CDIP, PDIP, SOIC	PLCC		
CAOUT	3	4	O	Current amplifier output. This is the output of a wide-bandwidth operational amplifier that senses line current and commands the pulse-width modulator (PWM) to force the correct current. This output swings close to GND, allowing the PWM to force zero duty cycle when necessary. The current amplifier remains active even if the IC is disabled. The current-amplifier output stage is an NPN emitter-follower pullup and an 8-kΩ resistor to ground.
CT	14	18	I	Oscillator timing capacitor. A capacitor from CT to GND sets the PWM oscillator frequency. Use Equation 1: $F = \frac{1.25}{R_{SET} \times C_T}$ (1)
ENA	10	13	I	Enable. ENA is a logic input that enables the PWM output, voltage reference, and oscillator. ENA also releases the soft-start clamp, allowing SS to rise. When not in use, connect ENA to a 5-V supply or pull ENA high with a 22-kΩ resistor. The ENA pin is not intended to be used as a high speed shutdown to the PWM output.
GND	1	2	—	Ground. All voltages are measured with respect to GND. VCC and VREF must be bypassed directly to GND with an 0.1-µF or larger ceramic capacitor. The timing capacitor discharge current also returns to this pin, so the lead from the oscillator timing capacitor to GND must also be as short and as direct as possible.
GTDRV	16	20	O	Gate drive. The output of the PWM is a totem-pole MOSFET gate driver on GTDRV. This output is internally clamped to 15 V so that the IC operates with V_{CC} as high as 35 V. Use a series gate resistor of at least 5 Ω to prevent interaction between the gate impedance and the GTDRV output driver that might cause the GTDRV output to overshoot excessively. Some overshoot of the GTDRV output is always expected when driving a capacitive load.
IAC	6	8	I	Input AC current. This input to the analog multiplier is a current. The multiplier is tailored for very low distortion from this current input (IAC) to MULTOUT, this is the only multiplier input that must be used for sensing instantaneous line voltage. The nominal voltage on IAC is 6 V, in addition to a resistor from IAC to rectified 60 Hz, connect a resistor from IAC to REF. If the resistor to VREF is one-fourth of the value of the resistor to the rectifier, then the 6-V offset is cancelled, and the line current has minimal cross-over distortion.
ISENSE	4	5	I	Current-sense minus. This is the inverting input to the current amplifier. This input and the non-inverting input, MULTOUT, remain functional down to and below GND. Take care to avoid taking these inputs below –0.5 V because they are protected with diodes to GND.
MULTOUT	5	7	I/O	Multiplier output and current-sense plus. The output of the analog multiplier and the non-inverting input of the current amplifier are connected together at MULTOUT. The cautions about taking ISENSE below –0.5 V also apply to MULTOUT. As the multiplier output is a current, this is a high-impedance input similar to ISENSE, so the current amplifier can be configured as a differential amplifier to reject GND noise. Figure 9 shows an example of using the current amplifier differentially.
NC	—	1, 6, 11, 16	—	No connection
PKLMT	2	3	I	Peak current limit. The threshold for PKLMT is 0 V. Connect this input to the negative voltage on the current-sense resistor as shown in Figure 9. Use a resistor to VREF to offset the negative current-sense signal up to GND.
RSET	12	15	I	Oscillator charging current and multiplier limit set. A resistor from RSET to GND programs oscillator charging current and maximum multiplier output. Multiplier output current does not exceed 3.75 V divided by the resistor from RSET to GND.
SS	13	17	I	Soft start. SS remains at GND as long as the device is disabled or V_{CC} is too low. SS pulls up to over 8 V by an internal 14-mA current source when both V_{CC} becomes valid and the IC is enabled. SS acts as the reference input to the voltage amplifier if SS is below VREF. With a large capacitor from SS to GND, the reference to the voltage regulating amplifier rises slowly, and increases the PWM duty cycle slowly. In the event of a disable command or a supply dropout, SS quickly discharges to ground and disables the PWM.
VAOUT	7	9	O	Voltage amplifier output. This is the output of the operational amplifier that regulates output voltage. Like the current amplifier, the voltage amplifier remains active even if the IC is disabled with either ENA or VCC. This means that large feedback capacitors across the amplifier stay charged through momentary disable cycles. Voltage amplifier output levels below 1 V inhibit multiplier output. The voltage amplifier output is internally limited to approximately 5.8 V to prevent overshoot. The voltage amplifier output stage is an NPN emitter-follower pullup and an 8-kΩ resistor to ground.

Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	CDIP, PDIP, SOIC	PLCC		
VCC	15	19	—	Positive supply voltage. Connect VCC to a stable source of at least 20 mA above 17 V for normal operation. Also bypass VCC directly to GND to absorb supply current spikes required to charge external MOSFET gate capacitances. To prevent inadequate GTDRV signals, these devices are inhibited unless V_{CC} exceeds the upper undervoltage-lockout threshold and remains above the lower threshold.
VREF	9	12	O	Voltage reference output. VREF is the output of an accurate 7.5-V voltage reference. This output is capable of delivering 10 mA to peripheral circuitry and is internally short-circuit current limited. VREF is disabled and remains at 0 V when V_{CC} is low or when ENA is low. Bypass VREF to GND with an 0.1-µF or larger ceramic capacitor for best stability.
VRMS	8	10	I	RMS line voltage. The output of a boost PWM is proportional to the input voltage, so when the line voltage into a low-bandwidth boost PWM-voltage regulator changes, the output changes immediately and slowly recovers to the regulated level. For these devices, the VRMS input compensates for line voltage changes if it is connected to a voltage proportional to the RMS input line voltage. For best control, the VRMS voltage must stay between 1.5 V and 3.5 V.
VSENSE	11	14	I	Voltage amplifier inverting input. This is normally connected to a feedback network and to the boost converter output through a divider network.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)(4)(5)

		MIN	MAX	UNIT
Supply voltage	VCC		35	V
Input Voltage	VSENSE, VRMS		11	V
	ISENSE, MULTOUT		11	
	PKLMT		5	
Gate driver current Input current	50% duty cycle		1.5	A
	Continuous		0.5	
Input current	RSET, IAC, PKLMT, ENA		10	mA
Power dissipation			1	W
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages with respect to GND.
(3) All currents are positive into the specified terminal.
(4) ENA input is internally clamped to approximately 14 V.
(5) Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		10	20	
T_J	Operating junction temperature	UC1854	–55	125	°C
		UC2854	–40	85	
		UC3854	0	70	

7.4 Thermal Information

THERMAL METRIC[1]		UCx854				UNIT
		DW (SOIC)	FN (PLCC)	J (CDIP)	N (PDIP)	
		16 PINS	20 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	71.5	—	25	40.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.7	—	—	26.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36.3	—	5.5	20.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.8	—	2.1	10.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	35.8	—	5.4	20.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	3.4	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Unless otherwise stated, V_{CC} = 18 V, R_{SET} = 15 kΩ to ground, C_T = 1.5 nF to ground, V_{PKLMT} = 1 V, V_{ENA} = 7.5 V, V_{RMS} = 1.5 V, I_{AC} = 100 µA, V_{ISENSE} = 0 V, V_{CAOUT} = 3.5 V, V_{VAOUT} = 5 V, V_{SENSE} = 7.5 V, no load on SS, CAOUT, VAOUT, VREF, GTDRV, $T_A = T_J$, T_A = –55°C to 125°C for the UC1854, T_A = –40°C to 85°C for the UC2854, and T_A = 0°C to 70°C for the UC3854.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVERALL						
	Supply current, OFF	V_{ENA} = 0 V		1.5	2	mA
	Supply current, ON			10	16	mA
	V_{CC} turn-on threshold		14.5	16	17.5	V
	V_{CC} turn-off threshold		9	10	11	V
	ENA threshold, rising		2.4	2.55	2.7	V
	ENA threshold hysteresis		0.2	0.25	0.3	V
	ENA input current	V_{ENA} = 0 V	–5	–0.2	5	µA
	V_{RMS} input current	V_{RMS} = 5 V	–1	–0.01	1	µA
VOLTAGE AMPLIFIER						
	Voltage amplifier offset voltage	V_{VAOUT} = 5 V	–8		8	mV
	VSENSE bias current		–500	–25	500	nA
	Voltage amplifier gain		70	100		dB
	Voltage amplifier output swing		0.5		5.8	V
	Voltage amplifier short circuit current	V_{VAOUT} = 0 V	–36	–20	–5	mA
	SS current	V_{SS} = 2.5 V	–20	–14	–6	µA
CURRENT AMPLIFIER						
	Current amplifier offset voltage		–4		4	mV
	ISENSE bias current		–500	–120	500	nA
	Input range (ISENSE, MULTOUT)		–0.3		2.5	V
	Current amplifier gain		80	110		dB

Electrical Characteristics (continued)

Unless otherwise stated, V_{CC} = 18 V, R_{SET} = 15 kΩ to ground, C_T = 1.5 nF to ground, V_{PKLMT} = 1 V, V_{ENA} = 7.5 V, V_{RMS} = 1.5 V, I_{AC} = 100 µA, V_{ISENSE} = 0 V, V_{CAOUT} = 3.5 V, V_{VAOUT} = 5 V, V_{SENSE} = 7.5 V, no load on SS, CAOUT, VAOUT, VREF, GTDRV, $T_A = T_J$, T_A = –55°C to 125°C for the UC1854, T_A = –40°C to 85°C for the UC2854, and T_A = 0°C to 70°C for the UC3854.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current amplifier output swing		0.5		16	V
Current amplifier short-circuit current	V_{CAOUT} = 0 V	–36	–20	–5	mA
Current amplifier gain–bandwidth product	T_A = 25°C (1)	400	800		kHz
REFERENCE					
Reference output voltage	I_{REF} = 0 mA, T_A = 25°C	7.4	7.5	7.6	V
Reference output voltage	I_{REF} = 0 mA, over temperature	7.35	7.5	7.65	V
VREF load regulation	–10 mA < I_{REF} < 0 mA	–15	5	15	mV
VREF line regulation	15 V < V_{CC} < 35 V	–10	2	10	mV
VREF short circuit current	V_{REF} = 0 V	–50	–28	–12	mA
MULTIPLIER					
Multiplier out current IAC limited	I_{AC} = 100 µA, R_{SET} = 10 kΩ, V_{RMS} = 1.25 V	–220	–200	–180	µA
Multiplier out current zero	I_{AC} = 0 µA, R_{SET} = 15 kΩ	–2	–0.2	–2	µA
Multiplier out current RSET limited	I_{AC} = 450 µA, R_{SET} = 15 kΩ, V_{RMS} = 1 V, V_{VAOUT} = 6 V	–280	–255	–220	µA
Multiplier out current	I_{AC} = 50 µA, V_{RMS} = 2 V, V_{VAOUT} = 4 V	–50	–42	–33	µA
Multiplier out current	I_{AC} = 100 µA, V_{RMS} = 2 V, V_{VAOUT} = 2 V	–38	–27	–12	µA
Multiplier out current	I_{AC} = 200 µA, V_{RMS} = 2 V, V_{VAOUT} = 4 V	–165	–150	–105	µA
Multiplier out current	I_{AC} = 300 µA, V_{RMS} = 1 V, V_{VAOUT} = 2 V	–250	–225	–150	µA
Multiplier out current	I_{AC} = 100 µA, V_{RMS} = 1 V, V_{VAOUT} = 2 V	–95	–80	–60	µA
Multiplier gain constant	See (2)		–1		V
OSCILLATOR					
Oscillator frequency	R_{SET} = 15 kΩ	46	55	62	kHz
Oscillator frequency	R_{SET} = 8.2 kΩ	86	102	118	kHz
CT ramp peak-to-valley amplitude		4.9	5.4	5.9	V
CT ramp valley voltage		0.8	1.1	1.3	V
GATE DRIVER (GTDRV)					
Maximum gate driver output voltage	0-mA load on gate driver, 18 V < V_{CC} < 35 V	13	14.5	18	V
Gate driver output voltage high	–200-mA load on gate driver, V_{CC} = 15 V	12	12.8		V
Gate driver output voltage low, OFF	V_{CC} = 0 V, 50-mA load on gate driver		0.9	1.5	V
Gate driver output voltage low	200-mA load on gate driver		1	2.2	V
Gate driver output voltage low	10-mA load on gate driver		0.1	0.4	V
Peak Gate driver current	10 nF from gate driver to GND		1		A
Gate driver rise and fall time	1 nF from gate driver to GND		35		ns
Gate driver maximum duty cycle	V_{CAOUT} = 7 V		95%		
CURRENT LIMIT					
PKLMT offset voltage		–10		10	mV
PKLMT input current	V_{PKLMT} = –0.1 V	–200	–100		µA
PKLMT to gate driver delay	V_{PKLMT} falling from 50 to –50 mV		175		ns

(1) Specified by design. Not production tested.

(2) Multiplier gain constant (k) is defined by:

$$I_{Mult\,Out} = \frac{k \times I_{AC} \times (VA\,Out - 1)}{V_{RMS}^2}$$

7.6 Typical Characteristics

$T_A = T_J = 25°C$

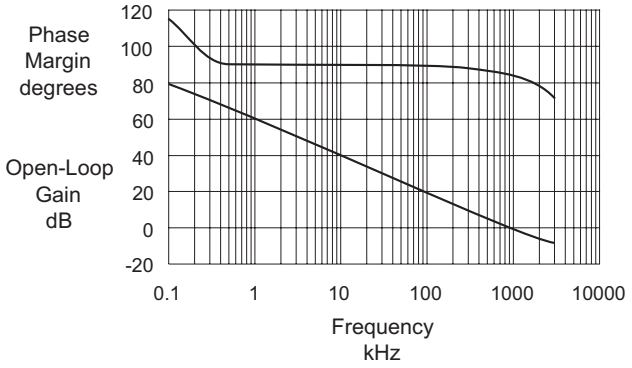


Figure 1. Current Amplifier Gain and Phase vs Frequency

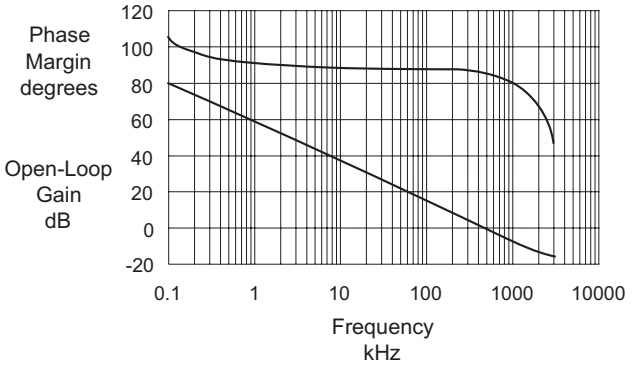


Figure 2. Voltage Amplifier Gain and Phase vs Frequency

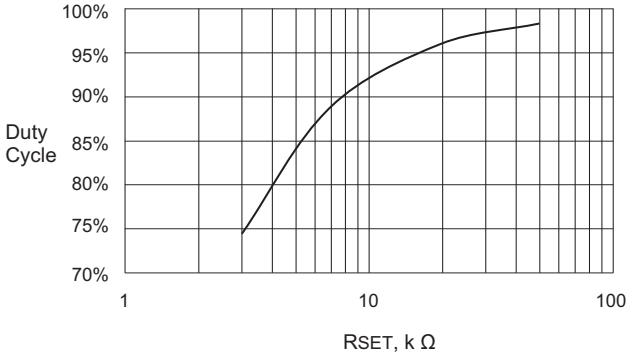


Figure 3. Gate-Drive Maximum Duty Cycle

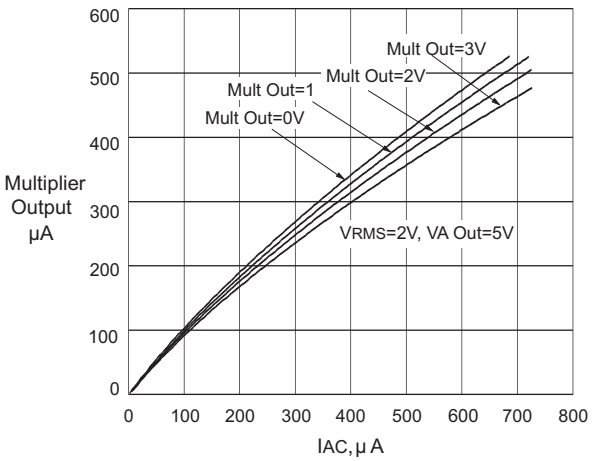


Figure 4. Multiplier Output vs Voltage On MULTOUT

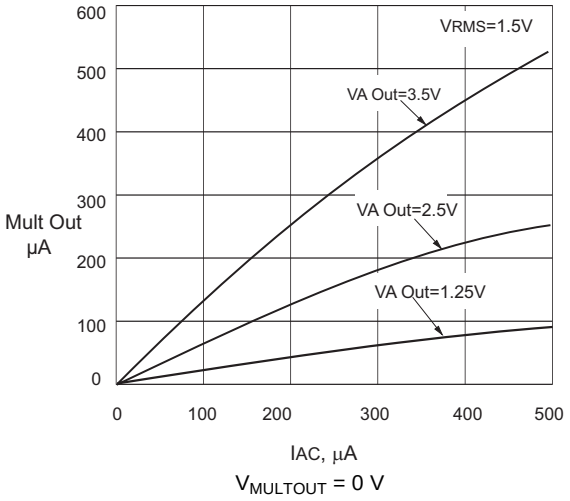


Figure 5. Multiplier Output vs Multiplier Inputs

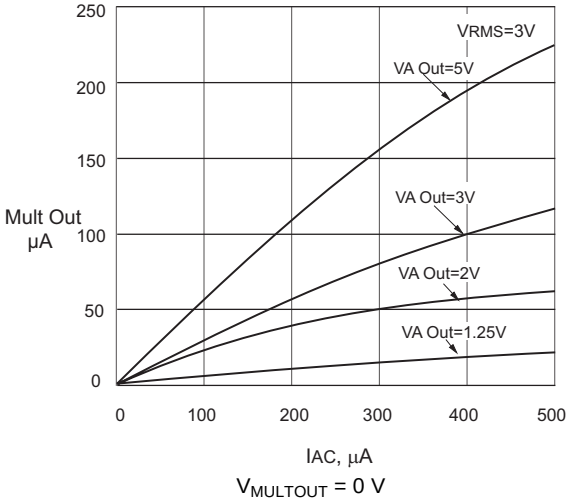


Figure 6. Multiplier Output vs Multiplier Inputs

Typical Characteristics (continued)

$T_A = T_J = 25°C$

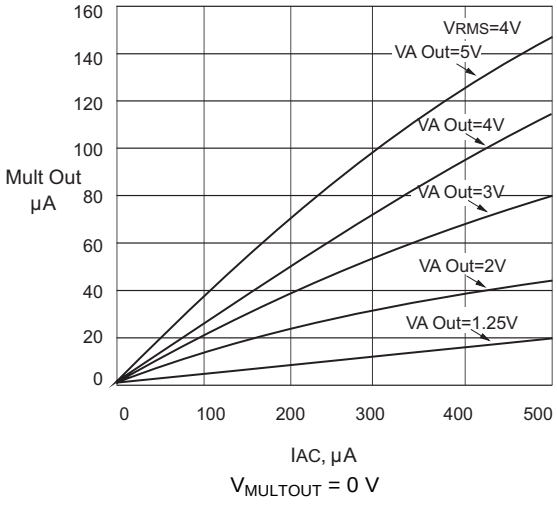


Figure 7. Multiplier Output vs Multiplier Inputs

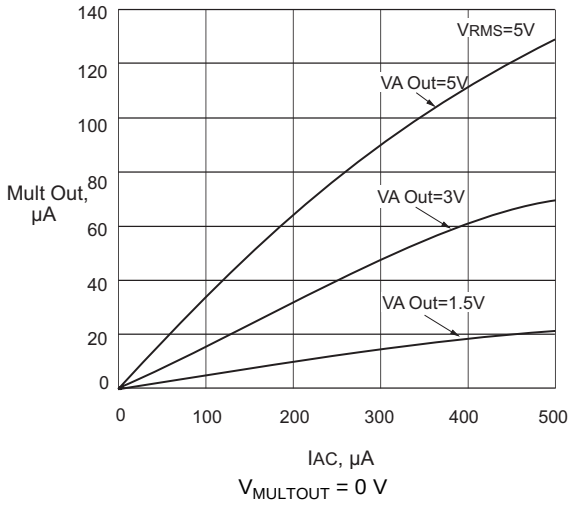


Figure 8. Multiplier Output vs Multiplier Inputs

8 Detailed Description

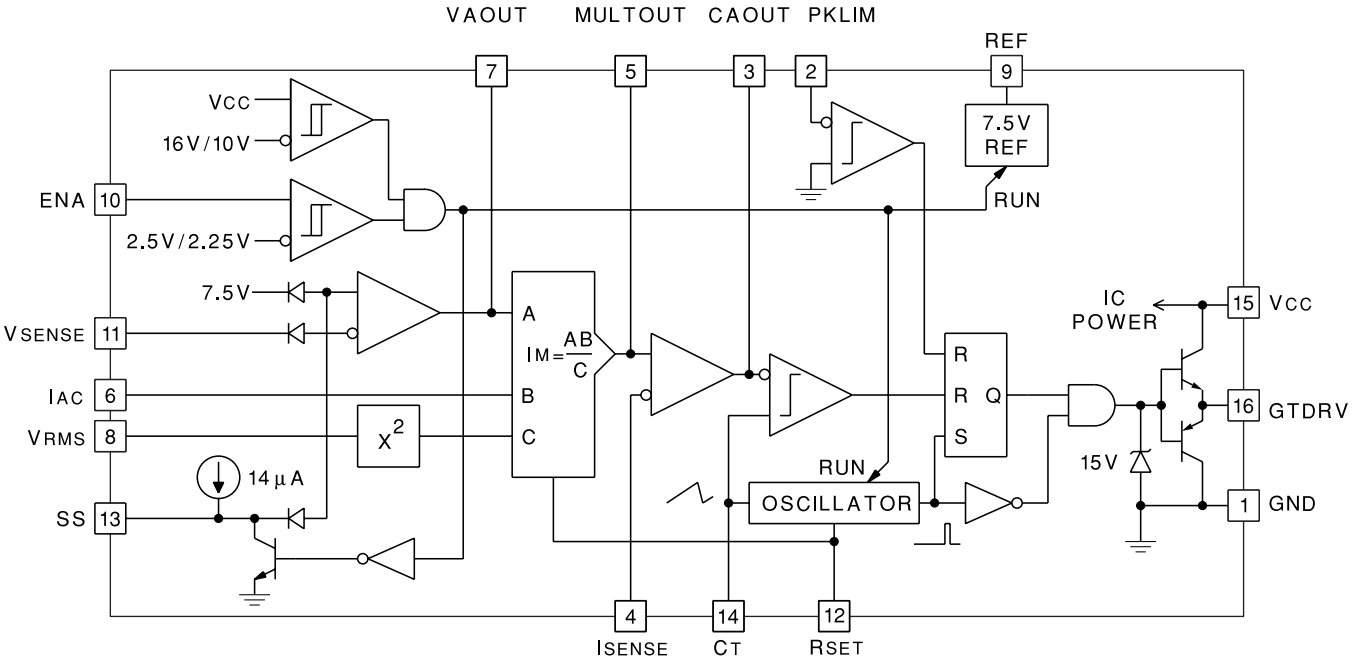
8.1 Overview

The UC3854 provides active power factor correction for systems that otherwise would draw non-sinusoidal current from sinusoidal power lines. This device implements all the control functions necessary to build a power supply capable of optimally using available power-line current while minimizing line current distortion.

The UC3854 uses average current-mode control to accomplish fixed-frequency current control with stability and low distortion. The UC3854, with average current mode control, allows the boost stage to move between continuous and discontinuous modes of operation without a performance change. Unlike peak current-mode, average current control accurately maintains sinusoidal line current without slope compensation and with minimal response to noise transients.

The UC3854 implements all the control functions necessary to build a power supply capable of optimally using available power-line current while minimizing line-current distortion. The UC3854 contains a voltage amplifier, an analog multiplier and divider, a current amplifier, and a fixed-frequency PWM. In addition, the UC3854 contains a power MOSFET compatible gate driver, 7.5-V reference, line anticipator, load-enable comparator, low-supply detector, and over-current comparator.

8.2 Functional Block Diagram



8.3 Feature Description

The UC3854 integrated circuit contains all the circuits necessary to control a power factor corrector. The UC3854 is designed to implement average current mode control but is flexible enough to be used for a wide variety of power topologies and control methods.

The top left corner, of the UC3854 block diagram, contains the under voltage lock out comparator and the enable comparator. The output of both of these comparators must be true to allow the device to operate. The inverting input to the voltage error amplifier is connected to pin VSENSE. The diodes shown around the voltage error amplifier are intended to represent the functioning of the internal circuits rather than to show the actual devices. The diodes shown in the block diagram are ideal diodes and indicate that the non-inverting input to the error amplifier is connected to the 7.5-V DC reference voltage under normal operation but is also used for the soft-start function. This configuration lets the voltage control loop begin operation before the output voltage has reached its operating point and eliminates the turn-on overshoot which plagues many power supplies. The diode shown between VSENSE and the inverting input of the error amplifier is also an ideal diode and is shown to eliminate confusion about whether there might be an extra diode drop added to the reference or not. In the actual device we do it with differential amplifiers. An internal current source is also provided for charging the soft-start timing capacitor.

The output of the voltage error amplifier is available on pin VAOUT, of the UC3854, and it is also an input to the multiplier. The other input to the multiplier is lAC, and this is the input for the programming wave shape from the input rectifiers. This pin is held, internally, at 6 V and is a current input. The feedforward input is V_{FF}, and its value is squared before being fed into the divider input of the multiplier. The current (I_{SET}) from the RSET pin is also used in the multiplier to limit the maximum output current. The output current of the multiplier is I_{MO} and it flows out of pin MULTOUT which is also connected to the non-inverting input of the current error amplifier.

The inverting input of the current amplifier is connected to pin ISENSE. The output of the current error amplifier connects to the pulse width modulation (PWM) comparator where it is compared to the oscillator ramp on pin CT. The oscillator and the comparator drive the set-reset flip-flop which, in turn, drives the high current output on pin GTDRV. The output voltage is clamped internally to the UC3854 at 15 V so that power MOSFETs do not have their gates over driven. An emergency peak current limit is provided on pin PKLMT and it shuts off the output pulse when it is pulled slightly below ground. The reference voltage output is connected to pin VREF and the input voltage is connected to pin VCC.

8.4 Device Functional Modes

This device has no functional modes.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The UC3854 control IC is generally applicable to the control of AC-DC power supplies that require Active Power Factor Correction off Universal AC line. Applications using this IC generally meets the Class D equipment input current harmonics standards per EN61000-3-2. This standard applies to equipment with rated powers higher than 75 W.

Performance of the UC3854 Power Factor correction IC in a 250-W application example has been evaluated using a precision PFC and THD instrument. The result was a power factor of 0.999 and Total Harmonic Distortion (THD) of 3.81%, measured to the 50th line frequency harmonic at nominal line and full load.

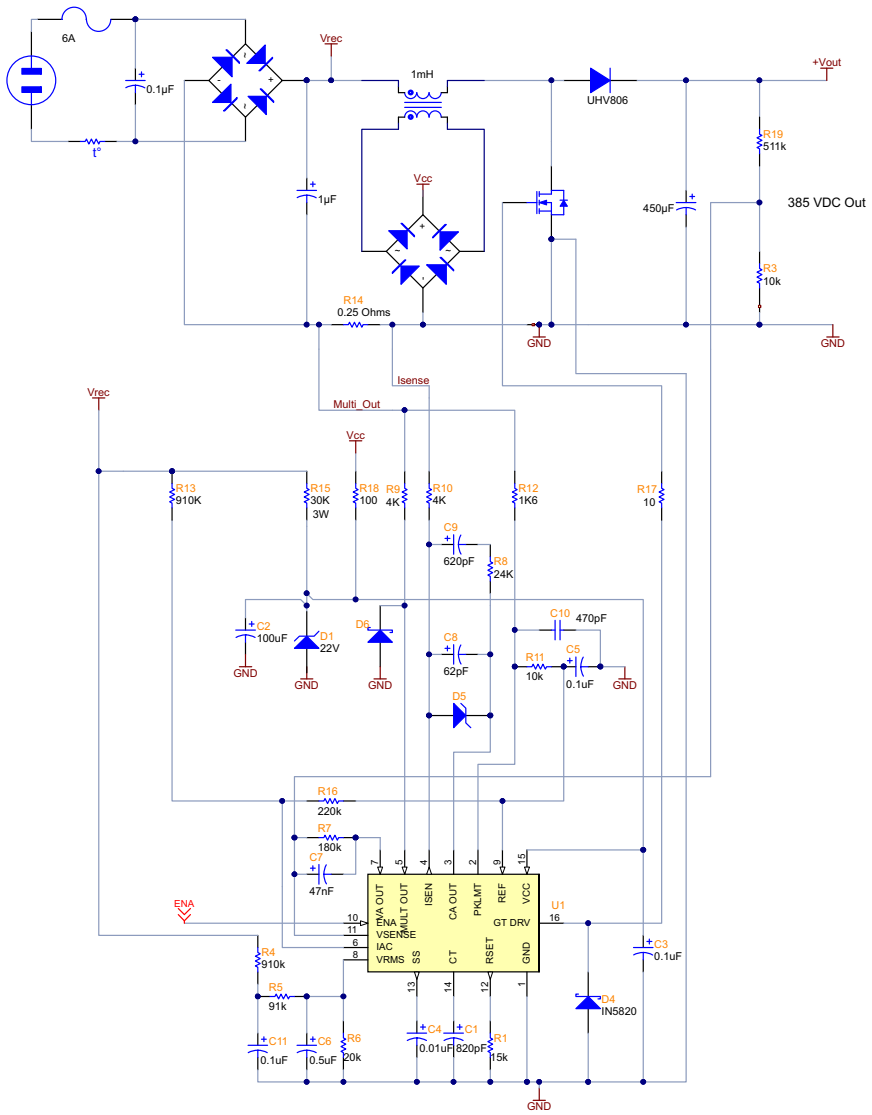
9.2 Typical Application

The circuit of Figure 9 shows a typical application of the UC3854 as a preregulator with high power factor and efficiency. The assembly consists of two distinct parts: the control circuit centering on the UC3854 and the power section.

The power section is a *boost* converter, with the inductor operating in continuous mode. In this mode, the duty cycle is dependent on the ratio between input and output voltages; also, the input current has low switching-frequency ripple, which means that the line noise is low. Furthermore, the output voltage must be higher than the peak value of the highest expected AC line voltage, and all components must be rated accordingly.

At full load, this preregulator exhibits a power factor of 0.99 at any power line voltage from 80 V to 260 V_{RMS}. This same circuit is used at higher power levels with minor modifications to the power stage. See *Optimizing Performance in UC3854 Power Factor Correction Applications* and *UC3854 Controlled Power Factor Correction Circuit Design*.

Typical Application (continued)



Boost inductor is fabricated with ARNOLD MPP toroidal core part number A-438381-2, using a 55-turn primary and a 13-turn secondary.

Figure 9. 250-W Preregulator Application

Typical Application (continued)

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER		MIN	TYP	MAX	UNIT
V_{IN}	RMS input voltage	80		260	V_{RMS}
V_{OUT}	Output voltage		390		V
f_{Line}	AC line frequency	47		65	Hz
$P_{OUT(max)}$	Maximum output power			250	W

9.2.2 Detailed Design Procedure

In the control section, the UC3854 provides PWM pulses (GTDRV) to the power MOSFET gate. The duty cycle of this output is simultaneously controlled by four separate inputs to the chip.

Table 2. Output Duty Cycle

INPUT PIN	FUNCTION
VSENSE	Output DC voltage
IAC	Line voltage waveform
ISENSE, MULTOUT	Line current
VRMS	RMS line voltage

Additional controls of an auxiliary nature are provided. They are intended to protect the switching power MOSFETS from certain transient conditions.

Table 3. Additional Controls of the Output Duty Cycle

INPUT PIN	FUNCTION
ENA	Startup delay
SS	Soft start
PKLMT	Maximum current limit

9.2.2.1 Protection Inputs

ENA (Enable): The ENA input must reach 2.5 V before the VREF and GTDRV outputs are enabled. This provides a means to shut down the gate in case of trouble, or to add a time delay at power up. A hysteresis gap of 200 mV is provided at this terminal to prevent erratic operation. Undervoltage protection is provided directly at VCC, where the on and off thresholds are 16 V and 10 V. If the ENA input is unused, it must be pulled up to V_{CC} through a current-limiting resistor of 100 kΩ.

SS (Soft Start): The voltage at SS pin reduces the reference voltage used by the error amplifier to regulate the output DC voltage. With SS open, the reference voltage is typically 7.5 V. An internal current source delivers approximately 14 mA from SS. Thus a capacitor (C_{SS}) connected between SS and ground charges linearly from 0 V to 7.5 V in [0.54 × C_{SS} (µF)] s.

PKLMT (Peak Current Limit): Use PKLIM to establish the highest value of current to be controlled by the power MOSFET. With the resistor divider values shown in Figure 9, the 0-V threshold at PKLIM is reached when the voltage drop across the 0.25-Ω current-sense resistor is 7.5 V × 2 k / 10 k = 1.5 V, corresponding to 6 A. TI recommends a bypass capacitor from PKLIM to GND to filter out very high frequency noise.

9.2.2.2 Control Inputs

VSENSE (Output DC Voltage Sense): The threshold voltage for the VSENSE input is 7.5 V and the input bias current is typically 50 nA. The values shown in Figure 9 are for an output voltage of 400-V DC. In this circuit, the voltage amplifier operates with a constant low-frequency gain for minimum output excursions. The 47-nF feedback capacitor places a 15-Hz pole in the voltage loop that prevents 120-Hz ripple from propagating to the input current.

IAC (Line Waveform): To force the line current waveshape to follow the line voltage, a sample of the power line voltage in waveform is introduced at IAC. This signal is multiplied by the output of the voltage amplifier in the internal multiplier to generate a reference signal for the current control loop.

This input is not a voltage, but a current (hence I_{AC}), and is set up by the 220-kΩ and 910-kΩ resistive divider (see Figure 12). The voltage at IAC is internally held at 6 V, and the two resistors are chosen so that the current flowing into IAC varies from zero (at each zero-crossing) to about 400 µA at the peak of the waveshape. The following formulas are used to calculate these resistors:

$$R_{AC} = \frac{V_{pk}}{I_{ACpk}} = \frac{260\text{VAC} \times \sqrt{2}}{400\ \mu\text{A}} = 910\ \text{k}$$

where

- V_{PK} is the peak line voltage (2)

$$R_{REF=} \frac{R_{AC}}{4} = 220\ \text{k} \quad (3)$$

ISENSE and MULTOUT (Line Current): The voltage drop across the 0.25-Ω current-sense resistor is applied to ISENSE and MULTOUT as shown. The current-sense amplifier also operates with high low-frequency gain, but unlike the voltage amplifier, it is set up to give the current-control loop a very wide bandwidth. This bandwidth enables the line current to follow the line voltage as closely as possible. In the present example, this amplifier has a zero at about 500 Hz, and a gain of about 18 dB thereafter.

VRMS (RMS Line Voltage): An important feature of the UC3854 preregulator is that it operates with a three-to-one range of input line voltages, covering everything from low line in the US (85 VAC) to high line in Europe (255 VAC). This is done using line feedforward, which keeps the input power constant with varying input voltage (assuming constant load power). To do this, the multiplier divides the line current by the square of the RMS value of the line voltage. The voltage applied to VRMS, proportional to the average of the rectified line voltage and proportional to the RMS value, is squared in the UC3854, and then used as a divisor by the multiplier block. The multiplier output, at MULTOUT, is a current that increases with the current at IAC and the voltage at VAOUT, and decreases with the square of the voltage at VRMS.

PWM Frequency: The PWM oscillator frequency in Figure 9 is 100 kHz. This value is determined by C_T at pin CT and R_{SET} at pin RSET. R_{SET} must be chosen first because it affects the maximum value of I_{MULT} according to the equation Equation 4.

$$I_{MULT_{MAX}} = \frac{-3.75\ \text{V}}{R_{SET}} \quad (4)$$

This effectively sets a maximum PWM-controlled current. With R_{SET} = 15 k,

$$I_{MULT_{MAX}} = \frac{-3.75\ \text{V}}{15\ \text{k}} = -250\ \mu\text{A} \quad (5)$$

Also note that the multiplier output current never exceeds twice I_{AC}.

With the 4-kΩ resistor from MULTOUT to the 0.25-Ω current-sense resistor, the maximum current in the current-sense resistor is:

$$I_{MAX} = \frac{-I_{MULT_{MAX}} \times 4\ \text{k}}{0.25\ \Omega} = -4\ \text{A} \quad (6)$$

Having thus selected R_{SET}, the current sense resistor, and the resistor from MULTOUT to the current sense resistor, calculate C_T for the desired PWM oscillator frequency from Equation 7.

$$C_T = \frac{1.25}{F \times R_{SET}} \quad (7)$$

9.2.3 Application Curves

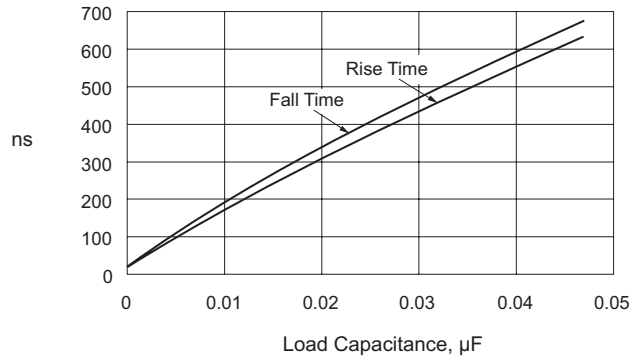


Figure 10. Gate-Drive Rise and Fall Time

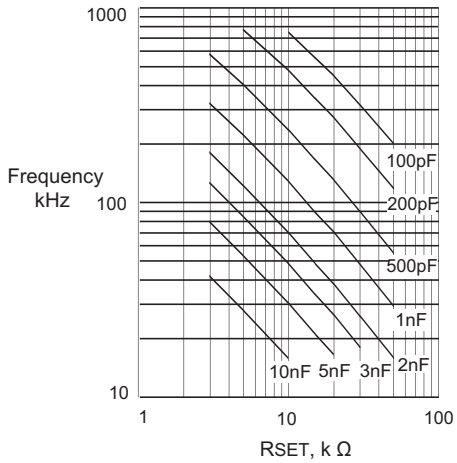


Figure 11. Oscillator Frequency vs R_{SET} and C_T

10 Power Supply Recommendations

Bypass the VCC pin directly to the GND pin, using a ceramic capacitor of at least 0.1 µF. This bypass capacitor absorbs supply current spikes required to charge external MOSFET gate capacitances.

VCC must be connected to a stable source that can deliver at least 20 mA. The VCC supply must exceed the VCC turnon threshold to start switching operation and must remain above the VCC turnoff threshold for normal operation.

A secondary winding on the PFC boost inductor can be used to deliver a regulated auxiliary bias supply with few external components as shown in Figure 12. Unlike more conventional and unregulated single diode or bridge rectifier techniques, this approach uses two diodes in a full wave configuration. This arrangement develops two separate voltages across capacitors C1 and C2 each with 120-Hz components. However, when these two are summed at capacitor C3, the line variations are cancelled, and a regulated auxiliary bias is obtained. The number of turns on the secondary winding adjusts the bias supply voltage.

A bootstrap resistor and storage capacitor must be added, as shown in Figure 12 when V_{CC} is obtained from a PFC boost inductor auxiliary winding. These parts must be added to ensure the UC3854 controller has sufficient VCC voltage to start up and operate through the soft-start process until sufficient voltage is available from the auxiliary winding.

11 Layout

11.1 Layout Guidelines

Figure 12 and Figure 13 show good layout practice. The timing capacitor (C1) and bypass capacitors for VCC and VREF (C3 and C5) must be connected directly from their respective pins to GND through the shortest route. Ensure that the ISEN and MULTOUT pins do not drop more than 0.5 V below the GND pin; accomplished by connecting a Schottky diode (D6) between GND and MULTOUT pins. The local controller GND must be connected to the power circuit at a single point between the source of the power MOSFET and the current sense resistor (R14). The power trace running between the power MOSFET source and current sense resistor (R14) must be kept short. Traces from the upper terminals of R9 and R10 must run directly to each side of the current sense resistor and not be shared with any other signal.

To minimize the possiblity of interference caused by magnetic coupling from the boost inductor, the device must be located at least 1 in. away from the boost inductor. TI recommends the device not be placed underneath magnetic elements.

11.2 Layout Example

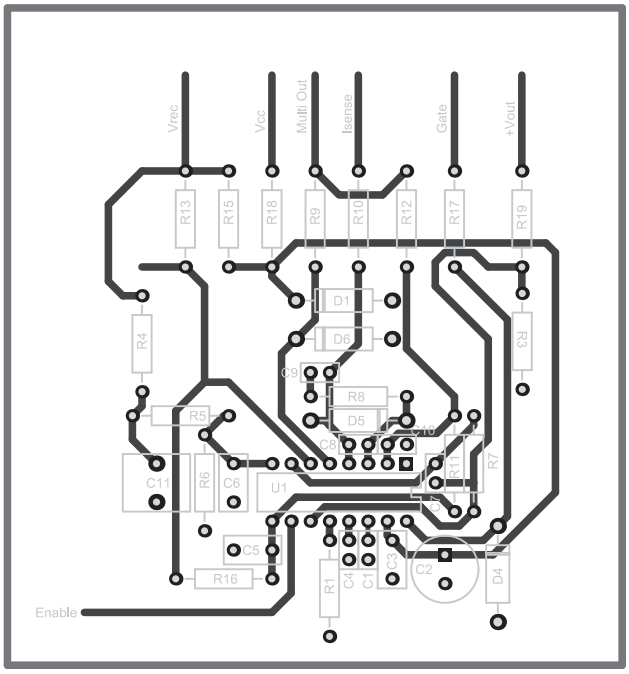


Figure 12. Layout Diagram (Top View)

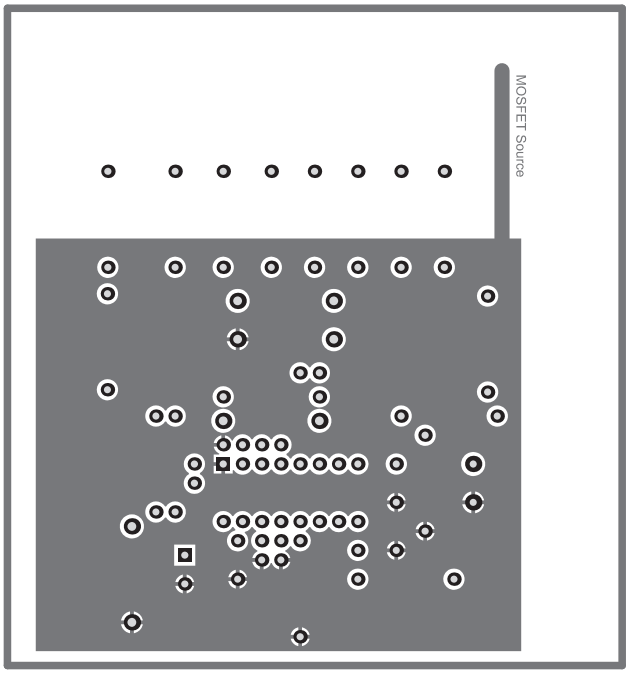


Figure 13. Layout Diagram (Bottom View)

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *Optimizing Performance in UC3854 Power Factor Correction Applications* (SLUA172)
- *UC3854 Controlled Power Factor Correction Circuit Design* (SLUA144)

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UC1854	Click here	Click here	Click here	Click here	Click here
UC2854	Click here	Click here	Click here	Click here	Click here
UC3854	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9326101MEA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9326101ME A UC1854J/883B	Samples
UC1854J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	UC1854J	Samples
UC1854J883B	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9326101ME A UC1854J/883B	Samples
UC2854BJ	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-40 to 85	UC2854BJ	Samples
UC2854DW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2854DW	Samples
UC2854DWTR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2854DW	Samples
UC2854N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	UC2854N	Samples
UC3854DW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3854DW	Samples
UC3854DWG4	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3854DW	Samples
UC3854DWTR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3854DW	Samples
UC3854DWTR-F	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3854DW-F	Samples
UC3854DWTRG4	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3854DW	Samples
UC3854N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	UC3854N	Samples
UC3854NG4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	UC3854N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF UC1854, UC2854, UC2854BM, UC3854 :

- Catalog : UC3854, UC2854B
- Enhanced Product : UC2854B-EP
- Military : UC2854M, UC1854

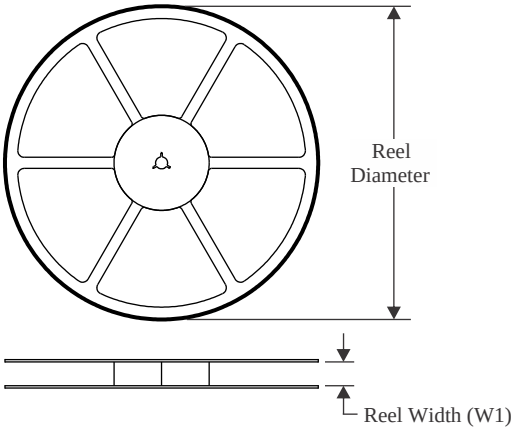
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

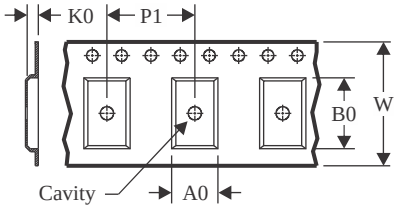
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

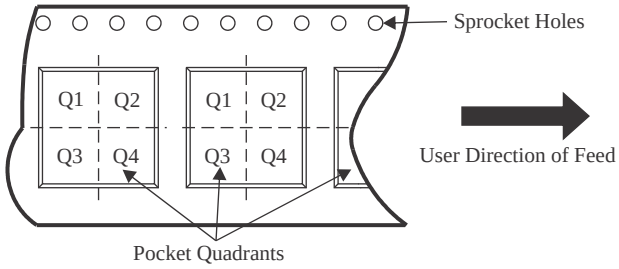


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

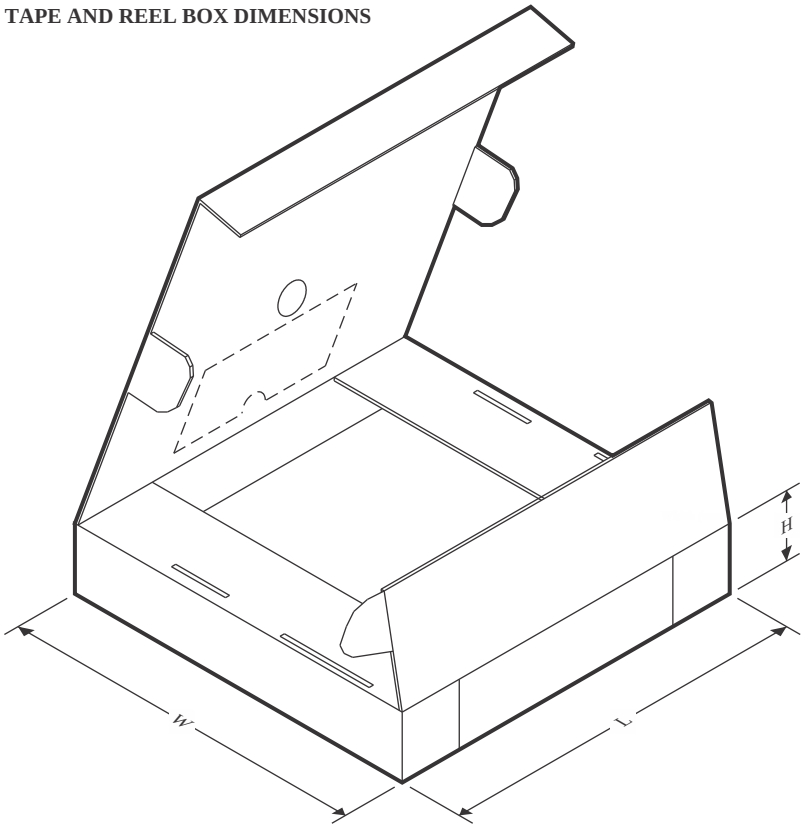
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2854DWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
UC3854DWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
UC3854DWTR-F	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

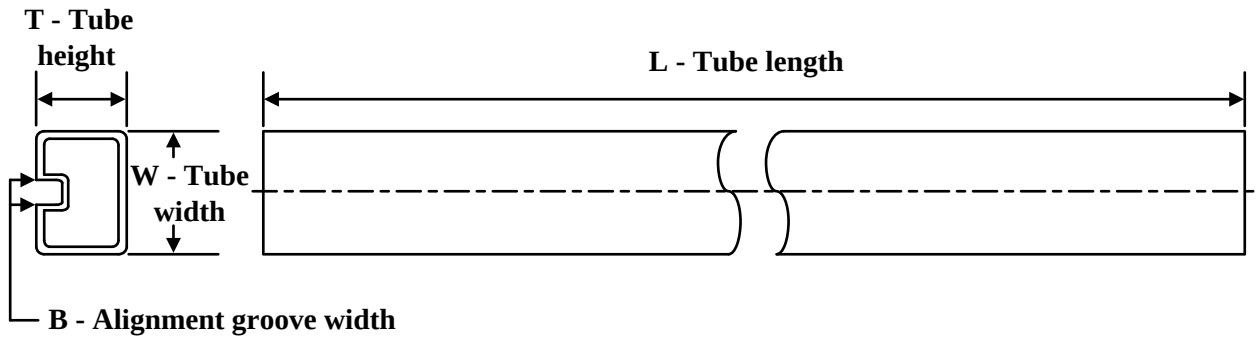
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2854DWTR	SOIC	DW	16	2000	367.0	367.0	38.0
UC3854DWTR	SOIC	DW	16	2000	367.0	367.0	38.0
UC3854DWTR-F	SOIC	DW	16	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UC2854DW	DW	SOIC	16	40	507	12.83	5080	6.6
UC2854N	N	PDIP	16	25	506	13.97	11230	4.32
UC3854DW	DW	SOIC	16	40	507	12.83	5080	6.6
UC3854DWG4	DW	SOIC	16	40	507	12.83	5080	6.6
UC3854N	N	PDIP	16	25	506	13.97	11230	4.32
UC3854NG4	N	PDIP	16	25	506	13.97	11230	4.32

GENERIC PACKAGE VIEW

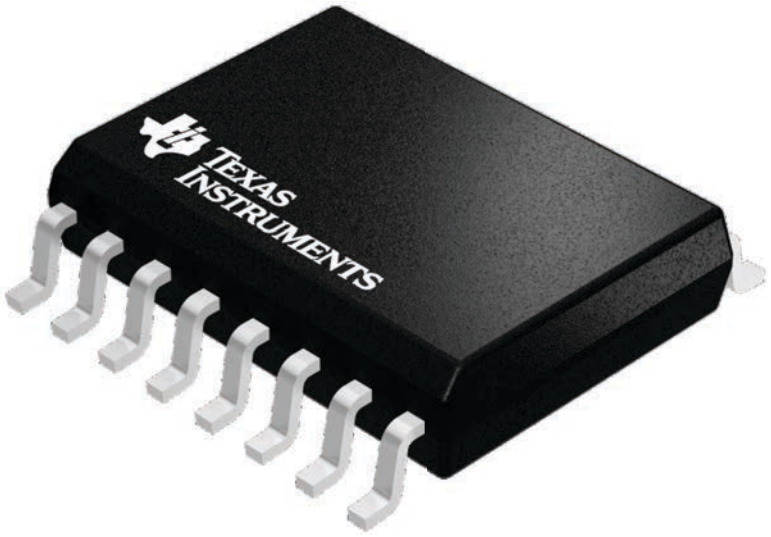
DW 16

SOIC - 2.65 mm max height

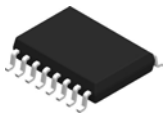
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

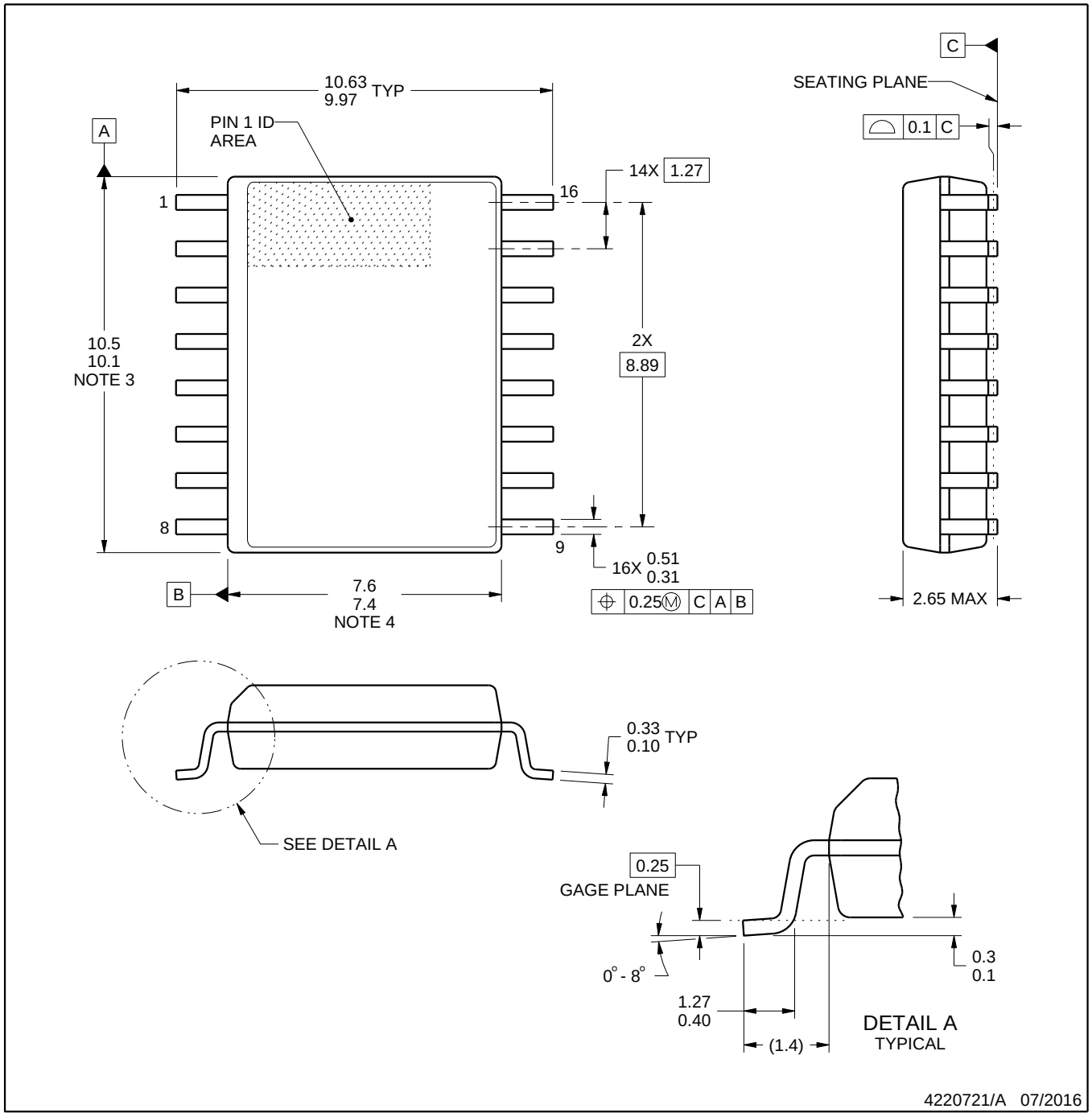


PACKAGE OUTLINE

DW0016A

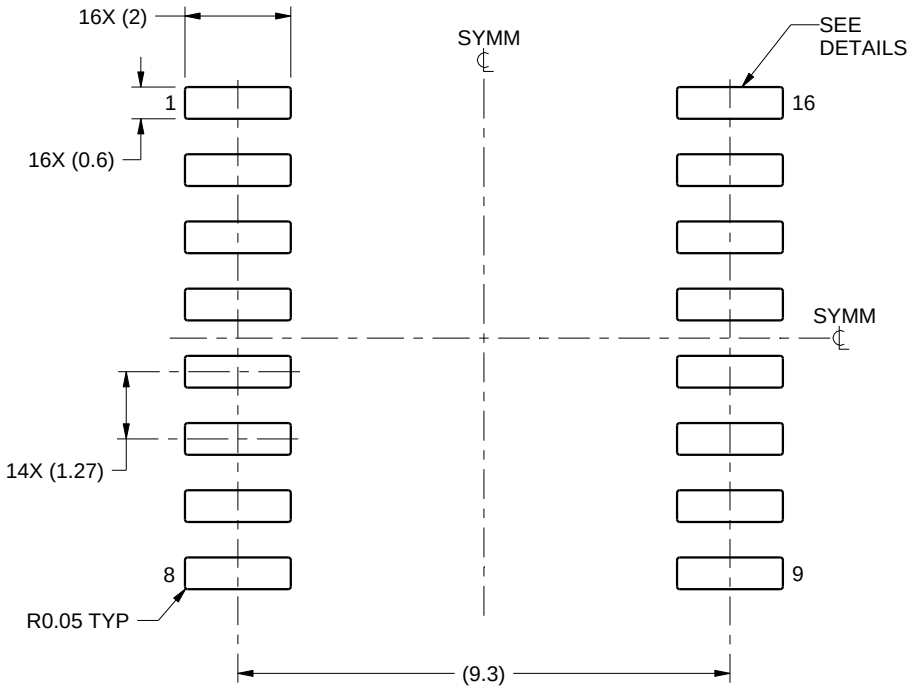
SOIC - 2.65 mm max height

SOIC

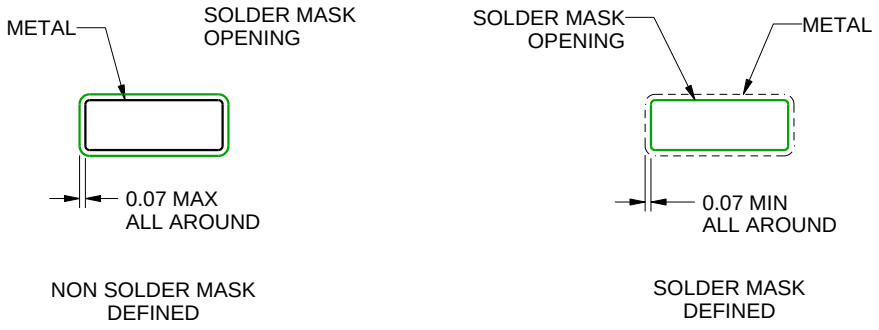


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

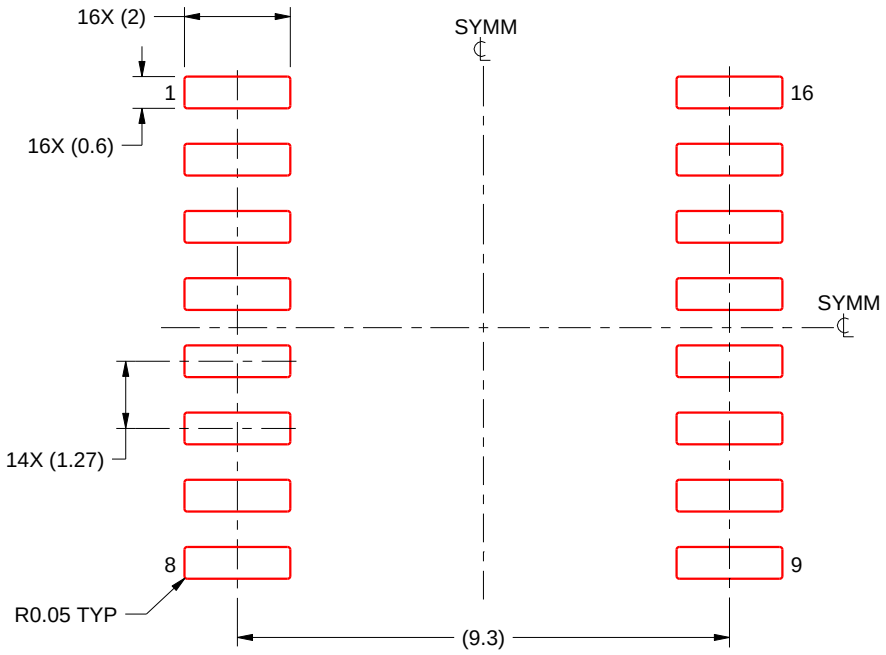


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

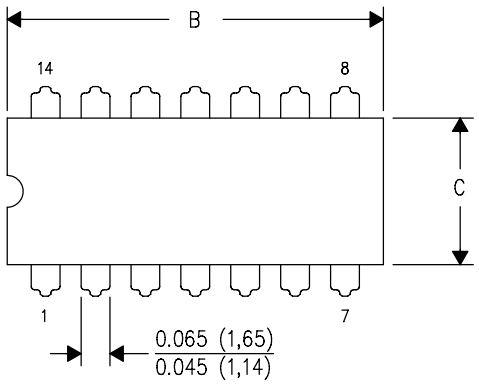
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

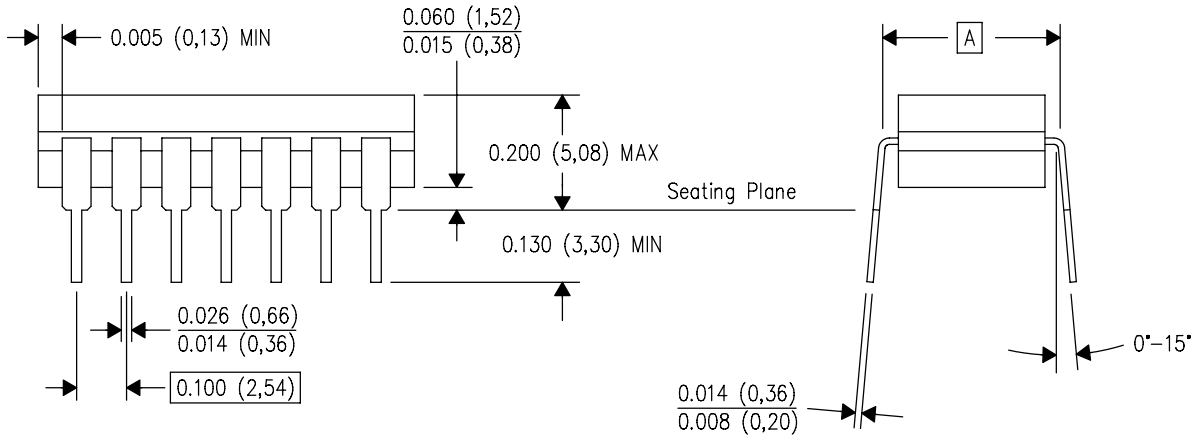
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



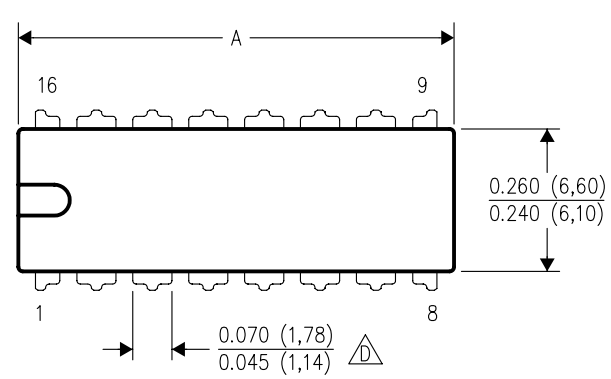
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

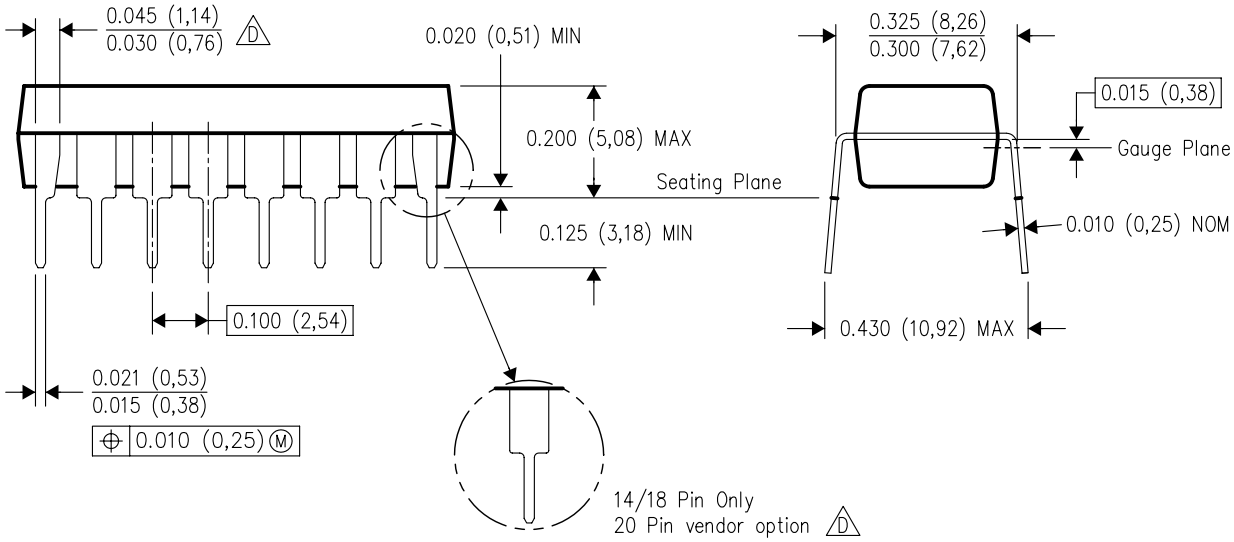
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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