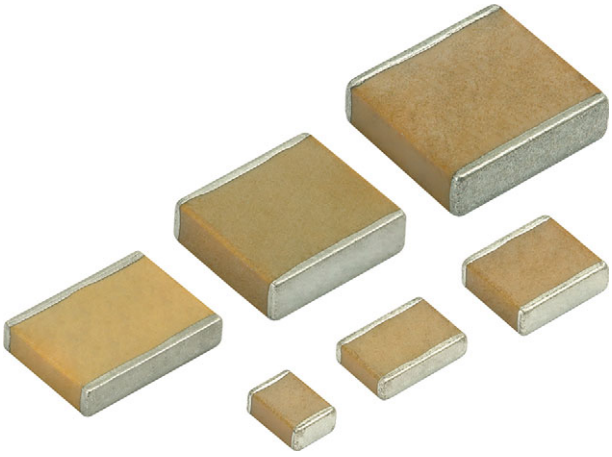
Surface Mount Multilayer Ceramic Capacitors for Pulse Current Applications



FEATURES

- Low electrostrictive ceramic formulation for repeated charge and discharge cycles
- High pulse discharge currents
- Excellent reliability and high voltage performance
- Available with tin / lead barrier termination (code “L”)
- Wet built process
- Reliable Noble Metal Electrode (NME) system
- Made with a combination of design, materials and tight process control to achieve very high field reliability
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Available

RoHS* Available

HALOGEN FREE

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

LINKS TO ADDITIONAL RESOURCES

Packages | Technical Notes | Related Documents

APPLICATIONS

- Power supplies
- Converters
- Voltage multipliers

ELECTRICAL SPECIFICATIONS

Note

- Electrical characteristics at +25 °C unless otherwise specified

Operating Temperature: -55 °C to +125 °C

Capacitance Range: 4.7 nF to 560 nF

Voltage Range: 1000 V_{DC}, 1500 V_{DC}

Temperature Coefficient of Capacitance (TCC):
X7R: ± 15 % from -55 °C to +125 °C, with 0 V_{DC} applied

Dissipation Factor (DF):
2.5 % max. at 1.0 V_{RMS} and 1 kHz

Aging Rate: 1 % maximum per decade

Insulation Resistance (IR):
at +25 °C and rated voltage: 100 000 MΩ minimum or 1000 ΩF, whichever is less
at +125 °C and rated voltage: 10 000 MΩ minimum or 100 ΩF, whichever is less

Dielectric Strength Test:
performed per method 103 of EIA 198-2-E.
Applied test voltages:
1000 V_{DC} / 1500 V_{DC}-rated: min. 120 % of rated voltage

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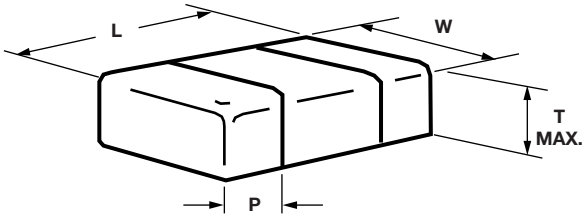
DIMENSIONS in inches [millimeters]



CASE CODE	PART ORDERING NUMBER	LENGTH (L)	WIDTH (W)	MAXIMUM THICKNESS (T)		TERMINATION (P)	
						MINIMUM	MAXIMUM
1812	VJ1812	0.177 ± 0.012 [4.50 ± 0.30]	0.126 ± 0.008 [3.20 ± 0.20]	0.086 [2.18]		0.010 [0.25]	0.035 [0.90]
1825	VJ1825	0.177 ± 0.012 [4.50 ± 0.30]	0.252 ± 0.010 [6.40 ± 0.25]	0.086 [2.18]		0.010 [0.25]	0.035 [0.90]
2225	VJ2225	0.220 ± 0.010 [5.59 ± 0.25]	0.250 ± 0.010 [6.35 ± 0.25]	0.086 [2.18]		0.010 [0.25]	0.037 [0.95]
3040	VJ3040	0.300 ± 0.015 [7.62 ± 0.38]	0.400 ± 0.015 [10.20 ± 0.38]	0.100 [2.54]		0.010 [0.25]	0.039 [1.00]
3640	VJ3640	0.360 ± 0.015 [9.14 ± 0.38]	0.400 ± 0.015 [10.20 ± 0.38]	0.120 [3.05]	0.130 (1) [3.30]	0.010 [0.25]	0.039 [1.00]
4044	VJ4044	0.400 ± 0.015 [10.16 ± 0.38]	0.440 ± 0.015 [11.17 ± 0.38]	0.120 [3.05]		0.020 [0.50]	0.040 [1.00]

Note

(1) Thickness used for 3640 - 1500 V - 220 nF and 270 nF

QUICK REFERENCE DATA

DIELECTRIC	CASE	MAXIMUM VOLTAGE (V)	CAPACITANCE	
			MINIMUM	MAXIMUM
X7R (X5P)	1812	1500	4.7 nF	27 nF
	1825	1500	10 nF	56 nF
	2225	1500	18 nF	100 nF
	3040	1500	33 nF	220 nF
	3640	1500	47 nF	330 nF
	4044	1500	100 nF	560 nF

Note

- Detail ratings see “Selection Chart”

ORDERING INFORMATION

VJ3640	Y	184	K	X	R	A	T	SE
CASE CODE	DIELECTRIC	CAPACITANCE NOMINAL CODE	CAPACITANCE TOLERANCE	TERMINATION	DC VOLTAGE RATING (1)	MARKING	PACKAGING (3)	PROCESS CODE (2)
1812 1825 2225 3040 3640 4044	Y = X7R	Expressed in picofarads (pF). The first two digits are significant, the third is a multiplier. **Examples:** 184 = 180 000 pF	J = ± 5 % K = ± 10 % M = ± 20 %	X = Ni barrier 100 % tin matte plated L = Ni barrier with tin lead plated finish min. 4 % lead	G = 1000 V R = 1500 V	A = unmarked	T = 7" reel / plastic tape J = 7" reel / plastic tape (low quantity)	

Notes

(1) DC voltage rating should not be exceeded in application
(2) Process code with 2 digits has to be added
(3) All types of packaging may not be available for all case sizes, see table end of this datasheet

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SELECTION CHART

DIELECTRIC		X7R											
STYLE		VJ1812 (1)		VJ1825 (1)		VJ2225 (1)		VJ3040 (1)		VJ3640 (1)		VJ4044 (1)	
CASE CODE		1812		1825		2225		3040		3640		4044	
VOLTAGE (V_{DC})		1000	1500	1000	1500	1000	1500	1000	1500	1000	1500	1000	1500
VOLTAGE CODE		G	R	G	R	G	R	G	R	G	R	G	R
CAP. CODE	CAP.												
332	3.3 nF												
392	3.9 nF												
472	4.7 nF		•										
562	5.6 nF		•										
682	6.8 nF	•	•										
822	8.2 nF	•	•										
103	10 nF	•	•		•								
123	12 nF	•	•		•								
153	15 nF	•	•	•	•								
183	18 nF	•	•	•	•		•						
223	22 nF	•		•	•		•						
273	27 nF	•		•	•	•	•						
333	33 nF			•	•	•	•		•				
393	39 nF			•	•	•	•		•				
473	47 nF			•		•	•		•		•		
563	56 nF			•		•	•	•	•		•		
683	68 nF					•	•	•	•		•		
823	82 nF					•		•	•		•		
104	100 nF					•		•	•	•	•		•
124	120 nF							•	•	•	•		•
154	150 nF							•		•	•	•	•
184	180 nF							•		•	•	•	•
224	220 nF							•		•	•	•	•
274	270 nF									•	•	•	•
334	330 nF									•		•	•
394	390 nF											•	
474	470 nF											•	
564	560 nF											•	
684	680 nF												
824	820 nF												
105	1000 nF												

Notes

RoHS-compliant except when supplied with lead (Pb)-containing termination, code “L”

• Plastic tape

(1) See soldering recommendations within this data book, or visit www.vishay.com/doc?45034

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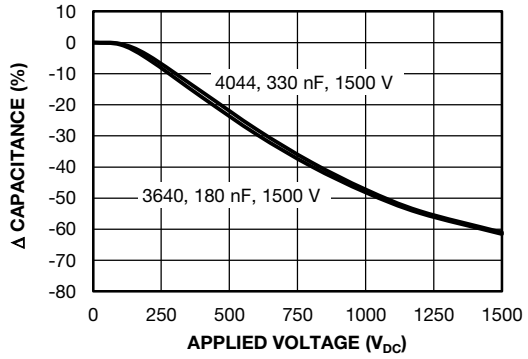
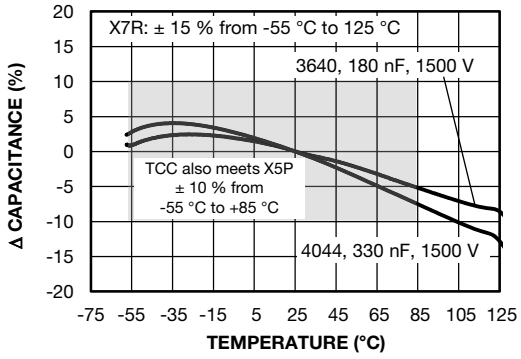
TYPICAL PARAMETERS

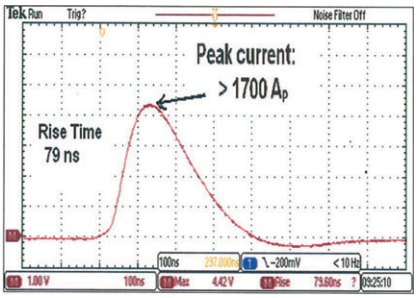
VOLTAGE COEFFICIENT OF CAPACITANCE



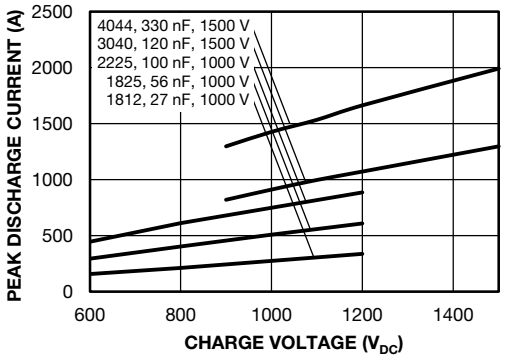
TEMPERATURE COEFFICIENT OF CAPACITANCE



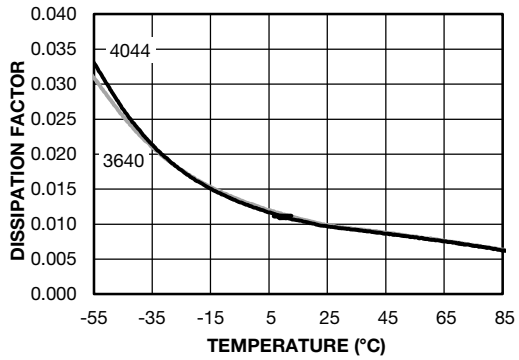
DISCHARGE PULSE OF 330 nF, 4044 SEC



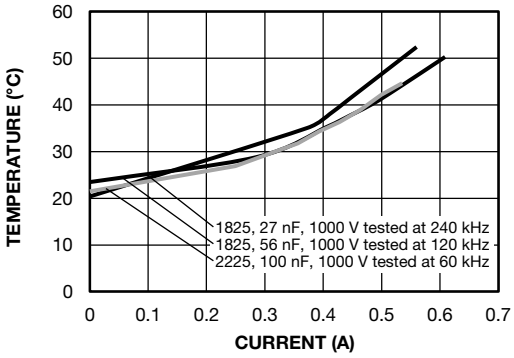
DISCHARGE CURRENT VS. CHARGE VOLTAGE



DISSIPATION FACTOR VS. TEMPERATURE



TEMPERATURE VS. RIPPLE CURRENT



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STANDARD PACKAGING QUANTITIES

CASE CODE	TAPE SIZE	7" REEL QUANTITIES	
		PLASTIC TAPE PACKAGING CODE "T"	LOW QUANTITY PACKAGING CODE "J"
1812	12 mm	1000	500
1825	12 mm	500	250
2225	12 mm	500	250
3040	16 mm	500	n/a
3640	16 mm	350	n/a
4044	24 mm	300	n/a

Notes

- Reference: EIA standard RS 481 - "Taping of Surface Mount Components for Automatic Placement"
- n/a = not available

STORAGE AND HANDLING CONDITIONS

(1) Store the components at 5 °C to 40 °C ambient temperature and ≤ 70 % relative humidity conditions.
(2) The product is recommended to be used within a time-frame of 2 years after shipment.
Check solderability in case extended shelf life beyond the expiry date is needed.

Precautions:

a. Do not store products in an environment containing corrosive elements, especially where chloride gas, sulfide gas, acid, alkali, salt or the like are present. This may cause corrosion or oxidization of the terminations, which can easily lead to poor soldering.
b. Store products on the shelf and avoid exposure to moisture or dust.
c. Do not expose products to excessive shock, vibration, direct sunlight and so on.

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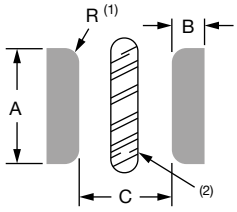
Solder Pad Dimensions for Vishay Surface-Mount Multilayer Ceramic Chip Capacitors

DIMENSIONS in millimeters



CASE CODE	A	B	C
0402	0.50	0.50	0.40
0505	1.35	1.00	0.60
0603	0.90	1.00	1.00 (3)
0805	1.30	1.20	1.00
1111	2.90	1.30	1.75
1206	1.80	1.20	2.10
1210	2.80	1.30	1.90
1808	2.40	1.50	3.00
1812	3.60	1.50	3.00
1825	6.50	1.50	3.00
2008	2.70	1.50	4.08
2220	5.50 (4)	1.50	4.20
2225	6.50	1.50	4.20
2525	6.60	1.50	4.50
3040	10.80	2.00	5.50
3640	10.80	2.00	7.00
3838	10.20	2.00	7.50
4044	12.30	2.00	8.00

Notes

(1) For safety capacitors and voltages above 3000 V, corner rounding (R) of 0.5 mm is recommended to suppress arcing
(2) Add a 1 mm slot in PCB between pads to allow cleaning and coating under MLCC
(3) For VJ HiFREQ Series, this dimension is 0.6 mm
(4) For safety capacitors, the A dimension should be 5.80 mm

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PRINTED CIRCUIT BOARD PCB DESIGN CONSIDERATIONS FOR HIGH VOLTAGE SURFACE-MOUNT MLCCS

Special assembly process and design considerations should be employed for today's high voltage rating MLCCs. As case sizes remain the same and voltage ratings increase, MLCC manufacturers must design, evaluate, and qualify their capacitors using methods that reduce the occurrence of corona discharge and arcover events. To meet similar capability in high voltage applications, users should employ similar cautionary design and assembly methods.

MLCC PAD LAYOUT

A capacitor's arcover inception point can degrade due to factors such as the MLCC termination, PCB pad design, PCB cleanliness, solder flux residue, surface contamination / deposits and environmental conditions. PCB pads and their design affect the air gap distance between the opposing polarities of the MLCC termination. For voltage rating greater than 1500 V_{DC} add a corner radius to the inward facing edge of the MLCC pads and as large a gap as possible between the pads. Too small of a pad gap distance will reduce the capacitor's own arcover inception voltage level. Refer to the Figure and Table Figure 1.0, MLCC Pad Layout and Table 1.0, Vishay MLCC Solder Pad Dimensions for the recommended MLCC solder pad dimensions.

SLOT OR TRENCH BETWEEN PADS

PCB assembly can deposit dust, trap solder balls, or flux residue underneath the capacitors. These contaminants will reduce conductive clearances and the arcover inception level. Assembly methods must include a final PCB cleaning process. A slot or trench can be cut into the PCB in between the pads to allow cleaners to penetrate underneath the MLCC. The slot will also allow conformal or epoxy coatings to flow underneath the MLCC and build an insulative barrier between pads. Refer to Figure 1.0 MLCC Pad Layout for slot reference location.

COATING PRINTED CIRCUIT BOARD

Coating a printed circuit board with materials such as acrylic, silicone and urethane resins provide a protective dielectric barrier that is non-conductive and will enhance the resistance to arcing. Various processes exist which include dipping, brushing, and spaying. Optimal performance will come from coating the MLCC on all sides, top and bottom. The PCB slot in between the pads should extend slightly beyond the width of the MLCC. Refer to Figure 1.0 MLCC Pad Layout for slot reference location.

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