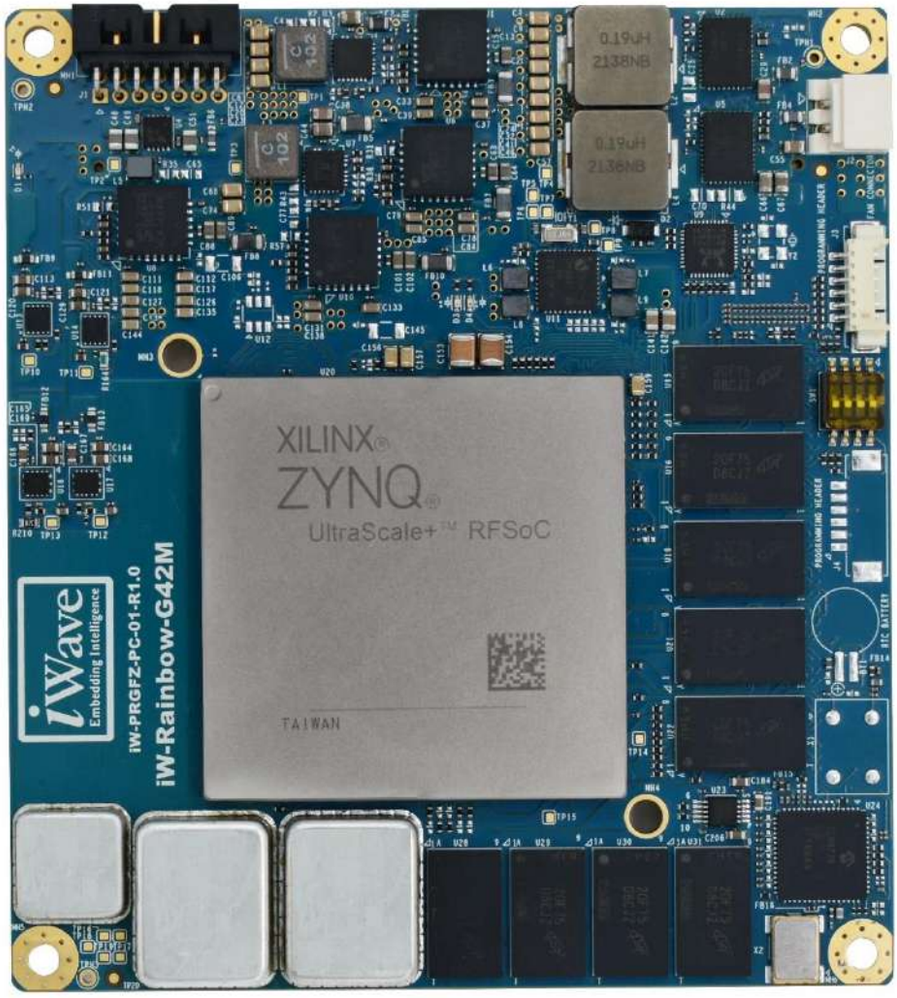
iW-RainboW-G42M
Zynq Ultrascale+ RFSoC (ZU29/39/49DR) SOM
Hardware User Guide



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1. INTRODUCTION

1.1 Purpose

This document is the Hardware User Guide for the Zynq Ultrascale+ RFSoC System on Module based on the Xilinx Zynq Ultrascale+ RFSoC (ZU49/39/29DR). This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the Zynq Ultrascale+ RFSoC System on Module from a Hardware Systems perspective.

1.2 SOM Overview

Zynq Ultrascale+ RFSoC SOM has a form factor of 100mm x 90mm and provides the functional requirements for an embedded application. Two high speed ruggedized terminal strip connectors and Two High-Speed High-Density connectors provide the carrier board interface to carry all the I/O signals to and from the Zynq Ultrascale+ RFSoC SOM.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 2: Acronyms & Abbreviations

Acronyms	Abbreviations
ADC	Analog to Digital Converter
ARM	Advanced RISC Machine
BSP	Board Support Package
CAN	Controller Area Network
CPU	Central Processing Unit
DAC	Digital to Analog converter
DDR4 SDRAM	Double Data Rate fourth-generation Synchronous Dynamic Random Access Memory
FPGA	Field Programmable Gate Array
eMMC	Embedded Multimedia Card
GB	Giga Byte
Gbps	Gigabits per sec
GEM	Gigabit Ethernet Controller
GHz	Giga Hertz
GPIO	General Purpose Input Output
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
JTAG	Joint Test Action Group
Kbps	Kilobits per second
LVDS	Low Voltage Differential Signalling
MAC	Media Access Controller
MB	Mega Byte
Mbps	Megabits per sec

Acronyms	Abbreviations
MHz	Mega Hertz
NPTH	Non-Plated Through hole
PCB	Printed Circuit Board
PMIC	Power Management Integrated Circuit
PTH	Plated Through hole
PL	Programmable Logic
PS	Processing System
RGMII	Reduced Gigabit Media Independent Interface
RTC	Real Time Clock
SD	Secure Digital
SDIO	Secure Digital Input Output
SGMII	Serial Gigabit Media Independent Interface
SoC	System On Chip
SOM	System On Module
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
ULPI	UTMI+ Low Pin Interface
USB	Universal Serial Bus
USB OTG	USB On The Go
UTMI	USB2.0 Transceiver Macrocell Interface

1.4 Terminlogy Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 3: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
LVDS	Low Voltage Differential Signal
DIFF	Differential Signal
GBE	Gigabit Ethernet Media Dependent Interface differential pair signals
USB	Universal Serial Bus differential pair signals
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-SOM.

1.5 References

- Zynq Ultrascale+ RFSoC Technical Reference Manual
- Zynq Ultrascale+ RFSoC Device Overview
- Zynq Ultrascale+ RFSoC AC and DAC characteristics

2. ARCHITECTURE AND DESIGN

This section provides detailed information about the Zynq Ultrascale+ RFSoC (ZU29/39/49DR) SOM features and Hardware architecture with high level block diagram. Also, this section provides detailed information about Board-to-Board connectors pin assignment and usage.

2.1 Zynq Ultrascale+ RFSoC (ZU29/39/49DR) SOM Block Diagram

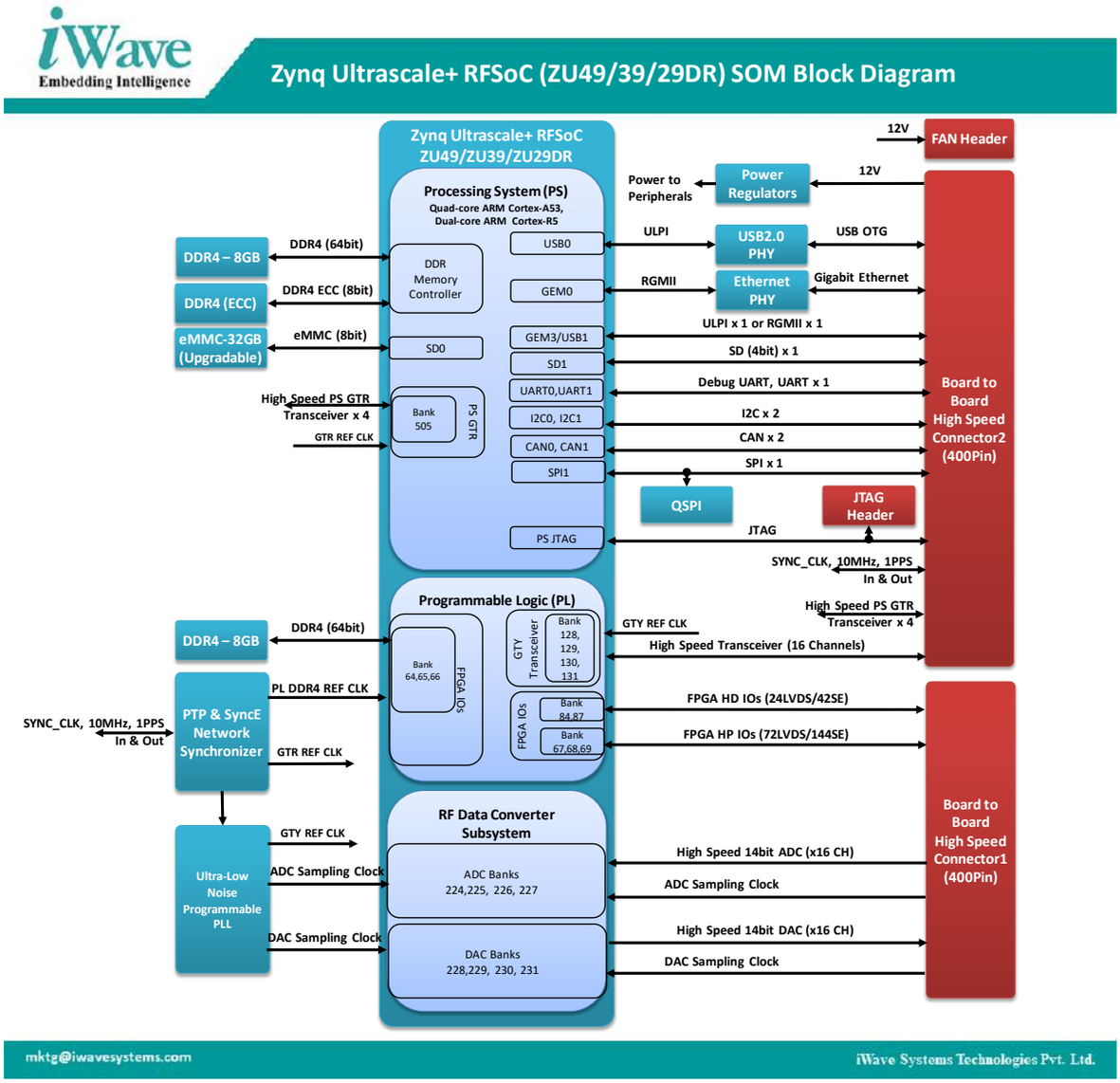


Figure 1: Zynq Ultrascale+ RFSoC SOM Block Diagram

2.2 Zynq Ultrascale+ RFSoC SOM Features

The Zynq Ultrascale+ RFSoC (ZU29/39/49DR) SOM supports the following features.

SoC

- Xilinx Zynq Ultrascale+ RFSoC
  - Compatible Zynq Ultrascale+ RFSoC Family (FFVF1760) – ZU49DR, ZU39DR, ZU29DR
    Programming Logic with up to 930K Logic cells with integrated RF-ADC & RF-DAC.
    Processing System with integrated Quad-core ARM Cortex-A53 MPCore Application processor (up to 1.3GHz), Dual-core ARM Cortex-R5 MPCore Real Time Processor (up to 533MHz).

PMIC

- Dialog's DA9062 PMIC with RTC

Memory

- 8GB DDR4 SDRAM (64bit) with ECC for PS.
- 8GB DDR4 SDRAM (64bit) for PL
- 256MB QSPI Flash
- 32GB eMMC Flash (Expandable)

Clock

- Integrated Ultra-low-noise programmable RF PLL
- Integrated SyncE & PTP Network Synchronization

Other On-SOM Features

- Gigabit Ethernet PHY
- USB2.0 Transceiver
- JTAG Header
- Fan Header

Board to Board Connector1 Interfaces (400pin)

From PL Block

- ADC Channels x16 up to 2.5Gsps
- DAC Channels x16 up to 10Gsps
- PL IOs – 192 IOs
  - HP Bank IOs – Upto 72LVDS/144SE [1]
  - HD Bank IOs – Upto 24LVDS/48SE [1]

Board to Board Connector2 Interfaces (400pin)

From PL Block

- PL-GTY High Speed Transceivers (upto 28.21Gbps) x 16
- Synchronous Clock In/Out
- 10MHz In/Out
- 1PPS In/Out

From PS Block

- PS-GTR High Speed Transceivers (upto 6Gbps) x 4
- Gigabit Ethernet x 1 Port (through On-SOM Gigabit Ethernet PHY transceiver)
- RGMII Interface or ULPI Interface x 1 [2]
- USB2.0 OTG x 1 Port (through On-SOM USB2.0 transceiver)
- SD (4bit) x 1 Port
- SPI/QSPI x 1 Port
- Debug UART x 1 Port
- Data UART x 1 Port
- I2C x 2 Ports
- PS JTAG

General Specification

- Power Supply : 12V (from Board-to-Board Connector2)
- Form Factor : 100mm x 90mm

[1] *In Zynq Ultrascale+ RFSoC SOM, PL HP BANK and PL HD BANK supports variable IO voltage setting which configurable through software.*

[2] *In Zynq Ultrascale+ RFSoC PS, GEM3 RGMII interface & USB1 ULPI interface signals are multiplexed in same pins and so either GEM3 or USB1 only can be supported.*

2.3 Zynq Ultrascale+ RFSoC

The Zynq Ultrascale+ RFSoC (ZU29/39/49DR) SOM is based on Xilinx Zynq Ultrascale+ RFSoC (ZU29/39/49DR) with FFVF1760 package. Zynq UltraScale+ RFSoC's integrate up to 16 channels of RF-ADCs and RF-DACs, all with excellent noise spectral density. The RF data converters also include power efficient digital down converters (DDCs) and digital up converters (DUCs) that include programmable interpolation and decimation, NCO, and complex mixer. Zynq Ultrascale+ RFSoC family integrates Processing system (PS) and Xilinx programmable logic (PL) in a single device. RFSoC's Processing system includes feature- 64-bit quad-core Arm® Cortex™-A53 and dual-core Arm Cortex-R5F based processing system.

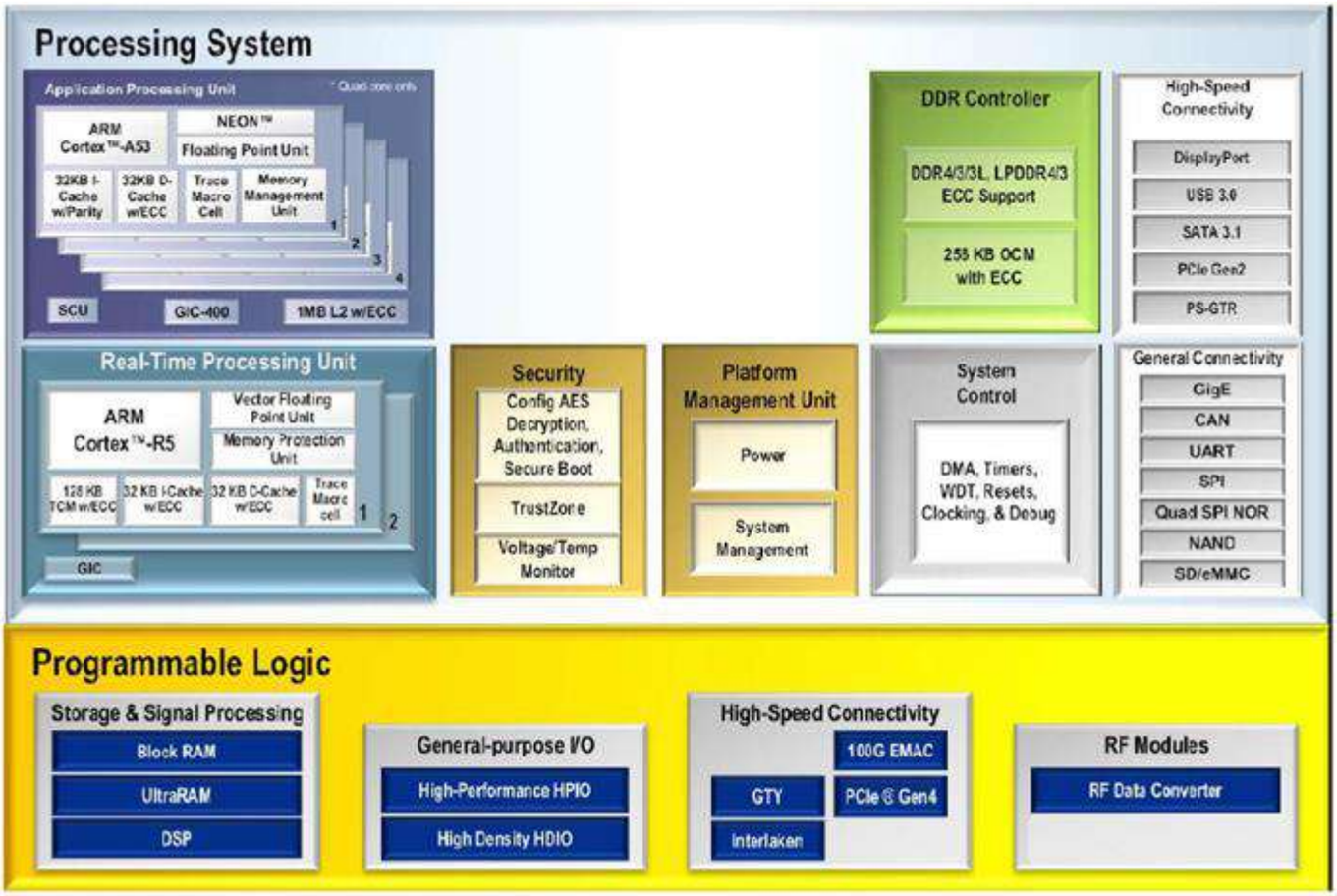


Figure 2: Zynq Ultrascale+ RFSoC CPU Simplified Block Diagram

Note: Please refer the latest Zynq Ultrascale+ RFSoC Datasheet & Technical Reference Manual for more details which may be revised from time to time.

The Zynq Ultrascale+ RFSoC SOM is compatible to ZU29DR, ZU39DR and ZU49DR RFSoC devices and feature comparison between these devices are shown below.

Features	ZU29DR (Gen 1)	ZU39DR (Gen 2)	ZU49DR (Gen 3)
12-bit RF-ADC /DDC(GSPS)	16(2.058)	16(2.220)	-
14-bit RF-ADC w/DDC(GSPS)	-	-	16(2.5)
14-bit RF-DAC w/DUC(GSPS)	16(6.554)	16(6.554)	16(10)
Number of DDCs per RF-ADC	1	1	1
RF input Freq max. GHz	4	5	6
Decimation / Interpolation	1x, 2x, 4x, 8x	1x, 2x, 4x, 8x	1x, 2x, 3x, 4x, 5x, 6x, 8x, 10x, 12x, 16x, 20x, 24x, 40x
Application Processor Core	Quad-core Arm® Cortex®-A53 MPCore™ up to 1.3GHz		
Real Time Processor Core	Dual-core Arm Cortex-R5F MPCore up to 533MHz		
High-Speed Connectivity	4 PS-GTR; PCIe® Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII		
System Logic Cells (K)	930	930	930
CLB LUTs (K)	425	425	425
Max. Dist. RAM (Mb)	13.0	13.0	13.0
Total Block RAM (Mb)	38.0	38.0	38.0
UltraRAM (Mb)	22.5	22.5	22.5
DSP Slices	4,272	4,272	4,272
GTY Transceivers	16	16	16
PCIe® Gen3 x16	2	2	-
PCIe® Gen4 x8	-	-	2
150G Interlaken	1	1	1
100G Ethernet MAC/PCS w/RS-FEC	2	2	2
System Monitor	2	2	2
F1760	Yes	Yes	Yes

The Zynq Ultrascale+ RFSoC's PS 16 ADC channels up to 2.5Gsps and 16 DAC Channels up to 10Gsps.PS has 78 dedicated I/O pins referred as MIO (Multiplexed I/O) for the PS peripheral interfaces. These 78 MIO pins are divided into three banks (PS BANK500, 501 & 502) and each bank includes 26 device pins. Since 78 MIO pins are not enough to support simultaneous use of all the peripherals supported by PS, there is option in RFSoC to route most of the IO peripheral interfaces to PL Bank I/O pins referred as EMIO (Extended MIO). Zynq Ultrascale+ RFSoC's PS Peripheral Pin mapping options between MIO & EMIO is shown below.

Peripheral Interface	MIO	EMIO
Quad-SPI	Yes	No
USB2.0: 0,1	Yes: External PHY	No
SDIO 0,1	Yes	Yes
SPI: 0,1	Yes	Yes
I2C: 0,1	Yes	Yes
CAN: 0,1	CAN: External PHY	CAN: External PHY
GPIO	GPIO: Up to 78 bits	GPIO: Up to 96 bits
GigE: 0,1,2,3	RGMII v2.0: External PHY	Supports GMII, RGMII v2.0 (HSTL), RGMII v1.3, MII, SGMII, and 1000BASE-X in Programmable Logic
UART: 0,1	Simple UART: Only two pins (TX and RX)	Full UART (TX, RX, DTR, DCD, DSR, RI, RTS, and CTS) requires either: • Two Processing System (PS) pins (RX and TX) through MIO and six additional Programmable Logic (PL) pins, or • Eight Programmable Logic (PL) pins
Debug Trace Ports	Yes: Up to 16 trace bits	Yes: Up to 32 trace bits
Processor JTAG	Yes	Yes

Zynq Ultrascale+ RFSoC's has 16 channels of RF-ADC's which is grouped among 4 ADC banks (Bank 224,225,226&227) and 16 channels of RF-DAC's which is grouped among 4 DAC Banks (Bank 228,229,230&231).

The Zynq Ultrascale+ RFSoC's PL Banks are classified as high-performance (HP) banks or high-density (HD) banks. The HP Bank I/Os are optimized for highest performance operation organized in banks of 52pins. The HD Bank I/Os are reduced-feature I/Os organized in banks of 24pins.

In Zynq Ultrascale+ RFSoC PL, each bank supports four global clock (GC or HDGC) input pin pairs. GC pins have direct access to the global clock buffers, MMCMs and PLLs of the same Bank. HDGC pins are from HD I/O banks and have direct access only to the global clock buffers.

Also, Zynq Ultrascale+ RFSoC supports three types of high-speed transceivers namely GTY and PS-GTR. These transceivers are arranged in groups of four known as a transceiver Quad. GTY transceivers are from PL and PS-GTR transceivers are from PS.

2.3.1 RFSoC Configuration & Status

The Zynq Ultrascale+ RFSoC uses multi-stage boot process that supports both a non-secure and a secure boot. The PS is the master of the boot and configuration process. Upon reset, device executes code out of on-chip ROM and copies the first stage boot loader (FSBL) from the boot device to the on-chip RAM. The FSBL initiates the boot of the PS and can load and configure the PL or configuration of the PL can be deferred to a later stage.

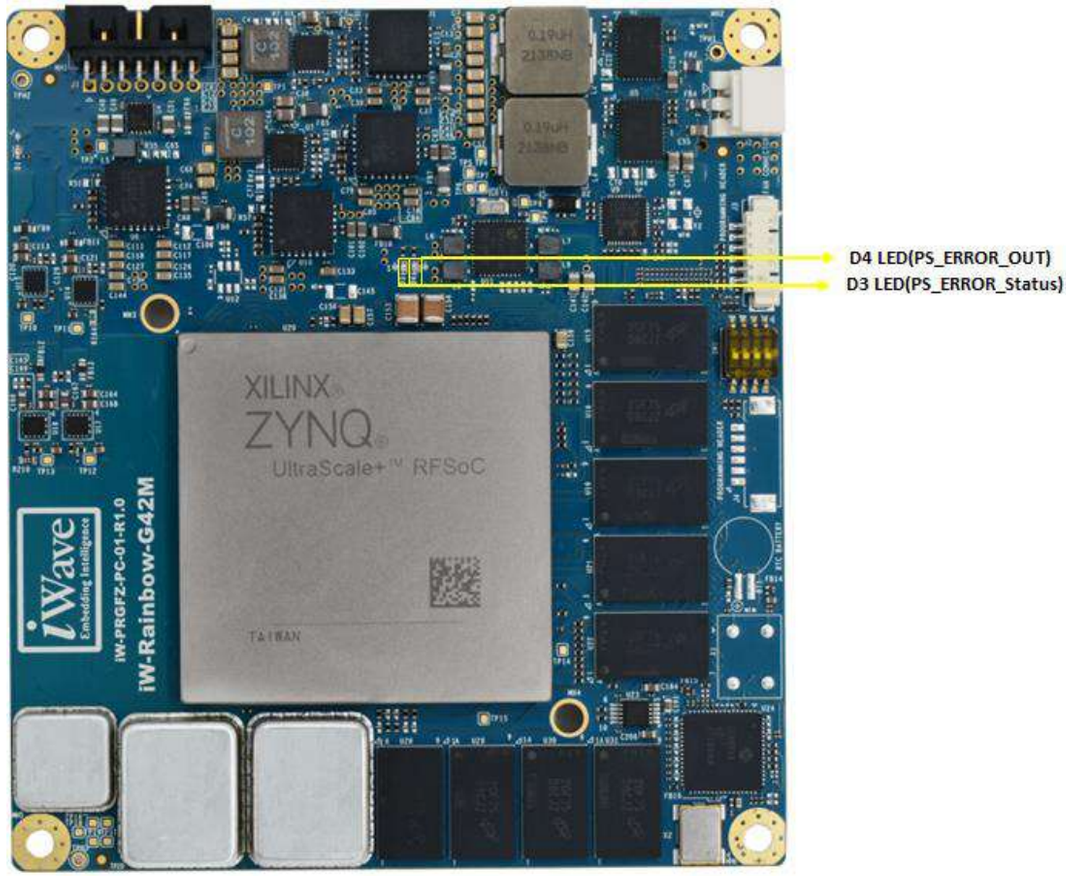


Figure 3: Error Status Indication LEDs

The Zynq Ultrascale+ RFSoC SOM supports two LEDs for the RFSoC error status indication namely PS_ERROR_OUT and PS_ERROR_STATUS. LED D4 is for PS_ERROR_OUT and it is asserted for accidental loss of power, a hardware error, or an exception in the PMU. LED D3 is for PS_ERROR_STATUS and it indicates a secure lockdown state. Alternatively, it can be used by the PMU firmware to indicate system status.

The Zynq Ultrascale+ RFSoC SOM supports three dedicated input and output configuration pins. By default, PUDC_B pin is connected to 1.8V(Weak pre configuration I/O pull-up resistors disabled), POR_OVERRIDE pin is connected to the Ground(Standard PL power-on delay time)and PS-Done pin is connected to 1V8 and the same signal connected to the B15th pin of the Board-to-Board connector2.

2.3.2 RFSoC Boot Mode Switch

The Zynq Ultrascale+ RFSoC always boots from PS first and configures the PL through software. RFSoC can support QSPI, eMMC, SD1, USB0 & JTAG as boot device and configurable through mode pins. Upon device reset, RFSoC mode pins are read to determine the primary boot device.

The Zynq Ultrascale+ RFSoC SOM supports Boot Mode switch (SW1) to select the required boot device. By default, QSPI is supported as boot device. Refer the below table to select the required boot device. Also the same signals are connected to C13, C14 and C15 pins of the board to board connector2 to control the boot mode from the carrier board.

Table 4: Boot Mode Switch Truth Table

Zynq Ultrascale+ RFSoC Boot Mode	SW1 (4 Position Switch)				
	PS Mode 3	PS Mode 2	PS Mode 1	PS Mode 0	Switch Position Image
PS JTAG	OFF	OFF	OFF	OFF	
SD1	OFF	ON	OFF	ON	
eMMC	OFF	ON	ON	OFF	
USB0	OFF	ON	ON	ON	
QSPI (Default)	OFF	OFF	ON	OFF	

2.3.3 RFSoC Power

The Zynq Ultrascale+ RFSoC SOM uses discrete power regulators along with DA9062 PMIC from Dialog Semiconductor for RFSoC power management. It also has low-noise regulators specifically for ADC and DAC. In SOM, PS low-power domain, PS full-power domain & PL power domain supply voltage (VCC_PSINTLP, VCC_PSINTFP) is fixed to 0.85V .Also all PS Bank (VCCO_PSIO) I/O voltage is fixed to 1.8V.ADC domain supply voltage (VADC_AVCC) is fixed to 0.925V and VADC_AVCCAUX is fixed to 1.8V.DAC domain supply voltage VDAC_AVCC is fixed to 0.925V and VDAC_AVCCAUX is fixed to 1.8V.

The I/O voltage of PL HP Banks (PL Bank 67,68 & 69) and PL HD Banks (PL Bank 84 & 87) which are connected to Board-to-Board Connectors are generated from PMIC LDO1 and LDO4 respectively. By default, HP Banks voltages are set to 1.0V & HD Banks voltages are set to 1.2V and configurable through software after bootup.

2.3.4 RFSoC Reset

The Zynq Ultrascale+ RFSoC SOM uses PMIC's Reset output (nRESET) for PS Power On Reset and connected to PS_POR_B pin of RFSoC. Also, it supports warm reset input from Board-to-Board Connector2 pinB14 and connected to PS_SRST_B pin of RFSoC.

2.3.5 RFSoC System Monitor/Low speed ADC

The Zynq Ultrascale+ RFSoC contain two System Monitor block (SYSMONE4), one in the PL (PL SYSMON) and another in the PS (PS SYSMON). It is used to enhance the overall safety, security and reliability of the system by monitoring the physical environment via on-chip power supply and temperature sensors.

The PL SYSMON uses 10-bit 200kSPS ADC to digitize the sensor/ADC inputs. It monitors the die temperature in the PL and several internal PL and PS power supply nodes. The PL SYSMON can also monitor up to 17 external analog channels which includes 16 auxiliary analog inputs and one VP_VN dedicated input. The external auxiliary inputs can be routed through any PL Bank. The ADC voltage reference is selectable between an internal reference and the external pins VREFP and VREFN. In Zynq Ultrascale+ RFSoC SOM, 1.25V external voltage reference is supported.

The PS SYSMON uses 10-bit 1MSPS ADC to digitize the sensor inputs. It is located in the PS LPD and monitors two temperature points & several internal fixed voltage nodes. The PS has two temperature sensors, one is physically located in the PS SYSMON near the RPU. The second, remote sensor is located in the FPD near the APU. The ADC always uses an internally generated voltage reference.

2.4 Clock Design

2.4.1 Clock Synthesizer with Integrated SyncE & PTP

The Zynq Ultrascale + RFSoC SOM supports on-Board Clock Synthesizer "ZL30733LDG1" from Microchip with Integrated SyncE & PTP support. This clock synthesizer acts as primary clock source for whole SOM including RFSoC & other peripheral to make the system completely synchronised. It also supports difference reference clock inputs including high precision OCXO.

Table 5: Clock Synthesizer Input & Output

Sl. No	Clock Synthesizer In/Out	Frequency	RFSoC Pin Name/ Net Name	RFSoC Pin No	Signal Type/ Termination	Description
Input Reference Clock Options to Clock Synthesizer						
1	REF0P/ REF0N	Configurable	SYS_SYNC_CLK_IN	NA	1.8V, LVDS	External clock input from B2B2
2	REF2P	10MHz	10MHz_EX_IN	NA	1.8V, LVCMOS	External 10MHz input from B2B2
3	REF3P	1Hz	1PPS_EX_IN	NA	1.8V, LVCMOS	External 1PPS input from B2B2
4	REF4N	20MHz	OCXO_CLK20M	NA	3.3V, LVCMOS	20MHz high precision OCXO input
5	OSCB	114.285MHz (Default)	XO_114_285MHZ	NA	3.3V, LVCMOS	114.285MHz high precision OCXO input.
Output Clock from Clock Synthesizer						
1	OUT0P	25MHz	GEM0_REFCLK	NA	1.8V, LVCMOS	Ethernet PHY reference clock. *Optionally connected to the B41 and B42 pins of board-to-board connector2 through AC caps.*
2	OUT1P	10MHz	10MHz_EX_OUT	NA	1.8V, LVCMOS	10MHz clock output to B2B2
3	OUT1N	1Hz	1PPS_EX_OUT	NA	1.8V, LVCMOS	1PPS clock output to B2B2
4	OUT2P	100MHz	IO_L5P_HDGC_88	L15	1.8V, LVCMOS	Reference clock to PL Bank 88
5	OUT3P/ OUT3N	266.525MHz	IO_L13P_T2L_N0_GC_QBC_64 IO_L13N_T2L_N1_GC_QBC_64,	AU17 AU16,	1.8V, LVDS	Reference clock to PL DDR SDRAM
6	OUT4P/ OUT4N	27MHz	PS_MGTREFCLK2P_505 PS_MGTREFCLK2N_505	AC36, AC37	1.8V, LVDS	Reference clock for GTR2 Bank 505
7	OUT5P/N	12.8MHz	LMK_CLK_IN_P/N	NA	O, LVDS	LMK04828B PLL input
8	OUT6P/ OUT6N	156.25MHz	MGTREFCLK1P_128, MGTREFCLK1N_128	Y34, Y35	1.8V, LVDS	Reference clock1 for GTY Bank 128
9	OUT7P/ OUT7N	156.25MHz	MGTREFCLK1P_129, MGTREFCLK1N_129	T34, T35	1.8V, LVDS	Reference clock1 for GTY Bank 129
10	OUT8P/ OUT8N	156.25MHz	MGTREFCLK1P_130, MGTREFCLK1N_130	M34, M35	1.8V, LVDS	Reference clock1 for GTY Bank 130
11	OUT9P/ OUT9N	156.25MHz	MGTREFCLK1P_131, MGTREFCLK1N_131	H34, H35	1.8V, LVDS	Reference clock1 for GTY Bank 131

2.4.2 Ultra-low-noise RF PLL & Wideband RF Synthesizer with JESD204B Support

The Zynq Ultrascale+ RFSoC SOM integrates fully configurable JESD204B Compliant RF PLL circuit on board to support wide variety of applications. It supports Wideband ultra-low-noise JESD204B Compliant Clock Jitter cleaner LMK04828 and RF Synthesizer "LMX2594" from Texas Instruments. These signals This provides reference clocks to ADC Bank 225, and DAC Bank 229.

The LMK04828B clock synthesizer and LMX2594 RF-PLL SPI signals are connected to PL HD Bank89 through EMIO. This PL HD-Bank89 IO level is fixed to 3.3V in SOM.

The external 122.88MHz TXCO provides frequency-accurate, low-phase noise reference clock for the LMK04828B. It operates with a wide-loop bandwidth and generates the input references and SYNC signal for the ADC/DAC RF PLLs, the PLL reference clocks, the SYSREF signal for the RFSoC ADC/DAC, the reference clocks for the RFSoC PL banks, and the output reference clock for multi-tile and multi-board synchronization.

Note: For more details and frequency planning on RF PLL, contact iWave

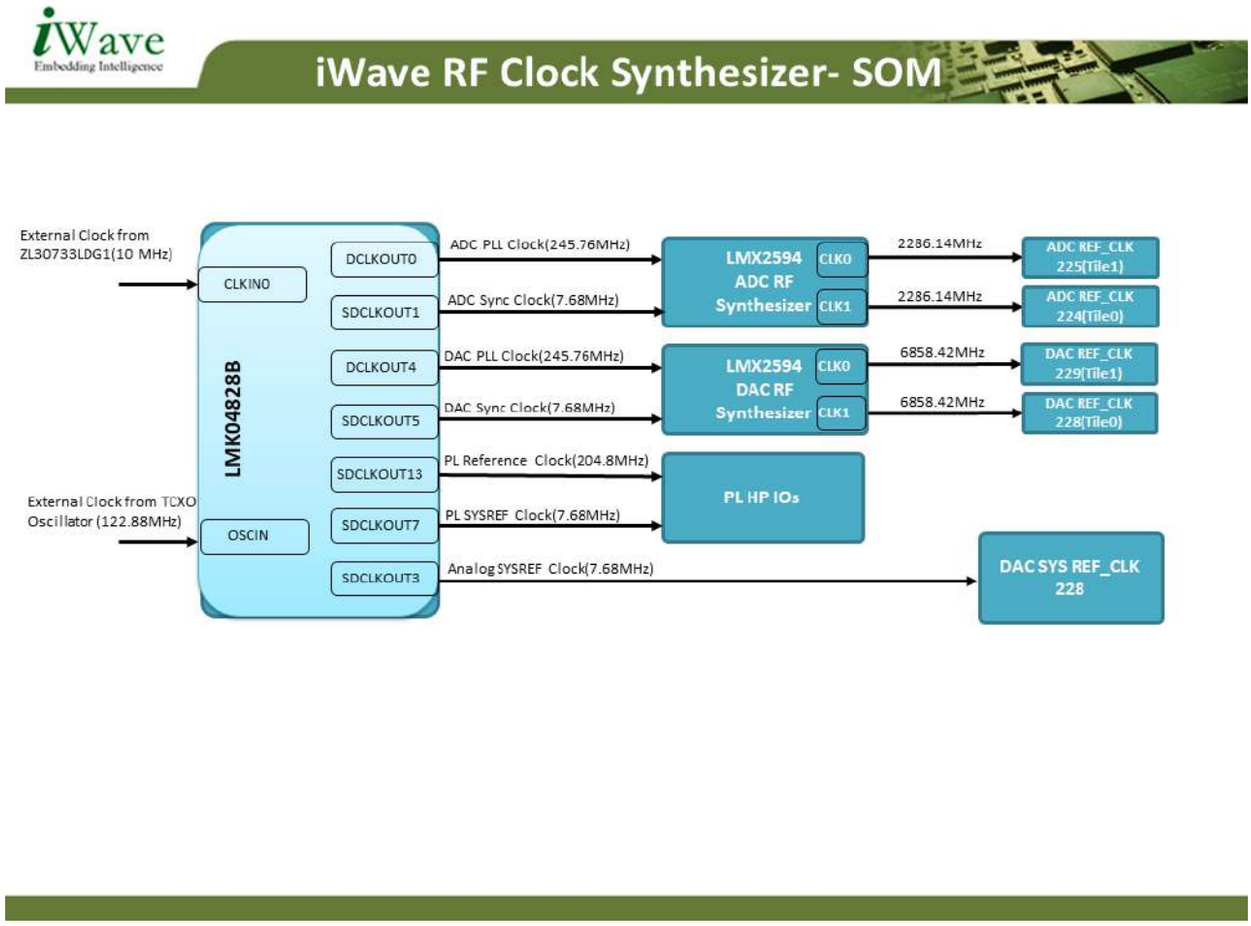


Figure 4: RFPLL Clock Distribution

Table 6: LMK04828B Clock Synthesizer Input & Output

Sl. No	Clock Synthesizer In/Out	Frequency	RFSoC Pin Name/ Net Name	RFSoC Pin No	Signal Type/ Termination	Description
Input Reference Clock Options to Clock Synthesizer						
1	CLKIN0_P CLKIN0_N	10 MHz	LMK_CLK_IN_P/ LMK_CLK_IN_N	NA	I, LVDS	External clock input from ZL30733LDG1.
2	OSCIN_P	122.88 MHz (Default)	OSCIN_P	NA	3.3V, LVCMOS	122.88 MHz high precision TCXO input.
Output Clock from Clock Synthesizer						
1	DCLKOUT0_P DCLKOUT0_N	245.76 MHz	RF_ADC_PLL_P RF_ADC_PLL_N	NA	O, LVDS	ADC PLL clock to LMX259 RF Synthesizer.
2	SDCLKOUT1_P	7.68 MHz	RF_ADC_PLL_SYNC	NA	3.3V, LVCMOS	ADC Sync clock to LMX259 RF Synthesizer
3	DCLKOUT4_P DCLKOUT4_N	245.76 MHz	RF_DAC_PLL_P RF_DAC_PLL_N	NA	O, LVDS	DAC PLL clock to LMX259 RF Synthesizer.
4	SDCLKOUT5_P	7.68 MHz	RF_DAC_PLL_SYNC	NA	3.3V, LVCMOS	DAC Sync clock to LMX259 RF Synthesizer
5	SDCLKOUT13_P SDCLKOUT13_N	204.8 MHz	PL_H20_LVDS69_L13P_GC PL_G20_LVDS69_L13N_GC	H20, G20	O, LVDS	PL Reference clock
6	SDCLKOUT7_P SDCLKOUT7_N	7.68 MHz	PL_F19_LVDS69_L14P_GC PL_F18_LVDS69_L14N_GC	F19, F18	O, LVDS	PL SYSREF Clock.
7	SDCLKOUT3_P SDCLKOUT3_N	7.68 MHz	SYSREF_DAC_P_228 SYSREF_DAC_N_228	D2 D1	O, LVDS	Analog SYSREF Clock.

Table 7: LMX259 ADC Clock Synthesizer Input & Output

Sl. No	Clock Synthesizer In/Out	Frequency	RFSoC Pin Name/ Net Name	RFSoC Pin No	Signal Type/ Termination	Description
Input Reference Clock Options to Clock Synthesizer						
1	OSCIN_P OSCIN_M	245.76 MHz	RF_ADC_PLL_P RF_ADC_PLL_N	NA	I, LVDS	External clock input from LMK04828B.
Output Clock from Clock Synthesizer						
2	RF_OUTA_P RF_OUTA_M	6858.42 MHz	ADC_REF_CLK_P_225 ADC_REF_CLK_N_225	AW4 AY4	O, LVDS	ADC Reference clock for Bank 225 and 224
3	RF_OUTB_P RF_OUTB_M	6858.42 MHz	ADC_REF_CLK_P_224 ADC_REF_CLK_N_224	BA3 BB3	O, LVDS	ADC Reference clock for Bank 224

Table 8: LMX259 ADC Clock Synthesizer Input & Output

Sl. No	Clock Synthesizer In/Out	Frequency	RFSoC Pin Name/ Net Name	RFSoC Pin No	Signal Type/ Termination	Description
Input Reference Clock Options to Clock Synthesizer						
1	OSCIN_P OSCIN_M	245.76 MHz	RF_DAC_PLL_P RF_DAC_PLL_N	NA	I, LVDS	External clock input from LMK04828B.
Output Clock from Clock Synthesizer						
2	RF_OUTA_P RF_OUTA_M	2286.14 MHz	DAC_REF_CLK_P_229 DAC_REF_CLK_N_229	D4 C4	O, LVDS	DAC Reference clock for Bank 229
3	RF_OUTB_P RF_OUTB_M	2286.14 MHz	DAC_REF_CLK_P_228 DAC_REF_CLK_N_228	B3 A3	O, LVDS	DAC Reference clock for Bank 228

2.5 PMIC with RTC

The Zynq Ultrascale+ RFSoC SOM supports Dialog semiconductor DA9062 PMIC. The I2C0 module of Zynq Ultrascale+ RFSoC PS is used for PMIC interface through MIO pins with I2C address 0x58 and 0X59.

PMIC's LDO1 is connected to I/O voltage of PL HP Banks (PL Bank 67 ,68 & 69). The I/O voltage is configured to 1V by PMIC's internal OTP during powerup. The I/O voltage is configurable through software from 1V to 1.8V after bootup.

PMIC's LDO4 is connected to I/O voltage of PL HD Banks (PL Bank 84, 87 & 88) and by default set to 1.8V.). The I/O voltage is configured to 1.2V by PMIC's internal OTP during powerup. The I/O voltage is configurable through software from 1.2V to 3.3V after bootup.

PMIC supports reset output and connected to Zynq Ultrascale+ RFSoC PS (PS_POR_B) for power on reset.

The PMIC supports Real Time Clock functionality. It uses the Coin cell battery power from Board-to-Board Connector2 pinC12 for RTC backup power. The PMIC can support backup battery charging to charge Lithium-Manganese coin cell batteries and super capacitors if required.

Important Note: Every Power Off and On, The DA9062 PMIC work as initial OTP Setting

2.6 Memory

2.6.1 DDR4 SDRAM with ECC for PS

The Zynq Ultrascale+ RFSoC SOM supports 64bit, 8GB DDR4 RAM memory for RFSoC's PS. Four 16 bit, 2GB DDR4 SDRAM ICs are used to support a total on board RAM memory of 8GB. Also, Zynq Ultrascale+ RFSoC SOM supports 8bit ECC for RAM memory. These DDR4 devices operates at 2400Mbps data rate. DDR4 memory is connected to the hard memory controller of the RFSoC PS.

*Note: Refer **ORDERING INFORMATION** section for exact RAM size used on the SOM based on the Product Part Number.*

2.6.2 DDR4 SDRAM for PL

The Zynq Ultrascale+ RFSoC SOM supports 64bit, 8GB DDR4 RAM memory for RFSoC's PL. Four 16 bit, 2GB DDR4 SDRAM IC is used to support RAM memory of 8GB for PL. These DDR4 devices operates at 2400Mbps data rate. In Zynq Ultrascale+ RFSoC SOM, Bank64, 65 & 66 is used for PL DDR4 interface.

The Zynq Ultrascale+ RFSoC SOM supports 266.525MHz LVDS Oscillator on board for PL DDR4 reference clock and connected to Bank64 AU17 & AU16 dedicated clock input pins through AC Coupling capacitors.

*Note: Refer **ORDERING INFORMATION** section for exact RAM size used on the SOM based on the Product Part Number.*

2.6.3 eMMC Flash

The Zynq Ultrascale+ RFSoC SOM supports 8GB eMMC Flash memory for Boot & Storage of Zynq Ultrascale+ RFSoC PS. This eMMC Flash memory is directly connected to the SD0 controller of the RFSOC's PS through MIO pins and operates at 1.8V Voltage level. This SD/SDIO controller supports eMMC4.51 standard with up to 8bit HS200 mode. The eMMC Flash size can be expandable based on the availability of higher density eMMC Flash device.

*Note: Refer **ORDERING INFORMATION** section for exact eMMC Flash size used on the SOM based on the Product Part Number.*

2.6.4 QSPI Flash

The Zynq Ultrascale+ RFSoC SOM supports one on board 256MB QSPI and optionally connected to Board-to-Board Connector2 through resistors. The QSPI controller of RFSoC's PS is used for QSPI interface through MIO pins at 1.8V Voltage level. The SOM supports 4-bit QSPI Flash. Also, the same signals are optionally connected to Board-to-Board connector through resistors. By default these resistors are not populated in SOM. Also, mode bit is configured to "0010" for QSPI Flash as configuration device.

2.7 On SOM Fearures

2.7.1 JTAG Header

The Zynq Ultrascale+ RFSoC SOM supports 14Pin JTAG Header (J1) for JTAG interface. JTAG Interface Signals from RFSoC's PS BANK503 is daisy chained and connected to this Header. The Zynq Ultrascale+ RFSoC's PS and PL share a common set of JTAG pins and each have their own TAP controller which are chained together inside the Zynq Ultrascale RFSoC. These JTAG interface signals are at 1.8V Voltage level.

The JTAG Header (J1) is physically located on topside of the SOM as shown below. JTAG-HS2 Programming Cable can be directly connected to this JTAG Header. JTAG interface signals are also connected to Board-to-Board Connector2 to access from carrier board.

Number of Pins - 14
Connector Part - 877601416 from Molex
Mating Connector - 0791077006 from Molex

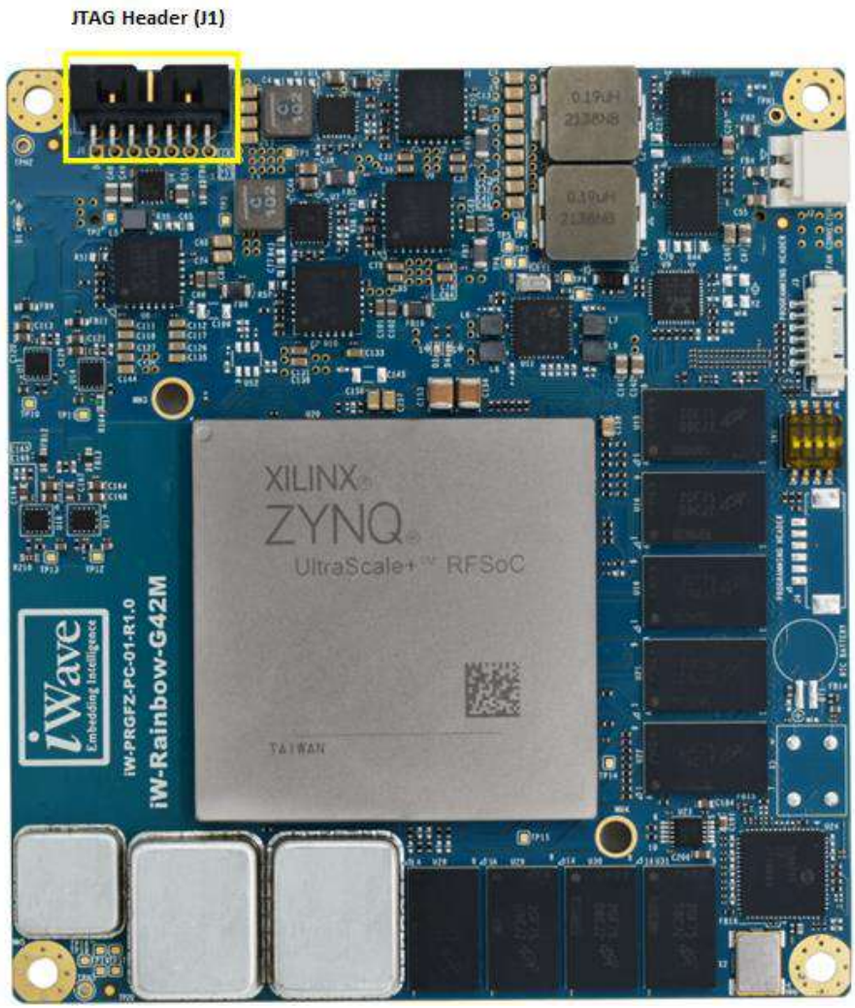


Figure 5: JTAG Header

Table 9: JTAG Header Pinout

Pin No	Signal Name	Signal Type/ Termination	Description
1	-	-	NC.
2	VCC_1V8	O, 1.8V Power	Supply Voltage.
3	GND	Power	Ground.
4	JTAG_TMS	I, 1.8V LVCMOS/ 4.7K PU	JTAG Test Mode Select.
5	GND	Power	Ground.
6	JTAG_TCK	I, 1.8V LVCMOS/ 4.7K PU	JTAG Test Clock.
7	GND	Power	Ground.
8	JTAG_TDO	O, 1.8V LVCMOS	JTAG Test Data Output.
9	GND	Power	Ground.
10	JTAG_TDI	I, 1.8V LVCMOS/ 4.7K PU	JTAG Test Data Input.
11	GND	Power	Ground.
12	-	-	NC.
13	GND	Power	Ground.
14	-	-	NC.

2.7.2 Fan Header

The Zynq Ultrascale+ RFSoC SOM supports a Fan Header (J2) to connect cooling Fan if required. The Fan Header (J2) is physically located on topside of the SOM as shown below.

Number of Pins - 2

Connector Part - 52125-02-0200-01 from Molex

Mating Connector - 51021-0200 from Molex

Compatible Fan (Example) - AFB0505MB from Delta Electronics

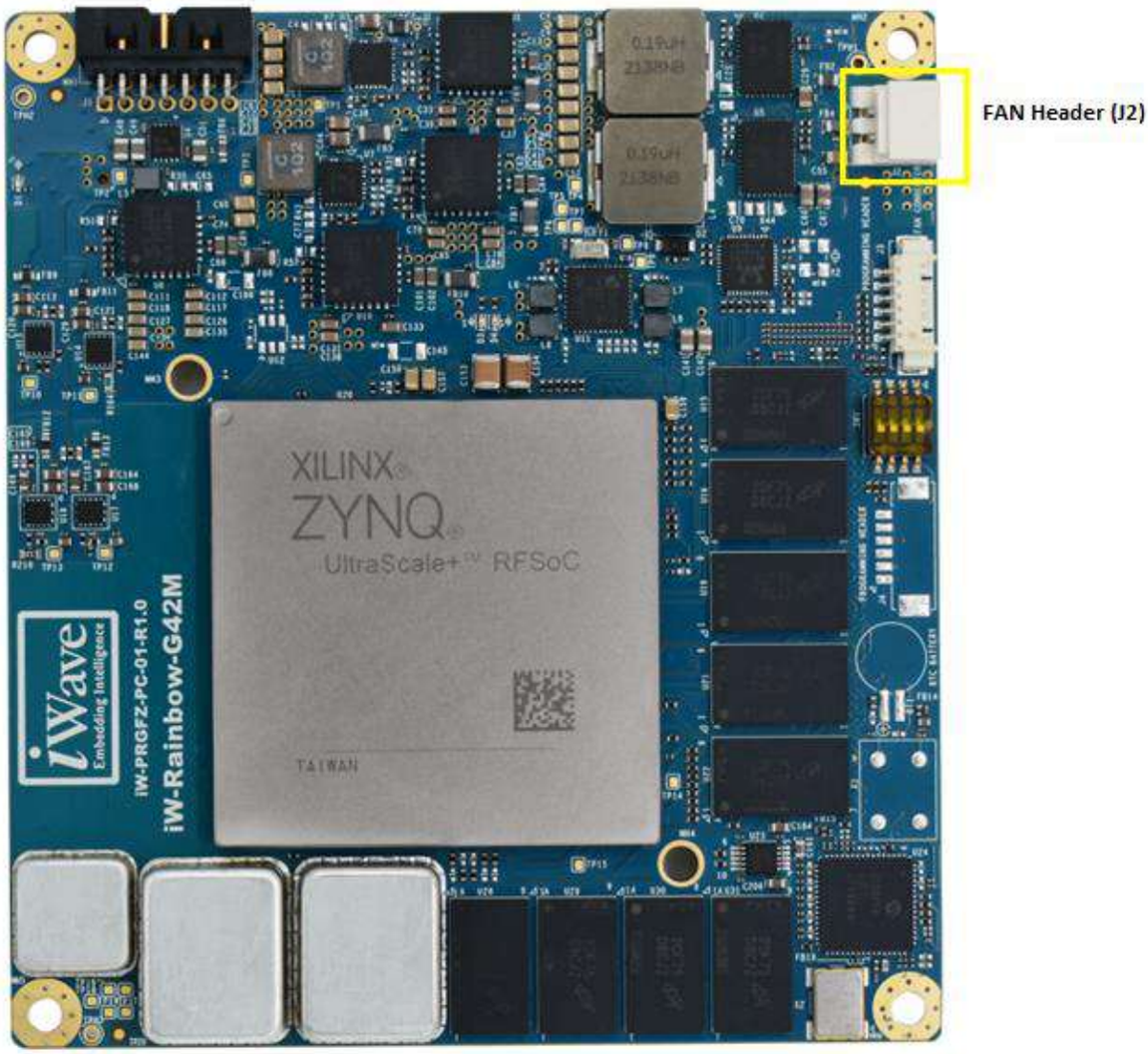


Figure 6: Fan Header

Table 10: Fan Header Pinout

Pin No	Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination	Description
1	VCC_12V	-	-	-	O, 12V Power	Supply Voltage.
2	GND	-	-	-	Power	Ground.

2.8 Board to Board Connector1

The Zynq Ultrascale+ RFSoC SOM supports two 400 pin high speed ruggedized terminal strip connectors for interfaces expansion. All the effort is made in Zynq Ultrascale+ RFSoC SOM design to provide the maximum interfaces of Zynq Ultrascale+ RFSoC to the carrier board by adding these two Board to Board Connectors.

The Zynq Ultrascale+ RFSoC SOM Board to Board Connector1 pinout is provided in the below table and the interfaces which are available at Board-to-Board Connector1 are explained in the following sections. The Board-to-Board Connector1 (J6) is physically located on bottom side of the SOM as shown below.

Number of Pins - 400
Connector Part Number - ASP-209946-01 from Samtech
Mating Connector - ASP-214802-01 from Samtech
Staking Height - 5mm

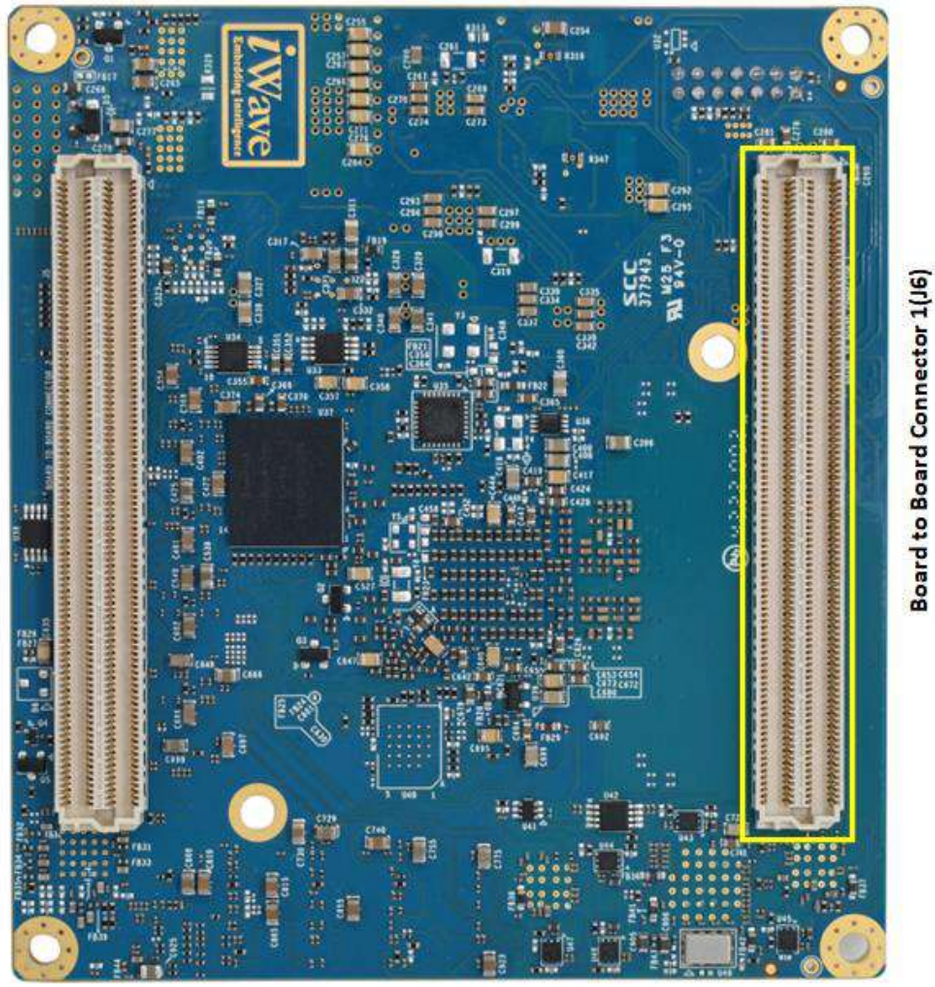


Figure 7: Board to Board Connector1

Table 11: Board to Board Connector1 Pinout

B2B-1 Pin	Signal Name	B2B-1 Pin	Signal Name	B2 B-1 Pin	Signal Name	B2B-1 Pin	Signal Name
A1	VCCO_HDB	B1	VCCO_HPB	C1	VCCO_HPB	D1	VCCO_HPB
A2	PL_B32_LVDS67_L23P	B2	PL_B28_LVDS67_L22P_DBC	C2	PL_D29_LVDS67_L17P	D2	PL_F27_LVDS67_L16P_QBC
A3	PL_A32_LVDS67_L23N	B3	PL_A28_LVDS67_L22N_DBC	C3	PL_C29_LVDS67_L17N	D3	PL_F28_LVDS67_L16N_QBC
A4	PL_H30_LVDS67_L11P_GC	B4	PL_B30_LVDS67_L21P	C4	PL_B27_LVDS67_L20P	D4	PL_F29_LVDS67_L15P
A5	PL_G30_LVDS67_L11N_GC	B5	PL_B31_LVDS67_L21N	C5	PL_A27_LVDS67_L20N	D5	PL_E29_LVDS67_L15N
A6	PL_H28_LVDS67_L12P_GC	B6	PL_A29_LVDS67_L24P	C6	PL_C30_LVDS67_L19P_DBC	D6	PL_E27_LVDS67_L18P
A7	PL_H29_LVDS67_L12N_GC	B7	PL_A30_LVDS67_L24N	C7	PL_C31_LVDS67_L19N_DBC	D7	PL_D27_LVDS67_L18N
A8	GND	B8	GND	C8	GND	D8	GND
A9	PL_N26_LVDS67_L3P	B9	PL_L25_LVDS67_L6P	C9	PL_K29_LVDS67_L9P	D9	PL_F30_LVDS67_L13P_GC
A10	PL_M26_LVDS67_L3N	B10	PL_K25_LVDS67_L6N	C10	PL_J29_LVDS67_L9N	D10	PL_E30_LVDS67_L13N_GC
A11	PL_R25_LVDS67_L2P	B11	PL_M27_LVDS67_L5P	C11	PL_K26_LVDS67_L8P	D11	PL_G27_LVDS67_L14P_GC
A12	PL_R26_LVDS67_L2N	B12	PL_M28_LVDS67_L5N	C12	PL_J26_LVDS67_L8N	D12	PL_G28_LVDS67_L14N_GC
A13	PL_R27_LVDS67_L1P_DBC	B13	PL_N25_LVDS67_L4P_DBC	C13	PL_L28_LVDS67_L7P_QBC	D13	PL_J27_LVDS67_L10P_QBC
A14	PL_P27_LVDS67_L1N_DBC	B14	PL_M25_LVDS67_L4N_DBC	C14	PL_L29_LVDS67_L7N_QBC	D14	PL_J28_LVDS67_L10N_QBC
A15	GND	B15	GND	C15	GND	D15	GND
A16	PL_D23_LVDS68_L18P	B16	PL_C26_LVDS68_L19P_DBC	C16	PL_C25_LVDS68_L21P	D16	PL_G25_LVDS68_L15P
A17	PL_C23_LVDS68_L18N	B17	PL_B26_LVDS68_L19N_DBC	C17	PL_B25_LVDS68_L21N	D17	PL_F25_LVDS68_L15N
A18	PL_H24_LVDS68_L11P_GC	B18	PL_D24_LVDS68_L20P	C18	PL_A22_LVDS68_L24P	D18	PL_E22_LVDS68_L16P_QBC
A19	PL_H25_LVDS68_L11N_GC	B19	PL_C24_LVDS68_L20N	C19	PL_A23_LVDS68_L24N	D19	PL_D22_LVDS68_L16N_QBC
A20	PL_G22_LVDS68_L12P_GC	B20	PL_E26_LVDS68_L17P	C20	PL_A24_LVDS68_L23P	D20	PL_B22_LVDS68_L22P_DBC
A21	PL_F22_LVDS68_L12N_GC	B21	PL_D26_LVDS68_L17N	C21	PL_A25_LVDS68_L23N	D21	PL_B23_LVDS68_L22N_DBC
A22	GND	B22	GND	C22	GND	D22	GND
A23	PL_R22_LVDS68_L2P	B23	PL_N21_LVDS68_L3P	C23	PL_K24_LVDS68_L9P	D23	PL_H26_LVDS68_L13P_GC
A24	PL_P23_LVDS68_L2N	B24	PL_M21_LVDS68_L3N	C24	PL_J24_LVDS68_L9N	D24	PL_G26_LVDS68_L13N_GC
A25	PL_M22_LVDS68_L6P	B25	PL_R24_LVDS68_L4P_DBC	C25	PL_K22_LVDS68_L8P	D25	PL_F23_LVDS68_L14P_GC
A26	PL_M23_LVDS68_L6N	B26	PL_P24_LVDS68_L4N_DBC	C26	PL_J22_LVDS68_L8N	D26	PL_F24_LVDS68_L14N_GC
A27	PL_N23_LVDS68_L5P	B27	PL_R21_LVDS68_L1P_DBC	C27	PL_L23_LVDS68_L7P_QBC	D27	PL_H23_LVDS68_L10P_QBC
A28	PL_N24_LVDS68_L5N	B28	PL_P21_LVDS68_L1N_DBC	C28	PL_L24_LVDS68_L7N_QBC	D28	PL_G23_LVDS68_L10N_QBC

B2B-1 Pin	Signal Name	B2B-1 Pin	Signal Name	B2 B-1 Pin	Signal Name	B2B-1 Pin	Signal Name
A29	GND	B29	GND	C29	GND	D29	GND
A30	PL_D19_LVDS69_L18P	B30	PL_M20_LVDS69_L5P	C30	PL_H18_LVDS69_L10P_QBC	D30	PL_J18_LVDS69_L8P
A31	PL_D18_LVDS69_L18N	B31	PL_L20_LVDS69_L5N	C31	PL_G18_LVDS69_L10N_QBC	D31	PL_J17_LVDS69_L8N
A32	PL_J21_LVDS69_L11P_GC	B32	PL_M18_LVDS69_L6P	C32	PL_P19_LVDS69_L4P_DBC	D32	PL_K21_LVDS69_L7P_QBC
A33	PL_H21_LVDS69_L11N_GC	B33	PL_L18_LVDS69_L6N	C33	PL_N18_LVDS69_L4N_DBC	D33	PL_K20_LVDS69_L7N_QBC
A34	PL_G17_LVDS69_L12P_GC	B34	PL_E21_LVDS69_L17P	C34	PL_N20_LVDS69_L3P	D34	PL_J19_LVDS69_L9P
A35	PL_F17_LVDS69_L12N_GC	B35	PL_E20_LVDS69_L17N	C35	PL_N19_LVDS69_L3N	D35	PL_H19_LVDS69_L9N
A36	GND	B36	GND	C36	GND	D36	GND
A37	PL_A18_LVDS69_L24P	B37	PL_D21_LVDS69_L19P_DBC	C37	PL_R17_LVDS69_L2P	D37	NC
A38	PL_B18_LVDS69_L24N	B38	PL_C21_LVDS69_L19N_DBC	C38	PL_P17_LVDS69_L2N	D38	NC
A39	PL_A17_LVDS69_L22P_DBC	B39	PL_C19_LVDS69_L20P	C39	PL_G21_LVDS69_L15P	D39	NC
A40	PL_B17_LVDS69_L22N_DBC	B40	PL_C18_LVDS69_L20N	C40	PL_F20_LVDS69_L15N	D40	NC
A41	PL_B21_LVDS69_L21P	B41	PL_A19_LVDS69_L23P	C41	PL_E17_LVDS69_L16P_QBC	D41	PL_R20_LVDS69_L1P_DBC
A42	PL_B20_LVDS69_L21N	B42	PL_A20_LVDS69_L23N	C42	PL_D17_LVDS69_L16N_QBC	D42	PL_R19_LVDS69_L1N_DBC
A43	GND	B43	GND	C43	GND	D43	GND
A44	PL_F14_LVDS87_L12P	B44	PL_A13_LVDS87_L5P_HDGC	C44	PL_D13_LVDS87_L2P	D44	PL_D16_LVDS87_L10P
A45	PL_F13_LVDS87_L12N	B45	PL_A12_LVDS87_L5N_HDGC	C45	PL_D12_LVDS87_L2N	D45	PL_C16_LVDS87_L10N
A46	PL_B16_LVDS87_L8P_HDGC	B46	PL_F15_LVDS87_L6P_HDGC	C46	PL_D14_LVDS87_L3P	D46	PL_E16_LVDS87_L9P
A47	PL_B15_LVDS87_L8N_HDGC	B47	PL_E14_LVDS87_L6N_HDGC	C47	PL_C13_LVDS87_L3N	D47	PL_E15_LVDS87_L9N
A48	PL_C15_LVDS87_L7P_HDGC	B48	PL_A15_LVDS87_L11P	C48	PL_B13_LVDS87_L4P	D48	PL_F12_LVDS87_L1P
A49	PL_C14_LVDS87_L7N_HDGC	B49	PL_A14_LVDS87_L11N	C49	PL_B12_LVDS87_L4N	D49	PL_E12_LVDS87_L1N
A50	GND	B50	GND	C50	GND	D50	GND
A51	PL_AR12_LVDS84_L9P	B51	PL_AP11_LVDS84_L12P	C51	PL_BA10_LVDS84_L2P	D51	PL_AU12_LVDS84_L8P_HDGC
A52	PL_AT12_LVDS84_L9N	B52	PL_AP10_LVDS84_L12N	C52	PL_BB9_LVDS84_L2N	D52	PL_AU11_LVDS84_L8N_HDGC
A53	PL_AV11_LVDS84_L5P_HDGC	B53	PL_AR10_LVDS84_L10P	C53	PL_AV9_LVDS84_L6P_HDGC	D53	PL_AU10_LVDS84_L7P_HDGC
A54	PL_AW11_LVDS84_L5N_HDGC	B54	PL_AT10_LVDS84_L10N	C54	PL_AW9_LVDS84_L6N_HDGC	D54	PL_AV10_LVDS84_L7N_HDGC
A55	PL_BB11_LVDS84_L1P	B55	PL_AP12_LVDS84_L11P	C55	PL_AY11_LVDS84_L4P	D55	PL_AY9_LVDS84_L3P
A56	PL_BB10_LVDS84_L1N	B56	PL_AR11_LVDS84_L11N	C56	PL_AY10_LVDS84_L4N	D56	PL_BA9_LVDS84_L3N
A57	GND	B57	GND	C57	GND	D57	GND

B2B-1 Pin	Signal Name	B2B-1 Pin	Signal Name	B2 B-1 Pin	Signal Name	B2B-1 Pin	Signal Name
A58	GND	B58	GND	C58	GND	D58	GND
A59	DAC_REF_CLK_P_231	B59	DAC_REF_CLK_P_230	C59	GND	D59	GND
A60	DAC_REF_CLK_N_231	B60	DAC_REF_CLK_N_230	C60	GND	D60	GND
A61	GND	B61	GND	C61	GND	D61	GND
A62	GND	B62	GND	C62	GND	D62	GND
A63	DAC_T3_CH3_P_231	B63	DAC_T3_CH2_P_231	C63	DAC_T3_CH1_P_231	D63	DAC_T3_CH0_P_231
A64	DAC_T3_CH3_N_231	B64	DAC_T3_CH2_N_231	C64	DAC_T3_CH1_N_231	D64	DAC_T3_CH0_N_231
A65	GND	B65	GND	C65	GND	D65	GND
A66	GND	B66	GND	C66	GND	D66	GND
A67	DAC_T2_CH3_P_230	B67	DAC_T2_CH2_P_230	C67	DAC_T2_CH1_P_230	D67	DAC_T2_CH0_P_230
A68	DAC_T2_CH3_N_230	B68	DAC_T2_CH2_N_230	C68	DAC_T2_CH1_N_230	D68	DAC_T2_CH0_N_230
A69	GND	B69	GND	C69	GND	D69	GND
A70	GND	B70	GND	C70	GND	D70	GND
A71	DAC_T1_CH3_P_229	B71	DAC_T1_CH2_P_229	C71	DAC_T1_CH1_P_229	D71	DAC_T1_CH0_P_229
A72	DAC_T1_CH3_N_229	B72	DAC_T1_CH2_N_229	C72	DAC_T1_CH1_N_229	D72	DAC_T1_CH0_N_229
A73	GND	B73	GND	C73	GND	D73	GND
A74	GND	B74	GND	C74	GND	D74	GND
A75	DAC_T0_CH3_P_228	B75	DAC_T0_CH2_P_228	C75	DAC_T0_CH1_P_228	D75	DAC_T0_CH0_P_228
A76	DAC_T0_CH3_N_228	B76	DAC_T0_CH2_N_228	C76	DAC_T0_CH1_N_228	D76	DAC_T0_CH0_N_228
A77	GND	B77	GND	C77	GND	D77	GND
A78	GND	B78	GND	C78	GND	D78	GND
A79	ADC_T3_CH3_P_227	B79	ADC_T3_CH2_P_227	C79	ADC_T3_CH1_P_227	D79	ADC_T3_CH0_P_227
A80	ADC_T3_CH3_N_227	B80	ADC_T3_CH2_N_227	C80	ADC_T3_CH1_N_227	D80	ADC_T3_CH0_N_227
A81	GND	B81	GND	C81	GND	D81	GND
A82	GND	B82	GND	C82	GND	D82	GND
A83	ADC_T2_CH3_P_226	B83	ADC_T2_CH2_P_226	C83	ADC_T2_CH1_P_226	D83	ADC_T2_CH0_P_226
A84	ADC_T2_CH3_N_226	B84	ADC_T2_CH2_N_226	C84	ADC_T2_CH1_N_226	D84	ADC_T2_CH0_N_226
A85	GND	B85	GND	C85	GND	D85	GND
A86	GND	B86	GND	C86	GND	D86	GND
A87	ADC_T1_CH3_P_225	B87	ADC_T1_CH2_P_225	C87	ADC_T1_CH1_P_225	D87	ADC_T1_CH0_P_225

B2B-1 Pin	Signal Name	B2B-1 Pin	Signal Name	B2B-1 Pin	Signal Name	B2B-1 Pin	Signal Name
A88	ADC_T1_CH3_N_225	**B88**	ADC_T1_CH2_N_225	**C88**	ADC_T1_CH1_N_225	**D88**	ADC_T1_CH0_N_225
A89	GND	**B89**	GND	**C89**	GND	**D89**	GND
A90	GND	**B90**	GND	**C90**	GND	**D90**	GND
A91	ADC_T0_CH3_P_224	**B91**	ADC_T0_CH2_P_224	**C91**	ADC_T0_CH1_P_224	**D91**	ADC_T0_CH0_P_224
A92	ADC_T0_CH3_N_224	**B92**	ADC_T0_CH2_N_224	**C92**	ADC_T0_CH1_N_224	**D92**	ADC_T0_CH0_N_224
A93	GND	**B93**	GND	**C93**	GND	**D93**	GND
A94	GND	**B94**	GND	**C94**	GND	**D94**	GND
A95	ADC_REF_CLK_P_227	**B95**	ADC_REF_CLK_P_226	**C95**	GND	**D95**	GND
A96	ADC_REF_CLK_N_227	**B96**	ADC_REF_CLK_N_226	**C96**	GND	**D96**	GND
A97	GND	**B97**	GND	**C97**	GND	**D97**	GND
A98	GND	**B98**	GND	**C98**	GND	**D98**	GND
A99	GND	**B99**	VCM01_226	**C99**	GND	**D99**	VCM01_224
A100	GND	**B100**	VCM01_227	**C100**	GND	**D100**	VCM01_225

- RED: Power Rails
- Purple: Clock signals
- Brown: Optional signals

2.8.1 RF ADC/ADC Overview

The Zynq Ultrascale+ RFSoC (ZU29/39/49DR) SOM RF data convertors include power efficient digital down converters (DDCs) and digital up converters (DUCs) that include programmable interpolation and decimation rates, a numerically controlled oscillator (NCO), and a complex mixer. The DDCs and DUCs can also support multiband operation.

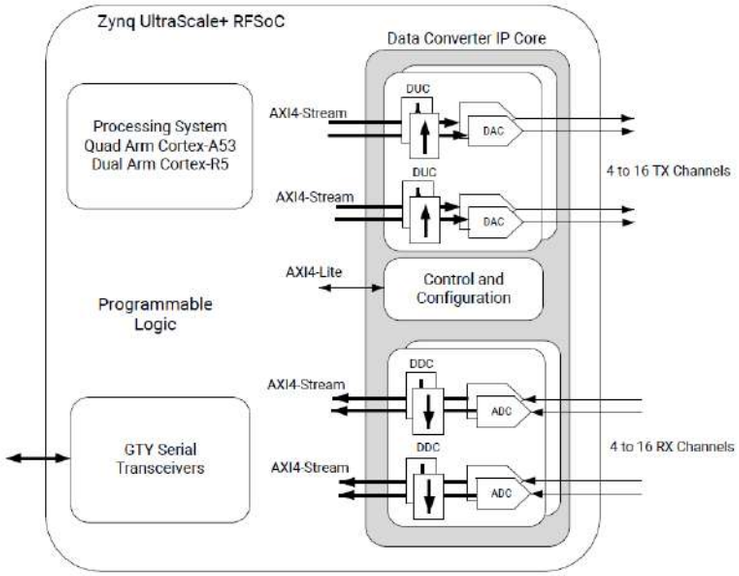


Figure 8: Zynq Ultrascale+ RFSoC Data Converter

2.8.1.1 RF-ADC/DAC Features

- Upto 14-bit RF-DACs
- Supports Multi tile synchronization.
- Pre-program RF-DAC and RF-ADC with Key user-defined parameter
- Decimation and interpolation
- Digital complex mixers and Numerical Controlled Oscillator
- Quadrature Modulation Correction
- On-chip clocking system including PLL for each tile

The RF-ADCs and RF-DACs are organized into tiles, each containing one, two, or four RF-ADCs or one, two, or four RF-DACs. Multiple tiles are available in each Zynq® UltraScale+™ RFSoC device. Each tile also includes a block with a PLL and all the necessary clock handling logic and distribution routing for the analog and digital logic. The Zynq Ultrascale+ RFSoC (ZU29/39/49DR) SOM RF data converter subsystem comprises RF-ADCs and RF-DACs arranged in tiles. Each Size and quantity for each device as shown below on based on tile configurations.

RF Transceiver	16x16	16x16	16x16
Features	**ZU29DR (Gen 1)**	**ZU39DR (Gen 2)**	**ZU49DR (Gen 3)**
14-bit Quad DAC	4	4	4
12-bit Quad ADC	4	4	-
14-bit Quad ADC	-	-	4

The Zynq Ultrascale+ RFSoC (ZU29/39/49DR) SOM Tiles as named as following package bank allocation. RF-ADC are named as Tile 224/225/226/227 and RF-DAC Tile 228/229/230/231.

RF-ADC		RF-DAC	
224	ADC_Tile0	228	DAC_Tile0
225	ADC_Tile1	229	DAC_Tile1
226	ADC_Tile2	230	DAC_Tile2
227	ADC_Tile3	231	DAC_Tile3

2.8.1.2 RF ADC

The Zynq Ultrascale+ RFSoC SOM has 16 ADC RF Signals on Board-to-Board Connector1 from RFSoC's ADC Bank 224,225,226 & 227. It has two of its reference clocks of Bank 227 & Bank 226 on Board-to-Board connector1 pin A95 & A96 and B95 & B96 respectively.

ADC Bank 224 signals are assigned to Board-to-Board Connector1 pin A91, A92, B91, B92, C91, C92, D91 & D92. ADC Bank 225 signals are assigned to Board-to-Board Connector1 pin A87, A88, B87, B88, C87, C88, D87 & D88. ADC Bank 226 signals are assigned to Board-to-Board Connector1 pin A83, A84, B83, B84, C83, C84, D83 &D84. ADC Bank 224 signals are assigned to Board-to-Board Connector1 pin A79, A80, B79, B80, C79, C80, D79 & D79.

B2B-1 Pin No	B2B Connector1 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination*	Description
A91	ADC_T0_CH3_P_224	ADC_VIN3_P_224	224	AR2	I, Analog	Analog Input Signal to ADC Bank 224
A92	ADC_T0_CH3_N_224	ADC_VIN3_N_224	224	AR1	I, Analog	Analog Input Signal to ADC Bank 224
B91	ADC_T0_CH2_P_224	ADC_VIN2_P_224	224	AR5	I, Analog	Analog Input Signal to ADC Bank 224
B92	ADC_T0_CH2_N_224	ADC_VIN2_N_224	224	AR4	I, Analog	Analog Input Signal to ADC Bank 224
C91	ADC_T0_CH1_P_224	ADC_VIN1_P_224	224	AU2	I, Analog	Analog Input Signal to ADC Bank 224
C92	ADC_T0_CH1_N_224	ADC_VIN1_N_224	224	AU1	I, Analog	Analog Input Signal to ADC Bank 224
D91	ADC_T0_CH0_P_224	ADC_VIN0_P_224	224	AU5	I, Analog	Analog Input Signal to ADC Bank 224
D92	ADC_T0_CH0_N_224	ADC_VIN0_N_224	224	AU4	I, Analog	Analog Input Signal to ADC Bank 224
A87	ADC_T1_CH3_P_225	ADC_VIN3_P_225	225	AL2	I, Analog	Analog Input Signal to ADC Bank 225
A88	ADC_T1_CH3_N_225	ADC_VIN3_N_225	225	AL1	I, Analog	Analog Input Signal to ADC Bank 225

B2B-1 Pin No	B2B Connector1 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination*	Description
B87	ADC_T1_CH2_P_225	ADC_VIN2_P_225	225	AL5	I, Analog	Analog Input Signal to ADC Bank 225
B88	ADC_T1_CH2_N_225	ADC_VIN2_N_225	225	AL4	I, Analog	Analog Input Signal to ADC Bank 225
C87	ADC_T1_CH1_P_225	ADC_VIN1_P_225	225	AN2	I, Analog	Analog Input Signal to ADC Bank 225
C88	ADC_T1_CH1_N_225	ADC_VIN1_N_225	225	AN1	I, Analog	Analog Input Signal to ADC Bank 225
D87	ADC_T1_CH0_P_225	ADC_VIN0_P_225	225	AN5	I, Analog	Analog Input Signal to ADC Bank 225
D88	ADC_T1_CH0_N_225	ADC_VIN0_N_225	225	AN4	I, Analog	Analog Input Signal to ADC Bank 225
A83	ADC_T2_CH3_P_226	ADC_VIN3_P_226	226	AG2	I, Analog	Analog Input Signal to ADC Bank 226
A84	ADC_T2_CH3_N_226	ADC_VIN3_N_226	226	AG1	I, Analog	Analog Input Signal to ADC Bank 226
B83	ADC_T2_CH2_P_226	ADC_VIN2_P_226	226	AG5	I, Analog	Analog Input Signal to ADC Bank 226
B84	ADC_T2_CH2_N_226	ADC_VIN2_N_226	226	AG4	I, Analog	Analog Input Signal to ADC Bank 226
C83	ADC_T2_CH1_P_226	ADC_VIN1_P_226	226	AJ2	I, Analog	Analog Input Signal to ADC Bank 226
C84	ADC_T2_CH1_N_226	ADC_VIN1_N_226	226	AJ1	I, Analog	Analog Input Signal to ADC Bank 226
D83	ADC_T2_CH0_P_226	ADC_VIN0_P_226	226	AJ5	I, Analog	Analog Input Signal to ADC Bank 226
D84	ADC_T2_CH0_N_226	ADC_VIN0_N_226	226	AJ4	I, Analog	Analog Input Signal to ADC Bank 226
A79	ADC_T3_CH3_P_227	ADC_VIN3_P_227	227	AC2	I, Analog	Analog Input Signal to ADC Bank 227
A80	ADC_T3_CH3_N_227	ADC_VIN3_N_227	227	AC1	I, Analog	Analog Input Signal to ADC Bank 227
B79	ADC_T3_CH2_P_227	ADC_VIN2_P_227	227	AC5	I, Analog	Analog Input Signal to ADC Bank 227
B80	ADC_T3_CH2_N_227	ADC_VIN2_N_227	227	AC4	I, Analog	Analog Input Signal to ADC Bank 227
C79	ADC_T3_CH1_P_227	ADC_VIN1_P_227	227	AE2	I, Analog	Analog Input Signal to ADC Bank 227
C80	ADC_T3_CH1_N_227	ADC_VIN1_N_227	227	AE1	I, Analog	Analog Input Signal to ADC Bank 227
D79	ADC_T3_CH0_P_227	ADC_VIN0_P_227	227	AE5	I, Analog	Analog Input Signal to ADC Bank 227
D80	ADC_T3_CH0_N_227	ADC_VIN0_N_227	227	AE4	I, Analog	Analog Input Signal to ADC Bank 227
A95	ADC_REF_CLK_P_ 227	ADC_CLK_P_227	227	AW6	I, RF PLL	ADC Reference clock to ADC Bank 227
A96	ADC_REF_CLK_N_ 227	ADC_CLK_N_227	227	AY6	I, RF PLL	ADC Reference clock to ADC Bank 227
B95	ADC_REF_CLK_P_ 226	ADC_CLK_P_226	226	BA5	I, RF PLL	ADC Reference clock to ADC Bank 226
B96	ADC_REF_CLK_N_ 226	ADC_CLK_N_226	226	BB5	I, RF PLL	ADC Reference clock to ADC Bank 226

2.8.1.3 RF DAC

The Zynq Ultrascale+ RFSoC SOM has 16 DAC RF Signals on Board-to-Board Connector1 from RFSoC's DAC Bank 228,229,230 & 231.It has two of its reference clocks of Bank 230 & Bank 231 on Board-to-Board connector1 pin B59 & B60 and A59 & A60 respectively.IO voltage of these DAC banks is from low noise regulator.

DAC Bank 228 signals are assigned to Board-to-Board Connector1 pin A75, A76, B75, B76, C75, C76, D75 & D76. DAC Bank 229 signals are assigned to Board-to-Board Connector1 pin A71, A72, B71, B72, C71, C72, D71 & D72. DAC Bank 230 signals are assigned to Board-to-Board Connector1 pin A67, A68, B67, B68, C67, C68, D67 & D68. DAC Bank 231 signals are assigned to Board-to-Board Connector1 pin A63, A64, B63, B64, C63, C64, D63 & D64

B2B-1 Pin No	B2B Connector1 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination*	Description
A75	DAC_T0_CH3_P_228	DAC_VOUT3_P_228	228	V2	O, Analog	Analog Output Signal from DAC Bank 228
A76	DAC_T0_CH3_N_228	DAC_VOUT3_N_228	228	V1	O, Analog	Analog Output Signal from DAC Bank 228
B75	DAC_T0_CH2_P_228	DAC_VOUT2_P_228	228	V5	O, Analog	Analog Output Signal from DAC Bank 228
B76	DAC_T0_CH2_N_228	DAC_VOUT2_N_228	228	V4	O, Analog	Analog Output Signal from DAC Bank 228
C75	DAC_T0_CH1_P_228	DAC_VOUT1_P_228	228	Y2	O, Analog	Analog Output Signal from DAC Bank 228
C76	DAC_T0_CH1_N_228	DAC_VOUT1_N_228	228	Y1	O, Analog	Analog Output Signal from DAC Bank 228
D75	DAC_T0_CH0_P_228	DAC_VOUT0_P_228	228	Y5	O, Analog	Analog Output Signal from DAC Bank 228
D76	DAC_T0_CH0_N_228	DAC_VOUT0_N_228	228	Y4	O, Analog	Analog Output Signal from DAC Bank 228
A71	DAC_T1_CH3_P_229	DAC_VOUT3_P_229	229	P2	O, Analog	Analog Output Signal from DAC Bank 229
A72	DAC_T1_CH3_N_229	DAC_VOUT3_N_229	229	P1	O, Analog	Analog Output Signal from DAC Bank 229
B71	DAC_T1_CH2_P_229	DAC_VOUT2_P_229	229	P5	O, Analog	Analog Output Signal from DAC Bank 229
B72	DAC_T1_CH2_N_229	DAC_VOUT2_N_229	229	P4	O, Analog	Analog Output Signal from DAC Bank 229
C71	DAC_T1_CH1_P_229	DAC_VOUT1_P_229	229	T2	O, Analog	Analog Output Signal from DAC Bank 229
C72	DAC_T1_CH1_N_229	DAC_VOUT1_N_229	229	T1	O, Analog	Analog Output Signal from DAC Bank 229
D71	DAC_T1_CH0_P_229	DAC_VOUT0_P_229	229	T5	O, Analog	Analog Output Signal from DAC Bank 229

B2B-1 Pin No	B2B Connector1 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination*	Description
D72	DAC_T1_CH0_N_229	DAC_VOUT0_N_229	229	T4	O, Analog	Analog Output Signal from DAC Bank 229
A67	DAC_T2_CH3_P_230	DAC_VOUT3_P_230	230	K2	O, Analog	Analog Output Signal from DAC Bank 230
A68	DAC_T2_CH3_N_230	DAC_VOUT3_N_230	230	K1	O, Analog	Analog Output Signal from DAC Bank 230
B67	DAC_T2_CH2_P_230	DAC_VOUT2_P_230	230	K5	O, Analog	Analog Output Signal from DAC Bank 230
B68	DAC_T2_CH2_N_230	DAC_VOUT2_N_230	230	K4	O, Analog	Analog Output Signal from DAC Bank 230
C67	DAC_T2_CH1_P_230	DAC_VOUT1_P_230	230	M2	O, Analog	Analog Output Signal from DAC Bank 230
C68	DAC_T2_CH1_N_230	DAC_VOUT1_N_230	230	M1	O, Analog	Analog Output Signal from DAC Bank 230
D67	DAC_T2_CH0_P_230	DAC_VOUT0_P_230	230	M5	O, Analog	Analog Output Signal from DAC Bank 230
D68	DAC_T2_CH0_N_230	DAC_VOUT0_N_230	230	M4	O, Analog	Analog Output Signal from DAC Bank 230
A63	DAC_T3_CH3_P_231	DAC_VOUT3_P_231	231	F2	O, Analog	Analog Output Signal from DAC Bank 231
A64	DAC_T3_CH3_N_231	DAC_VOUT3_N_231	231	F1	O, Analog	Analog Output Signal from DAC Bank 231
B63	DAC_T3_CH2_P_231	DAC_VOUT2_P_231	231	F5	O, Analog	Analog Output Signal from DAC Bank 231
B64	DAC_T3_CH2_N_231	DAC_VOUT2_N_231	231	F4	O, Analog	Analog Output Signal from DAC Bank 231
C63	DAC_T3_CH1_P_231	DAC_VOUT1_P_231	231	H2	O, Analog	Analog Output Signal from DAC Bank 231
C64	DAC_T3_CH1_N_231	DAC_VOUT1_N_231	231	H1	O, Analog	Analog Output Signal from DAC Bank 231
D63	DAC_T3_CH0_P_231	DAC_VOUT0_P_231	231	H5	O, Analog	Analog Output Signal from DAC Bank 231
D64	DAC_T3_CH0_N_231	DAC_VOUT0_N_231	231	H4	O, Analog	Analog Output Signal from DAC Bank 231
A59	DAC_REF_CLK_P_231	DAC_CLK_P_231	231	D6	I, RF PLL	DAC Reference clock to DAC Bank 231
A60	DAC_REF_CLK_N_231	DAC_CLK_N_231	231	C6	I, RF PLL	DAC Reference clock to DAC Bank 231
B59	DAC_REF_CLK_P_230	DAC_CLK_P_230	230	B5	I, RF PLL	DAC Reference clock to DAC Bank 230
B60	DAC_REF_CLK_N_230	DAC_CLK_N_230	230	A5	I, RF PLL	DAC Reference clock to DAC Bank 230

2.8.2 PL Interfaces

The interfaces which are supported in Board-to-Board Connector1 from Zynq Ultrascale+ RFSoC's PL is explained in the following section.

2.8.2.1 PL IOs – HP BANK67

The Zynq Ultrascale+ RFSoC SOM supports 24 LVDS IOs/48 Single Ended (SE) IOs on Board-to-Board Connector1 from RFSoC's PL High Performance (HP) Bank67. Upon these 24 LVDS IOs/48 SE IOs, upto 4 GC Global Clock Inputs and upto 16 PLSYSMON auxiliary analog inputs are available.

The IO voltage of PL Bank67 (Bank68&69) is connected from LDO1 output of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 0.95V to 1.8V through software. While using as LVDS IOs or Single Ended IOs, make sure to set the PMIC LDO1 to output appropriate IO voltage for PL Bank68 & 69. By default, IO voltage of PL Bank67 is set as 1V and after U-boot bootup configurable to 1.8V. For more details about supported IO standard, refer the Zynq Ultrascale+ RFSoC datasheet.

In the Zynq Ultrascale+ RFSoC SOM, PL Bank67 signals are routed as LVDS IOs to Board-to-Board Connector1. Even though PL Bank67 signals are routed as LVDS IOs, these pins can be used as SE IOs if required. The Board-to-Board Connector1 pins A4, A5, A6, A7, D9, D10, D11, and D12 are GC Global Clock Input capable pins of PL Bank67. Also, Board to Board Connector1 pins A9, A10, B2, B3, B4, B5, B9, B10, B11, B12, B13, B14, C2, C3, C4, C5, C6, C7, C9, C10, C11, C12, C13, C14, D2, D3, D4, D5, D6, D7, D13 and D14 are PLSYSMON auxiliary analog Input capable pins of PL Bank67.

Important Note: While changing the I/O voltage of PL Bank67, make sure to change the I/O standard of RFSoC Banks (Bank67 & 68,69), since all are sharing the same I/O power rail from PMIC LDO1.

For more details on PL HP Bank67 pinouts on Board-to-Board Connector1, refer the below table.

B2B-1 Pin No	B2B Connector1 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination*	Description
A2	PL_B32_LVDS67_L23P	IO_L23P_T3U_N8_67	67	B32	IO, 1.8V	PL Bank67 IO23 differential positive. Same pin can be configured as Single ended I/O.
A3	PL_A32_LVDS67_L23N	IO_L23N_T3U_N9_67	67	A32	IO, 1.8V	PL Bank67 IO23 differential negative. Same pin can be configured as Single ended I/O.
A4	PL_H30_LVDS67_L11P_GC	IO_L11P_T1U_N8_GC_67	67	H30	IO, 1.8V	PL Bank67 IO11 differential positive. Same pin can be configured as GC Global clock Input differential positive or Single ended I/O.

B2B-1 Pin No	B2B Connector1 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination*	Description
A5	PL_G30_LVDS67_L11N_GC	IO_L11N_T1U_N9_GC_67	67	G30	IO, 1.8V	PL Bank67 IO11 differential negative. Same pin can be configured as GC Global clock Input differential negative or Single ended I/O.
A6	PL_H28_LVDS67_L12P_GC	IO_L12P_T1U_N10_GC_67	67	H28	IO, 1.8V	PL Bank67 IO12 differential positive. Same pin can be configured as GC Global clock Input differential positive or Single ended I/O.
A7	PL_H29_LVDS67_L12N_GC	IO_L12N_T1U_N11_GC_67	67	H29	IO, 1.8V	PL Bank67 IO12 differential negative. Same pin can be configured as GC Global clock Input differential negative or Single ended I/O.
A9	PL_N26_LVDS67_L3P	IO_L3P_T0L_N4_AD15P_67	67	N26	IO, 1.8V	PL Bank67 IO3 differential positive. Same pin can be configured as PLSYSMON differential analog input15 positive or Single ended I/O
A10	PL_M26_LVDS67_L3N	IO_L3N_T0L_N5_AD15N_67	67	M26	IO, 1.8V	PL Bank67 IO3 differential negative. Same pin can be configured as PLSYSMON differential analog input15 negative or Single ended I/O
A11	PL_R25_LVDS67_L2P	IO_L2P_T0L_N2_67	67	R25	IO, 1.8V	PL Bank67 IO2 differential positive. Same pin can be configured as Single ended I/O.
A12	PL_R26_LVDS67_L2N	IO_L2N_T0L_N3_67	67	R26	IO, 1.8V	PL Bank67 IO2 differential negative. Same pin can be configured as Single ended I/O.
A13	PL_R27_LVDS67_L1P_DBC	IO_L1P_T0L_N0_DBC_67	67	R27	IO, 1.8V	PL Bank67 IO1 differential positive. Same pin can be configured as Single ended I/O.
A14	PL_P27_LVDS67_L1N_DBC	IO_L1N_T0L_N1_DBC_67	67	P27	IO, 1.8V	PL Bank67 IO1 differential negative. Same pin can be configured as Single ended I/O.
B2	PL_B28_LVDS67_L22P_DBC	IO_L22P_T3U_N6_DBC_AD0P_67	67	B28	IO, 1.8V	PL Bank67 IO22 differential positive. Same pin can be configured as PLSYSMON differential analog input0 positive or Single ended I/O.

B2B-1 Pin No	B2B Connector1 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination*	Description
B3	PL_A28_LVDS67_L22N_DBC	IO_L22N_T3U_N7_DBC_AD0N_67	67	A28	IO, 1.8V	PL Bank67 IO22 differential negative. Same pin can be configured as PLSYSMON differential analog input0 negative or Single ended I/O.
B4	PL_B30_LVDS67_L21P	IO_L21P_T3L_N4_AD8P_67	67	B30	IO, 1.8V	PL Bank67 IO21 differential positive. Same pin can be configured as PLSYSMON differential analog input8 positive or Single ended I/O.
B5	PL_B31_LVDS67_L21N	IO_L21N_T3L_N5_AD8N_67	67	B31	IO, 1.8V	PL Bank67 IO21 differential negative. Same pin can be configured as PLSYSMON differential analog input8 negative or Single ended I/O.
B6	PL_A29_LVDS67_L24P	IO_L24P_T3U_N10_67	67	A29	IO, 1.8V	PL Bank67 IO24 differential positive. Same pin can be configured as Single ended I/O.
B7	PL_A30_LVDS67_L24N	IO_L24N_T3U_N11_67	67	A30	IO, 1.8V	PL Bank67 IO24 differential negative. Same pin can be configured as Single ended I/O.
B9	PL_L25_LVDS67_L6P	IO_L6P_T0U_N10_AD6P_67	67	L25	IO, 1.8V	PL Bank67 IO6 differential positive. Same pin can be configured as PLSYSMON differential analog input6 positive or Single ended I/O.
B10	PL_K25_LVDS67_L6N	IO_L6N_T0U_N11_AD6N_67	67	K25	IO, 1.8V	PL Bank67 IO6 differential negative. Same pin can be configured as PLSYSMON differential analog input6 negative or Single ended I/O.
B11	PL_M27_LVDS67_L5P	IO_L5P_T0U_N8_AD14P_67	67	M27	IO, 1.8V	PL Bank67 IO5 differential positive. Same pin can be configured as PLSYSMON differential analog input14 positive or Single ended I/O.
B12	PL_M28_LVDS67_L5N	IO_L5N_T0U_N9_AD14N_67	67	M28	IO, 1.8V	PL Bank67 IO5 differential negative. Same pin can be configured as PLSYSMON differential analog input14 negative or Single ended I/O.
B13	PL_N25_LVDS67_L4P_DBC	IO_L4P_T0U_N6_DBC_AD7P_67	67	N25	IO, 1.8V	PL Bank67 IO4 differential positive. Same pin can be configured as PLSYSMON differential analog input7 positive or Single ended I/O.

B2B-1 Pin No	B2B Connector1 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination*	Description
B14	PL_M25_LVDS67 _L4N_DBC	IO_L4N_T0U_N7_ DBC_AD7N_67	67	M25	IO, 1.8V	PL Bank67 IO4 differential negative. Same pin can be configured as PLSYSMON differential analog input7 negative or Single ended I/O.
C2	PL_D29_LVDS67_ L17P	IO_L17P_T2U_N8 _AD10P_67	67	D29	IO, 1.8V	PL Bank67 IO17 differential positive. Same pin can be configured as PLSYSMON differential analog input10 positive or Single ended I/O.
C3	PL_C29_LVDS67_ L17N	IO_L17N_T2U_N9 _AD10N_67	67	C29	IO, 1.8V	PL Bank67 IO17 differential negative. Same pin can be configured as PLSYSMON differential analog input10 negative or Single ended I/O.
C4	PL_B27_LVDS67_ L20P	IO_L20P_T3L_N2_ AD1P_67	67	B27	IO, 1.8V	PL Bank67 IO20 differential positive. Same pin can be configured as PLSYSMON differential analog input1 positive or Single ended I/O.
C5	PL_A27_LVDS67_ L20N	IO_L20N_T3L_N3_ AD1N_67	67	A27	IO, 1.8V	PL Bank67 IO20 differential negative. Same pin can be configured as PLSYSMON differential analog input1 negative or Single ended I/O.
C6	PL_C30_LVDS67_ L19P_DBC	IO_L19P_T3L_N0_ DBC_AD9P_67	67	C30	IO, 1.8V	PL Bank67 IO19 differential positive. Same pin can be configured as PLSYSMON differential analog input9 positive or Single ended I/O.
C7	PL_C31_LVDS67_ L19N_DBC	IO_L19N_T3L_N1_ DBC_AD9N_67	67	C31	IO, 1.8V	PL Bank67 IO19 differential negative. Same pin can be configured as PLSYSMON differential analog input9 negative or Single ended I/O.
C9	PL_K29_LVDS67_ L9P	IO_L9P_T1L_N4_ AD12P_67	67	K29	IO, 1.8V	PL Bank67 IO9 differential positive. Same pin can be configured as PLSYSMON differential analog input12 positive or Single ended I/O.
C10	PL_J29_LVDS67_ L9N	IO_L9N_T1L_N5_ AD12N_67	67	J29	IO, 1.8V	PL Bank67 IO9 differential negative. Same pin can be configured as PLSYSMON differential analog input12 negative or Single ended I/O.

B2B-1 Pin No	B2B Connector1 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination*	Description
C11	PL_K26_LVDS67_L8P	IO_L8P_T1L_N2_AD5P_67	67	K26	IO, 1.8V	PL Bank67 IO8 differential positive. Same pin can be configured as PLSYSMON differential analog input5 positive or Single ended I/O.
C12	PL_J26_LVDS67_L8N	IO_L8N_T1L_N3_AD5N_67	67	J26	IO, 1.8V	PL Bank67 IO8 differential negative. Same pin can be configured as PLSYSMON differential analog input5 negative or Single ended I/O.
C13	PL_L28_LVDS67_L7P_QBC	IO_L7P_T1L_N0_QBC_AD13P_67	67	L28	IO, 1.8V	PL Bank67 IO7 differential positive. Same pin can be configured as PLSYSMON differential analog input13 positive or Single ended I/O.
C14	PL_L29_LVDS67_L7N_QBC	IO_L7N_T1L_N1_QBC_AD13N_67	67	L29	IO, 1.8V	PL Bank67 IO7 differential negative. Same pin can be configured as PLSYSMON differential analog input13 negative or Single ended I/O.
D2	PL_F27_LVDS67_L16P_QBC	IO_L16P_T2U_N6_QBC_AD3P_67	67	F27	IO, 1.8V	PL Bank67 IO16 differential positive. Same pin can be configured as PLSYSMON differential analog input3 positive or Single ended I/O.
D3	PL_F28_LVDS67_L16N_QBC	IO_L16N_T2U_N7_QBC_AD3N_67	67	F28	IO, 1.8V	PL Bank67 IO16 differential negative. Same pin can be configured as PLSYSMON differential analog input3 negative or Single ended I/O.
D4	PL_F29_LVDS67_L15P	IO_L15P_T2L_N4_AD11P_67	67	F29	IO, 1.8V	PL Bank67 IO15 differential positive. Same pin can be configured as PLSYSMON differential analog input11 positive or Single ended I/O.
D5	PL_E29_LVDS67_L15N	IO_L15N_T2L_N5_AD11N_67	67	E29	IO, 1.8V	PL Bank67 IO15 differential negative. Same pin can be configured as PLSYSMON differential analog input11 negative or Single ended I/O.
D6	PL_E27_LVDS67_L18P	IO_L18P_T2U_N10_AD2P_67	67	E27	IO, 1.8V	PL Bank67 IO18 differential positive. Same pin can be configured as PLSYSMON differential analog input2 positive or Single ended I/O

B2B-1 Pin No	B2B Connector1 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination*	Description
D7	PL_D27_LVDS67_L18N	IO_L18N_T2U_N11_AD2N_67	67	D27	IO, 1.8V	PL Bank67 IO18 differential negative. Same pin can be configured as PLSYSMON differential analog input2 negative or Single ended I/O.
D9	PL_F30_LVDS67_L13P_GC	IO_L13P_T2L_N0_GC_QBC_67	67	F30	IO, 1.8V	PL Bank67 IO13 differential positive. Same pin can be configured as GC Global clock Input differential positive or Single ended I/O.
D10	PL_E30_LVDS67_L13N_GC	IO_L13N_T2L_N1_GC_QBC_67	67	E30	IO, 1.8V	PL Bank67 IO13 differential negative. Same pin can be configured as GC Global clock Input differential negative or Single ended I/O.
D11	PL_G27_LVDS67_L14P_GC	IO_L14P_T2L_N2_GC_67	67	G27	IO, 1.8V	PL Bank67 IO14 differential positive. Same pin can be configured as GC Global clock Input differential positive or Single ended I/O.
D12	PL_G28_LVDS67_L14N_GC	IO_L14N_T2L_N3_GC_67	67	G28	IO, 1.8V	PL Bank67 IO14 differential negative. Same pin can be configured as GC Global clock Input differential negative or Single ended I/O.
D13	PL_J27_LVDS67_L10P_QBC	IO_L10P_T1U_N6_QBC_AD4P_67	67	J27	IO, 1.8V	PL Bank67 IO10 differential positive. Same pin can be configured as PLSYSMON differential analog input4 positive or Single ended I/O.
D14	PL_J28_LVDS67_L10N_QBC	IO_L10N_T1U_N7_QBC_AD4N_67	67	J28	IO, 1.8V	PL Bank67 IO10 differential negative. Same pin can be configured as PLSYSMON differential analog input4 negative or Single ended I/O.

**IO Type of IOs originating from ZU29/39/49 RFSoC is configurable. Hence for exact IO type configuration options, refer Xilinx ZU29/39/49 RFSoC datasheet.*

2.8.2.2 PL IOs – HP BANK68

The Zynq Ultrascale+ RFSoC SOM supports 24 LVDS IOs/48 Single Ended (SE) IOs on Board-to-Board Connector1 from RFSoC's PL High Performance (HP) Bank68. Upon these 24 LVDS IOs/48 SE IOs, upto 4 GC Global Clock Inputs and upto 16 PLSYSMON auxiliary analog inputs are available.

The IO voltage of PL Bank68 (Bank67 & 69) is connected from LDO1 output of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 0.95V to 1.8V through software. While using as LVDS IOs or Single Ended IOs, make sure to set the PMIC LDO1 to output appropriate IO voltage for PL Bank67 & 69. By default, IO voltage of PL Bank68 is set as 1V and after U-boot bootup configurable to 1.8V. For more details about supported IO standard, refer the Zynq Ultrascale+ RFSoC datasheet.

In the Zynq Ultrascale+ RFSoC SOM, PL Bank68 signals are routed as LVDS IOs to Board-to-Board Connector1. Even though PL Bank67 signals are routed as LVDS IOs, these pins can be used as SE IOs if required. The Board-to-Board Connector1 pins A18, A19, A20, A21, D23, D24, D25, and D26 are GC Global Clock Input capable pins of PL Bank68. Also, Board to Board Connector1 pins A16, A17, A25, A26, A27, A28, B16, B17, B18, B19, B20, B21, B23, B24, B25, B26, C16, C17, C23, C24, C25, C26, C27, C28, D16, D17, D18, D19, D20, D21, D27 and D28 are PLSYSMON auxiliary analog Input capable pins of PL Bank68.

Important Note: While changing the I/O voltage of PL Bank68, make sure to change the I/O standard of RFSoC Banks (Bank67 & 68,69), since all are sharing the same I/O power rail from PMIC LDO1.

B2B-1 Pin No	B2B Connector1 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination*	Description
A16	PL_D23_LVDS68_L18P	IO_L18P_T2U_N10_AD2P_68	68	D23	IO, 1.8V	PL Bank68 IO18 differential positive. Same pin can be configured as PLSYSMON differential analog input2 positive or Single ended I/O.
A17	PL_C23_LVDS68_L18N	IO_L18N_T2U_N11_AD2N_68	68	C23	IO, 1.8V	PL Bank68 IO18 differential negative. Same pin can be configured as PLSYSMON differential analog input2 negative or Single ended I/O.
A18	PL_H24_LVDS68_L11P_GC	IO_L11P_T1U_N8_GC_68	68	H24	IO, 1.8V	PL Bank68 IO11 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
A19	PL_H25_LVDS68_L11N_GC	IO_L11N_T1U_N9_GC_68	68	H25	IO, 1.8V	PL Bank68 IO11 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.

B2B-1 Pin No	B2B Connector1 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination*	Description
A20	PL_G22_LVDS68_L12P_GC	IO_L12P_T1U_N10_GC_68	68	G22	IO, 1.8V	PL Bank68 IO12 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
A21	PL_F22_LVDS68_L12N_GC	IO_L12N_T1U_N11_GC_68	68	F22	IO, 1.8V	PL Bank68 IO12 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
A23	PL_R22_LVDS68_L2P	IO_L2P_T0L_N2_68	68	R22	IO, 1.8V	PL Bank68 IO2 differential positive. Same pin can be configured as Single ended I/O.
A24	PL_P23_LVDS68_L2N	IO_L2N_T0L_N3_68	68	P23	IO, 1.8V	PL Bank68 IO2 differential negative. Same pin can be configured as Single ended I/O.
A25	PL_M22_LVDS68_L6P	IO_L6P_T0U_N10_AD6P_68	68	M22	IO, 1.8V	PL Bank68 IO6 differential positive. Same pin can be configured as PLSYSMON differential analog input6 positive or Single ended I/O.
A26	PL_M23_LVDS68_L6N	IO_L6N_T0U_N11_AD6N_68	68	M23	IO, 1.8V	PL Bank68 IO6 differential negative. Same pin can be configured as PLSYSMON differential analog input6 negative or Single ended I/O.
A27	PL_N23_LVDS68_L5P	IO_L5P_T0U_N8_AD14P_68	68	N23	IO, 1.8V	PL Bank68 IO5 differential positive. Same pin can be configured as PLSYSMON differential analog input14 positive or Single ended I/O.
A28	PL_N24_LVDS68_L5N	IO_L5N_T0U_N9_AD14N_68	68	N24	IO, 1.8V	PL Bank68 IO5 differential negative. Same pin can be configured as PLSYSMON differential analog input14 negative or Single ended I/O.
B16	PL_C26_LVDS68_L19P_DBC	IO_L19P_T3L_N0_DBC_AD9P_68	68	C26	IO, 1.8V	PL Bank68 IO19 differential positive. Same pin can be configured as PLSYSMON differential analog input9 positive or Single ended I/O.
B17	PL_B26_LVDS68_L19N_DBC	IO_L19N_T3L_N1_DBC_AD9N_68	68	B26	IO, 1.8V	PL Bank68 IO19 differential negative. Same pin can be configured as PLSYSMON differential analog input9 negative or Single ended I/O.

B2B-1 Pin No	B2B Connector1 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination*	Description
B18	PL_D24_LVDS68_L20P	IO_L20P_T3L_N2_AD1P_68	68	D24	IO, 1.8V	PL Bank68 IO20 differential positive. Same pin can be configured as PLSYSMON differential analog input1 positive or Single ended I/O.
B19	PL_C24_LVDS68_L20N	IO_L20N_T3L_N3_AD1N_68	68	C24	IO, 1.8V	PL Bank68 IO20 differential negative. Same pin can be configured as PLSYSMON differential analog input1 negative or Single ended I/O.
B20	PL_E26_LVDS68_L17P	IO_L17P_T2U_N8_AD10P_68	68	E26	IO, 1.8V	PL Bank68 IO17 differential positive. Same pin can be configured as PLSYSMON differential analog input10 positive or Single ended I/O.
B21	PL_D26_LVDS68_L17N	IO_L17N_T2U_N9_AD10N_68	68	D26	IO, 1.8V	PL Bank68 IO17 differential negative. Same pin can be configured as PLSYSMON differential analog input10 negative or Single ended I/O.
B23	PL_N21_LVDS68_L3P	IO_L3P_T0L_N4_AD15P_68	68	N21	IO, 1.8V	PL Bank68 IO3 differential positive. Same pin can be configured as PLSYSMON differential analog input15 positive or Single ended I/O.
B24	PL_M21_LVDS68_L3N	IO_L3N_T0L_N5_AD15N_68	68	M21	IO, 1.8V	PL Bank68 IO3 differential negative. Same pin can be configured as PLSYSMON differential analog input15 negative or Single ended I/O.
B25	PL_R24_LVDS68_L4P_DBC	IO_L4P_T0U_N6_DBC_AD7P_68	68	R24	IO, 1.8V	PL Bank68 IO4 differential positive. Same pin can be configured as PLSYSMON differential analog input7 positive or Single ended I/O.
B26	PL_P24_LVDS68_L4N_DBC	IO_L4N_T0U_N7_DBC_AD7N_68	68	P24	IO, 1.8V	PL Bank68 IO4 differential negative. Same pin can be configured as PLSYSMON differential analog input7 negative or Single ended I/O.
B27	PL_R21_LVDS68_L1P_DBC	IO_L1P_T0L_N0_DBC_68	68	R21	IO, 1.8V	PL Bank68 IO1 differential positive. Same pin can be configured as Single ended I/O.
B28	PL_P21_LVDS68_L1N_DBC	IO_L1N_T0L_N1_DBC_68	68	P21	IO, 1.8V	PL Bank68 IO1 differential negative. Same pin can be configured as Single ended I/O.

B2B-1 Pin No	B2B Connector1 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination*	Description
C16	PL_C25_LVDS68_L21P	IO_L21P_T3L_N4_AD8P_68	68	C25	IO, 1.8V	PL Bank68 IO21 differential positive. Same pin can be configured as PLSYSMON differential analog input8 positive or Single ended I/O.
C17	PL_B25_LVDS68_L21N	IO_L21N_T3L_N5_AD8N_68	68	B25	IO, 1.8V	PL Bank68 IO21 differential negative. Same pin can be configured as PLSYSMON differential analog input8 negative or Single ended I/O.
C18	PL_A22_LVDS68_L24P	IO_L24P_T3U_N10_68	68	A22	IO, 1.8V	PL Bank68 IO24 differential positive. Same pin can be configured as Single ended I/O.
C19	PL_A23_LVDS68_L24N	IO_L24N_T3U_N11_68	68	A23	IO, 1.8V	PL Bank68 IO24 differential negative. Same pin can be configured as Single ended I/O.
C20	PL_A24_LVDS68_L23P	IO_L23P_T3U_N8_68	68	A24	IO, 1.8V	PL Bank68 IO23 differential positive. Same pin can be configured as Single ended I/O.
C21	PL_A25_LVDS68_L23N	IO_L23N_T3U_N9_68	68	A25	IO, 1.8V	PL Bank68 IO23 differential negative. Same pin can be configured as Single ended I/O.
C23	PL_K24_LVDS68_L9P	IO_L9P_T1L_N4_AD12P_68	68	K24	IO, 1.8V	PL Bank68 IO9 differential positive. Same pin can be configured as PLSYSMON differential analog input12 positive or Single ended I/O.
C24	PL_J24_LVDS68_L9N	IO_L9N_T1L_N5_AD12N_68	68	J24	IO, 1.8V	PL Bank68 IO9 differential negative. Same pin can be configured as PLSYSMON differential analog input12 negative or Single ended I/O.
C25	PL_K22_LVDS68_L8P	IO_L8P_T1L_N2_AD5P_68	68	K22	IO, 1.8V	PL Bank68 IO8 differential positive. Same pin can be configured as PLSYSMON differential analog input5 positive or Single ended I/O.
C26	PL_J22_LVDS68_L8N	IO_L8N_T1L_N3_AD5N_68	68	J22	IO, 1.8V	PL Bank68 IO8 differential negative. Same pin can be configured as PLSYSMON differential analog input5 negative or Single ended I/O.

B2B-1 Pin No	B2B Connector1 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination*	Description
C27	PL_L23_LVDS68_ L7P_QBC	IO_L7P_T1L_N0_Q BC_AD13P_68	68	L23	IO, 1.8V	PL Bank68 IO7 differential positive. Same pin can be configured as PLSYSMON differential analog input13 positive or Single ended I/O.
C28	PL_L24_LVDS68_ L7N_QBC	IO_L7N_T1L_N1_ QBC_AD13N_68	68	L24	IO, 1.8V	PL Bank68 IO7 differential negative. Same pin can be configured as PLSYSMON differential analog input13 negative or Single ended I/O.
D16	PL_G25_LVDS68_ L15P	IO_L15P_T2L_N4_ AD11P_68	68	G25	IO, 1.8V	PL Bank68 IO15 differential positive. Same pin can be configured as PLSYSMON differential analog input11 positive or Single ended I/O.
D17	PL_F25_LVDS68_ L15N	IO_L15N_T2L_N5_ AD11N_68	68	F25	IO, 1.8V	PL Bank68 IO15 differential negative. Same pin can be configured as PLSYSMON differential analog input11 negative or Single ended I/O.
D18	PL_E22_LVDS68_ L16P_QBC	IO_L16P_T2U_N6 _QBC_AD3P_68	68	E22	IO, 1.8V	PL Bank68 IO16 differential positive. Same pin can be configured as PLSYSMON differential analog input3 positive or Single ended I/O.
D19	PL_D22_LVDS68_ L16N_QBC	IO_L16N_T2U_N7 _QBC_AD3N_68	68	D22	IO, 1.8V	PL Bank68 IO16 differential negative. Same pin can be configured as PLSYSMON differential analog input3 negative or Single ended I/O.
D20	PL_B22_LVDS68_ L22P_DBC	IO_L22P_T3U_N6 _DBC_AD0P_68	68	B22	IO, 1.8V	PL Bank68 IO22 differential positive. Same pin can be configured as PLSYSMON differential analog input0 positive or Single ended I/O.
D21	PL_B23_LVDS68_ L22N_DBC	IO_L22N_T3U_N7 _DBC_AD0N_68	68	B23	IO, 1.8V	PL Bank68 IO22 differential negative. Same pin can be configured as PLSYSMON differential analog input0 negative or Single ended I/O.
D23	PL_H26_LVDS68_ L13P_GC	IO_L13P_T2L_N0_ GC_QBC_68	68	H26	IO, 1.8V	PL Bank68 IO13 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.

B2B-1 Pin No	B2B Connector1 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination*	Description
D24	PL_G26_LVDS68_ L13N_GC	IO_L13N_T2L_N1_ GC_QBC_68	68	G26	IO, 1.8V	PL Bank68 IO13 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
D25	PL_F23_LVDS68_ L14P_GC	IO_L14P_T2L_N2_ GC_68	68	F23	IO, 1.8V	PL Bank68 IO14 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
D26	PL_F24_LVDS68_ L14N_GC	IO_L14N_T2L_N3_ GC_68	68	F24	IO, 1.8V	PL Bank68 IO14 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
D27	PL_H23_LVDS68_ L10P_QBC	IO_L10P_T1U_N6 _QBC_AD4P_68	68	H23	IO, 1.8V	PL Bank68 IO10 differential positive. Same pin can be configured as PLSYSMON differential analog input4 positive or Single ended I/O.
D28	PL_G23_LVDS68_ L10N_QBC	IO_L10N_T1U_N7 _QBC_AD4N_68	68	G23	IO, 1.8V	PL Bank68 IO10 differential negative. Same pin can be configured as PLSYSMON differential analog input4 negative or Single ended I/O.

**IO Type of IOs originating from ZU29/39/49 RFSoC is configurable. Hence for exact IO type configuration options, refer Xilinx ZU29/39/49 RFSoC datasheet*

2.8.2.3 PL IOs – HP BANK69

The Zynq Ultrascale+ RFSoC SOM supports 22 LVDS IOs/44 Single Ended (SE) IOs on Board-to-Board Connector1 from RFSoC's PL High Performance (HP) Bank69. Upon these 22 LVDS IOs/44 SE IOs, upto 2 GC Global Clock Inputs and upto 16 PLSYSMON auxiliary analog inputs are available.

The IO voltage of PL Bank69 (Bank67 & 68) is connected from LDO1 output of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 0.95V to 1.8V through software. While using as LVDS IOs or Single Ended IOs, make sure to set the PMIC LDO1 to output appropriate IO voltage for PL Bank67 & 68. By default, IO voltage of PL Bank69 is set as 1V and after U-boot bootup configurable to 1.8V. For more details about supported IO standard, refer the Zynq Ultrascale+ RFSoC datasheet.

In the Zynq Ultrascale+ RFSoC SOM, PL Bank69 signals are routed as LVDS IOs to Board-to-Board Connector1. Even though PL Bank67 signals are routed as LVDS IOs, these pins can be used as SE IOs if required. The Board-to-Board Connector1 pins A32, A33, A34, and A35 are GC Global Clock Input capable pins of PL Bank69. Also, Board to Board Connector1 pins A30, A31, A39, A40, A41, A42, B30, B31, B32, B33, B34, B35, B37, B38, B39, B40, C30, C31, C32, C33, C34, C35, C39, C40, C41, C42, D30, D31, D32, D33, D34, and D35 are PLSYSMON auxiliary analog Input capable pins of PL Bank68.

Important Note: While changing the I/O voltage of PL Bank69, make sure to change the I/O standard of RFSoC Banks (Bank67 & 68,69), since all are sharing the same I/O power rail from PMIC LDO1.

B2B-1 Pin No	B2B Connector1 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination*	Description
A30	PL_D19_LVDS69_L18P	IO_L18P_T2U_N10_AD2P_69	69	D19	IO, 1.8V	PL Bank69 IO18 differential positive. Same pin can be configured as PLSYSMON differential analog input2 positive or Single ended I/O.
A31	PL_D18_LVDS69_L18N	IO_L18N_T2U_N11_AD2N_69	69	D18	IO, 1.8V	PL Bank69 IO18 differential negative. Same pin can be configured as PLSYSMON differential analog input2 negative or Single ended I/O.
A32	PL_J21_LVDS69_L11P_GC	IO_L11P_T1U_N8_GC_69	69	J21	IO, 1.8V	PL Bank69 IO11 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
A33	PL_H21_LVDS69_L11N_GC	IO_L11N_T1U_N9_GC_69	69	H21	IO, 1.8V	PL Bank69 IO11 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.

B2B-1 Pin No	B2B Connector1 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination*	Description
A34	PL_G17_LVDS69_L12P_GC	IO_L12P_T1U_N10_GC_69	69	G17	IO, 1.8V	PL Bank69 IO12 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
A35	PL_F17_LVDS69_L12N_GC	IO_L12N_T1U_N11_GC_69	69	F17	IO, 1.8V	PL Bank69 IO12 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
A37	PL_A18_LVDS69_L24P	IO_L24P_T3U_N11_69	69	A18	IO, 1.8V	PL Bank69 IO24 differential positive. Same pin can be configured as Single ended I/O.
A38	PL_B18_LVDS69_L24N	IO_L24N_T3U_N10_69	69	B18	IO, 1.8V	PL Bank69 IO24 differential negative. Same pin can be configured as Single ended I/O.
A39	PL_A17_LVDS69_L22P_DBC	IO_L22P_T3U_N7_DBC_AD0P_69	69	A17	IO, 1.8V	PL Bank69 IO22 differential positive. Same pin can be configured as PLSYSMON differential analog input0 positive or Single ended I/O.
A40	PL_B17_LVDS69_L22N_DBC	IO_L22N_T3U_N6_DBC_AD0N_69	69	B17	IO, 1.8V	PL Bank69 IO22 differential negative. Same pin can be configured as PLSYSMON differential analog input0 negative or Single ended I/O.
A41	PL_B21_LVDS69_L21P	IO_L21P_T3L_N4_AD8P_69	69	B21	IO, 1.8V	PL Bank69 IO21 differential positive. Same pin can be configured as PLSYSMON differential analog input8 positive or Single ended I/O.
A42	PL_B20_LVDS69_L21N	IO_L21N_T3L_N5_AD8N_69	69	B20	IO, 1.8V	PL Bank69 IO21 differential negative. Same pin can be configured as PLSYSMON differential analog input8 negative or Single ended I/O.
B30	PL_M20_LVDS69_L5P	IO_L5P_T0U_N8_AD14P_69	69	M20	IO, 1.8V	PL Bank69 IO5 differential positive. Same pin can be configured as PLSYSMON differential analog input14 positive or Single ended I/O.

B2B-1 Pin No	B2B Connector1 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination*	Description
B31	PL_L20_LVDS69_ L5N	IO_L5N_T0U_N9_ AD14N_69	69	L20	IO, 1.8V	PL Bank69 IO5 differential negative. Same pin can be configured as PLSYSMON differential analog input14 negative or Single ended I/O.
B32	PL_M18_LVDS69 _L6P	IO_L6P_T0U_N10 _AD6P_69	69	M18	IO, 1.8V	PL Bank69 IO6 differential positive. Same pin can be configured as PLSYSMON differential analog input6 positive or Single ended I/O.
B33	PL_L18_LVDS69_ L6N	IO_L6N_T0U_N11 _AD6N_69	69	L18	IO, 1.8V	PL Bank69 IO6 differential negative. Same pin can be configured as PLSYSMON differential analog input6 negative or Single ended I/O.
B34	PL_E21_LVDS69_ L17P	IO_L17P_T2U_N8 _AD10P_69	69	E21	IO, 1.8V	PL Bank69 IO17 differential positive. Same pin can be configured as PLSYSMON differential analog input10 positive or Single ended I/O.
B35	PL_E20_LVDS69_ L17N	IO_L17N_T2U_N9 _AD10N_69	69	E20	IO, 1.8V	PL Bank69 IO17 differential negative. Same pin can be configured as PLSYSMON differential analog input10 negative or Single ended I/O.
B37	PL_D21_LVDS69_ L19P_DBC	IO_L19P_T3L_N0_ DBC_AD9P_69	69	D21	IO, 1.8V	PL Bank69 IO19 differential positive. Same pin can be configured as PLSYSMON differential analog input9 positive or Single ended I/O.
B38	PL_C21_LVDS69_ L19N_DBC	IO_L19N_T3L_N1_ DBC_AD9N_69	69	C21	IO, 1.8V	PL Bank69 IO19 differential negative. Same pin can be configured as PLSYSMON differential analog input9 negative or Single ended I/O.
B39	PL_C19_LVDS69_ L20P	IO_L20P_T3L_N2_ AD1P_69	69	C19	IO, 1.8V	PL Bank69 IO20 differential positive. Same pin can be configured as PLSYSMON differential analog input1 positive or Single ended I/O.
B40	PL_C18_LVDS69_ L20N	IO_L20N_T3L_N3_ AD1N_69	69	C18	IO, 1.8V	PL Bank69 IO20 differential negative. Same pin can be configured as PLSYSMON differential analog input1 negative or Single ended I/O.

B2B-1 Pin No	B2B Connector1 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination*	Description
B41	PL_A19_LVDS69_L23P	IO_L23P_T3U_N9_69	69	A19	IO, 1.8V	PL Bank69 IO23 differential positive. Same pin can be configured as Single ended I/O.
B42	PL_A20_LVDS69_L23N	IO_L23N_T3U_N8_69	69	A20	IO, 1.8V	PL Bank69 IO23 differential negative. Same pin can be configured as Single ended I/O.
C30	PL_H18_LVDS69_L10P_QBC	IO_L10P_T1U_N6_QBC_AD4P_69	69	H18	IO, 1.8V	PL Bank69 IO10 differential positive. Same pin can be configured as PLSYSMON differential analog input4 positive or Single ended I/O.
C31	PL_G18_LVDS69_L10N_QBC	IO_L10N_T1U_N7_QBC_AD4N_69	69	G18	IO, 1.8V	PL Bank69 IO10 differential negative. Same pin can be configured as PLSYSMON differential analog input4 negative or Single ended I/O.
C32	PL_P19_LVDS69_L4P_DBC	IO_L4P_T0U_N6_DBC_AD7P_69	69	P19	IO, 1.8V	PL Bank69 IO4 differential positive. Same pin can be configured as PLSYSMON differential analog input7 positive or Single ended I/O.
C33	PL_N18_LVDS69_L4N_DBC	IO_L4N_T0U_N7_DBC_AD7N_69	69	N18	IO, 1.8V	PL Bank69 IO4 differential negative. Same pin can be configured as PLSYSMON differential analog input7 negative or Single ended I/O.
C34	PL_N20_LVDS69_L3P	IO_L3P_T0L_N4_AD15P_69	69	N20	IO, 1.8V	PL Bank69 IO3 differential positive. Same pin can be configured as PLSYSMON differential analog input15 positive or Single ended I/O.
C35	PL_N19_LVDS69_L3N	IO_L3N_T0L_N5_AD15N_69	69	N19	IO, 1.8V	PL Bank69 IO3 differential negative. Same pin can be configured as PLSYSMON differential analog input15 negative or Single ended I/O.
C37	PL_R17_LVDS69_L2P	IO_L2P_T0L_N2_69	69	R17	IO, 1.8V	PL Bank69 IO2 differential positive. Same pin can be configured as PLSYSMON differential analog input positive or Single ended I/O.
C38	PL_P17_LVDS69_L2N	IO_L2N_T0L_N3_69	69	P17	IO, 1.8V	PL Bank69 IO2 differential negative. Same pin can be configured as PLSYSMON differential analog input negative or Single ended I/O.

B2B-1 Pin No	B2B Connector1 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination*	Description
C39	PL_G21_LVDS69_L15P	IO_L15P_T2L_N4_AD11P_69	69	G21	IO, 1.8V	PL Bank69 IO15 differential positive. Same pin can be configured as PLSYSMON differential analog input11 positive or Single ended I/O.
C40	PL_F20_LVDS69_L15N	IO_L15N_T2L_N5_AD11N_69	69	F20	IO, 1.8V	PL Bank69 IO15 differential negative. Same pin can be configured as PLSYSMON differential analog input11 negative or Single ended I/O.
C41	PL_E17_LVDS69_L16P_QBC	IO_L16P_T2U_N6_QBC_AD3P_69	69	E17	IO, 1.8V	PL Bank69 IO16 differential positive. Same pin can be configured as PLSYSMON differential analog input3 positive or Single ended I/O.
C42	PL_D17_LVDS69_L16N_QBC	IO_L16N_T2U_N7_QBC_AD3N_69	69	D17	IO, 1.8V	PL Bank69 IO16 differential negative. Same pin can be configured as PLSYSMON differential analog input3 negative or Single ended I/O.
D30	PL_J18_LVDS69_L8P	IO_L8P_T1L_N2_AD5P_69	69	J18	IO, 1.8V	PL Bank69 IO8 differential positive. Same pin can be configured as PLSYSMON differential analog input5 positive or Single ended I/O.
D31	PL_J17_LVDS69_L8N	IO_L8N_T1L_N3_AD5N_69	69	J17	IO, 1.8V	PL Bank69 IO8 differential negative. Same pin can be configured as PLSYSMON differential analog input5 negative or Single ended I/O.
D32	PL_K21_LVDS69_L7P_QBC	IO_L7P_T1L_N0_QBC_AD13P_69	69	K21	IO, 1.8V	PL Bank69 IO7 differential positive. Same pin can be configured as PLSYSMON differential analog input13 positive or Single ended I/O.
D33	PL_K20_LVDS69_L7N_QBC	IO_L7N_T1L_N1_QBC_AD13N_69	69	K20	IO, 1.8V	PL Bank69 IO7 differential negative. Same pin can be configured as PLSYSMON differential analog input13 negative or Single ended I/O.
D34	PL_J19_LVDS69_L9P	IO_L9P_T1L_N4_AD12P_69	69	J19	IO, 1.8V	PL Bank69 IO9 differential positive. Same pin can be configured as PLSYSMON differential analog input12 positive or Single ended I/O.

B2B-1 Pin No	B2B Connector1 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination*	Description
D35	PL_H19_LVDS69_L9N	IO_L9N_T1L_N5_AD12N_69	69	H19	IO, 1.8V	PL Bank69 IO9 differential negative. Same pin can be configured as PLSYSMON differential analog input12 negative or Single ended I/O.
D41	PL_R20_LVDS69_L1P_DBC	IO_L1P_T0L_N0_DBC_69	69	R20	IO, 1.8V	PL Bank69 IO1 differential positive. Same pin can be configured as Single ended I/O.
D42	PL_R19_LVDS69_L1N_DBC	IO_L1N_T0L_N1_DBC_69	69	R19	IO, 1.8V	PL Bank69 IO1 differential negative. Same pin can be configured as Single ended I/O.

**IO Type of IOs originating from ZU29/39/49 RFSoC is configurable. Hence for exact IO type configuration options, refer Xilinx ZU29/39/49 RFSoC datasheet*

2.8.2.4 PL IOs – HD BANK84

The Zynq Ultrascale+ RFSoC SOM supports 12 DIFF IOs/24 Single Ended (SE) IOs on Board-to-Board Connector1 from RFSoC's PL High-Density (HD) Bank 84. Upon these 12 DIFF IOs/24 SE IOs, upto 4 HDGC Global Clock Inputs. upto 12 PLSYSMON auxiliary analog inputs are available.

The IO voltage of PL Bank 84 is connected from LDO4 output of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 1.2V to 3.3V through software. While using as DIFF IOs or Single Ended IOs, make sure to set the PMIC LDO4 to output appropriate IO voltage for PL Bank 84. By default, IO voltage of PL Bank84 is set as 1.2V and after U-boot bootup configurable to 1.8V. For more details about supported IO standard, refer the Zynq Ultrascale+ RFSoC datasheet.

In the Zynq Ultrascale+ RFSoC SOM, PL Bank 84 signals are routed as LVDS IOs to Board-to-Board Connector1. Even though PL Bank 84&87 signals are routed as DIFF IOs, these pins can be used as SE IOs if required. The Board-to-Board Connector1 pins A53, A54, C53, C54, D44, D45, D46 and D47 are HDGC Global Clock Input capable pins of PL Bank 84. Also, Board to Board Connector1 pins A51, A52, B51, B52, B53, B54, B55, B56, C51, C52, C55 and C56 are PLSYSMON auxiliary analog Input capable pins of PL Bank84.

Important Note: While changing the I/O voltage of PL Bank84, make sure to change the I/O standard of RFSoC Banks (Bank84, 87, & 88), since all are sharing the same I/O power rail from PMIC LDO4.

For more details on PL HD Bank 84 pinouts on Board-to-Board Connector1, refer the below table.

B2B-1 Pin No	B2B Connector1 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination*	Description
A51	PL_AR12_LVDS84_L9P	IO_L9P_AD3P_84	84	AR12	IO, 1.8V	PL Bank84 IO9 differential positive. Same pin can be configured as PLSYSMON differential analog input3 positive or Single ended I/O.
A52	PL_AT12_LVDS84_L9N	IO_L9N_AD3N_84	84	AT12	IO, 1.8V	PL Bank84 IO9 differential negative. Same pin can be configured as PLSYSMON differential analog input3 negative or Single ended I/O.
A53	PL_AV11_LVDS84_L5P_HDGC	IO_L5P_HDGC_AD7P_84	84	AV11	IO, 1.8V	PL Bank84 IO5 differential positive. Same pin can be configured as GC Global Clock Input differential positive or PLSYSMON differential analog input7 positive or Single ended I/O.

B2B-1 Pin No	B2B Connector1 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination*	Description
A54	PL_AW11_LVDS 84_L5N_HDGC	IO_L5N_HDGC _AD7N_84	84	AW11	IO, 1.8V	PL Bank84 IO5 differential negative. Same pin can be configured as GC Global Clock Input differential negative or PLSYSMON differential analog input7 negative or Single ended I/O.
A55	PL_BB11_LVDS8 4_L1P	IO_L1P_AD11P _84	84	BB11	IO, 1.8V	PL Bank84 IO1 differential positive. Same pin can be configured as PLSYSMON differential analog input11 positive or Single ended I/O.
A56	PL_BB10_LVDS8 4_L1N	IO_L1N_AD11 N_84	84	BB10	IO, 1.8V	PL Bank84 IO1 differential negative. Same pin can be configured as PLSYSMON differential analog input11 negative or Single ended I/O.
B51	PL_AP11_LVDS8 4_L12P	IO_L12P_AD0P _84	84	AP11	IO, 1.8V	PL Bank84 IO12 differential positive. Same pin can be configured as PLSYSMON differential analog input0 positive or Single ended I/O.
B52	PL_AP10_LVDS8 4_L12N	IO_L12N_AD0 N_84	84	AP10	IO, 1.8V	PL Bank84 IO12 differential ngataive. Same pin can be configured as PLSYSMON differential analog input0 negative or Single ended I/O.
B53	PL_AR10_LVDS8 4_L10P	IO_L10P_AD2P _84	84	AR10	IO, 1.8V	PL Bank84 IO10 differential positive. Same pin can be configured as PLSYSMON differential analog input2 positive or Single ended I/O.
B54	PL_AT10_LVDS8 4_L10N	IO_L10N_AD2 N_84	84	AT10	IO, 1.8V	PL Bank84 IO10 differential negative. Same pin can be configured as PLSYSMON differential analog input2 negative or Single ended I/O.
B55	PL_AP12_LVDS8 4_L11P	IO_L11P_AD1P _84	84	AP12	IO, 1.8V	PL Bank84 IO11 differential positive. Same pin can be configured as PLSYSMON differential analog input1 positive or Single ended I/O.
B56	PL_AR11_LVDS8 4_L11N	IO_L11N_AD1 N_84	84	AR11	IO, 1.8V	PL Bank84 IO11 differential negaative. Same pin can be configured as PLSYSMON differential analog input1 negative or Single ended I/O.

B2B-1 Pin No	B2B Connector1 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination*	Description
C51	PL_BA10_LVDS84_L2P	IO_L2P_AD10P_84	84	BA10	IO, 1.8V	PL Bank84 IO2 differential positive. Same pin can be configured as PLSYSMON differential analog input10 positive or Single ended I/O.
C52	PL_BB9_LVDS84_L2N	IO_L2N_AD10N_84	84	BB9	IO, 1.8V	PL Bank84 IO2 differential negative. Same pin can be configured as PLSYSMON differential analog input10 negative or Single ended I/O.
C53	PL_AV9_LVDS84_L6P_HDGC	IO_L6P_HDGC_AD6P_84	84	AV9	IO, 1.8V	PL Bank84 IO6 differential positive. Same pin can be configured as GC Global Clock Input differential positive or PLSYSMON differential analog input6 positive or Single ended I/O.
C54	PL_AW9_LVDS84_L6N_HDGC	IO_L6N_HDGC_AD6N_84	84	AW9	IO, 1.8V	PL Bank84 IO6 differential negative. Same pin can be configured as GC Global Clock Input differential negative or PLSYSMON differential analog input6 negative or Single ended I/O.
C55	PL_AY11_LVDS84_L4P	IO_L4P_AD8P_84	84	AY11	IO, 1.8V	PL Bank84 IO4 differential positive. Same pin can be configured as PLSYSMON differential analog input8 positive or Single ended I/O.
C56	PL_AY10_LVDS84_L4N	IO_L4N_AD8N_84	84	AY10	IO, 1.8V	PL Bank84 IO4 differential negative. Same pin can be configured as PLSYSMON differential analog input8 negative or Single ended I/O.
D51	PL_AU12_LVDS84_L8P_HDGC	IO_L8P_HDGC_AD4P_84	84	AU12	IO, 1.8V	PL Bank84 IO8 differential positive. Same pin can be configured as GC Global Clock Input differential positive or PLSYSMON differential analog input4 positive or Single ended I/O.
D52	PL_AU11_LVDS84_L8N_HDGC	IO_L8N_HDGC_AD4N_84	84	AU11	IO, 1.8V	PL Bank84 IO8 differential negative. Same pin can be configured as GC Global Clock Input differential negative or PLSYSMON differential analog input4 negative or Single ended I/O.

B2B-1 Pin No	B2B Connector1 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination*	Description
D53	PL_AU10_LVDS84_L7P_HDGC	IO_L7P_HDGC_AD5P_84	84	AU10	IO, 1.8V	PL Bank84 IO7 differential positive. Same pin can be configured as GC Global Clock Input differential positive or PLSYSMON differential analog input5 positive or Single ended I/O.
D54	PL_AV10_LVDS84_L7N_HDGC	IO_L7N_HDGC_AD5N_84	84	AV10	IO, 1.8V	PL Bank84 IO7 differential negative. Same pin can be configured as GC Global Clock Input differential negative or PLSYSMON differential analog input5 negative or Single ended I/O.
D55	PL_AY9_LVDS84_L3P	IO_L3P_AD9P_84	84	AY9	IO, 1.8V	PL Bank84 IO3 differential positive. Same pin can be configured as PLSYSMON differential analog input9 positive or Single ended I/O.
D56	PL_BA9_LVDS84_L3N	IO_L3N_AD9N_84	84	BA9	IO, 1.8V	PL Bank84 IO3 differential negative. Same pin can be configured as PLSYSMON differential analog inpu9 negative or Single ended I/O.

**IO Type of IOs originating from ZU29/39/49 RFSoC is configurable. Hence for exact IO type configuration options, refer Xilinx ZU29/39/49 RFSoC datasheet.*

2.8.2.5 PL IOs – HD BANK87

The Zynq Ultrascale+ RFSoC SOM supports 12 DIFF IOs/24 Single Ended (SE) IOs on Board-to-Board Connector1 from RFSoC's PL High-Density (HD) Bank87. Upon these 12 DIFF IOs/24 SE IOs, upto 4 HDGC Global Clock Inputs and upto 8 PLSYSMON auxiliary analog inputs are available.

The IO voltage of Bank87 is connected from LDO4 output of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 1.2V to 3.3V through software. While using as DIFF IOs or Single Ended IOs, make sure to set the PMIC LDO4 to output appropriate IO voltage for PL Bank87. By default, IO voltage of PL Bank87 is set as 1.2V and after U-boot bootup configurable to 1.8V. For more details about supported IO standard, refer the Zynq Ultrascale+ RFSoC datasheet.

In the Zynq Ultrascale+ RFSoC SOM, PL Bank87 signals are routed as DIFF IOs to Board-to-Board Connector1. Even though PL Bank87 signals are routed as DIFF IOs, these pins can be used as SE IOs if required. The Board-to-Board Connector1 pins A46, A47, A48, A49, B44, B45, B46 and B47 are HDGC Global Clock Input capable pins of PL Bank87. Also, Board to Board Connector1 pins A44, A45, B48, B49, C44, C45, C46, C47, C48, C49, D51, D52, D53, D54, D55 and D56 are PLSYSMON auxiliary analog Input capable pins of PL Bank87.

Important Note: While changing the I/O voltage of PL Bank87, make sure to change the I/O standard of RFSoC Banks (Bank84, 87, & 88), since all are sharing the same I/O power rail from PMIC LDO4.

For more details on PL HD Bank87 pinouts on Board-to-Board Connector1, refer the below table.

B2B-1 Pin No	B2B Connector1 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination*	Description
A44	PL_F14_LVDS87_L12P	IO_L12P_AD8P_87	87	F14	IO, 1.8V	PL Bank87 IO12 differential positive. Same pin can be configured as PLSYSMON differential analog input8 positive or Single ended I/O.
A45	PL_F13_LVDS87_L12N	IO_L12N_AD8N_87	87	F13	IO, 1.8V	PL Bank87 IO12 differential negative. Same pin can be configured as PLSYSMON differential analog input8 negative or Single ended I/O.
A46	PL_B16_LVDS87_L8P_HDGC	IO_L8P_HDGC_87	87	B16	IO, 1.8V	PL Bank87 IO8 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
A47	PL_B15_LVDS87_L8N_HDGC	IO_L8N_HDGC_87	87	B15	IO, 1.8V	PL Bank87 IO8 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.

B2B-1 Pin No	B2B Connector1 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination*	Description
A48	PL_C15_LVDS87_L7P_HDGC	IO_L7P_HDGC_87	87	C15	IO, 1.8V	PL Bank87 IO7 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
A49	PL_C14_LVDS87_L7N_HDGC	IO_L7N_HDGC_87	87	C14	IO, 1.8V	PL Bank87 IO7 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
B44	PL_A13_LVDS87_L5P_HDGC	IO_L5P_HDGC_87	87	A13	IO, 1.8V	PL Bank87 IO5 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
B45	PL_A12_LVDS87_L5N_HDGC	IO_L5N_HDGC_87	87	A12	IO, 1.8V	PL Bank87 IO5 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
B46	PL_F15_LVDS87_L6P_HDGC	IO_L6P_HDGC_87	87	F15	IO, 1.8V	PL Bank87 IO6 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
B47	PL_E14_LVDS87_L6N_HDGC	IO_L6N_HDGC_87	87	E14	IO, 1.8V	PL Bank87 IO6 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
B48	PL_A15_LVDS87_L11P	IO_L11P_AD9P_87	87	A15	IO, 1.8V	PL Bank87 IO11 differential positive. Same pin can be configured as PLSYSMON differential analog input9 positive or Single ended I/O.
B49	PL_A14_LVDS87_L11N	IO_L11N_AD9N_87	87	A14	IO, 1.8V	PL Bank87 IO11 differential negative. Same pin can be configured as PLSYSMON differential analog input9 negative or Single ended I/O.
C44	PL_D13_LVDS87_L2P	IO_L2P_AD14P_87	87	D13	IO, 1.8V	PL Bank87 IO2 differential positive. Same pin can be configured as PLSYSMON differential analog input14 positive or Single ended I/O.
C45	PL_D12_LVDS87_L2N	IO_L2N_AD14N_87	87	D12	IO, 1.8V	PL Bank87 IO2 differential negative. Same pin can be configured as PLSYSMON differential analog input14 negative or Single ended I/O.

B2B-1 Pin No	B2B Connector1 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination*	Description
C46	PL_D14_LVDS87_L3P	IO_L3P_AD13P_87	87	D14	IO, 1.8V	PL Bank87 IO3 differential positive. Same pin can be configured as PLSYSMON differential analog input13 positive or Single ended I/O.
C47	PL_C13_LVDS87_L3N	IO_L3N_AD13N_87	87	C13	IO, 1.8V	PL Bank87 IO3 differential negative. Same pin can be configured as PLSYSMON differential analog input13 negative or Single ended I/O.
C48	PL_B13_LVDS87_L4P	IO_L4P_AD12P_87	87	B13	IO, 1.8V	PL Bank87 IO4 differential positive. Same pin can be configured as PLSYSMON differential analog input12 positive or Single ended I/O.
C49	PL_B12_LVDS87_L4N	IO_L4N_AD12N_87	87	B12	IO, 1.8V	PL Bank87 IO4 differential negative. Same pin can be configured as PLSYSMON differential analog input12 negative or Single ended I/O.
D44	PL_D16_LVDS87_L10P	IO_L10P_AD10P_87	87	D16	IO, 1.8V	PL Bank87 IO10 differential positive. Same pin can be configured as PLSYSMON differential analog input10 positive or Single ended I/O.
D45	PL_C16_LVDS87_L10N	IO_L10N_AD10N_87	87	C16	IO, 1.8V	PL Bank87 IO10 differential negative. Same pin can be configured as PLSYSMON differential analog input10 negative or Single ended I/O.
D46	PL_E16_LVDS87_L9P	IO_L9P_AD11P_87	87	E16	IO, 1.8V	PL Bank87 IO9 differential positive. Same pin can be configured as PLSYSMON differential analog input11 positive or Single ended I/O.
D47	PL_E15_LVDS87_L9N	IO_L9N_AD11N_87	87	E15	IO, 1.8V	PL Bank87 IO9 differential negative. Same pin can be configured as PLSYSMON differential analog input11 negative or Single ended I/O.
D48	PL_F12_LVDS87_L1P	IO_L1P_AD15P_87	87	F12	IO, 1.8V	PL Bank87 IO1 differential positive. Same pin can be configured as PLSYSMON differential analog input15 positive or Single ended I/O.
D49	PL_E12_LVDS87_L1N	IO_L1N_AD15N_87	87	E12	IO, 1.8V	PL Bank87 IO1 differential negative. Same pin can be configured as PLSYSMON differential analog input15 negative or Single ended I/O.

**IO Type of IOs originating from ZU29/39/49 RFSoC is configurable. Hence for exact IO type configuration options, refer Xilinx ZU29/39/49 RFSoC datasheet.*

2.8.3 Power Control Input

The Zynq Ultrascale+ RFSoC SOM Board to Board Connector1 is assigned with HP and HD IO voltage for HP and HD Bank IOs connected to the connector. Also, in Board-to-Board Connector1, Ground pins are distributed throughout the connector for better performance. For more details on Power control & Ground pins on Board-to-Board Connector1, refer the below table.

B2B-1 Pin No	B2B Connector1 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination	Description
A1	VCCO_HDB	NA	NA	NA	1.8V	HD Bank IO Voltage
B1, C1, D1	VCCO_HPB	NA	NA	NA	1.8V	HP Bank IO Voltage
A8, A15, A22, A29, A36, A43, A50, A57, A58, A61, A62, A65, A66, A69, A70, A73, A74, A77, A78, A81, A82, A85, A86, A89, A90, A93, A94, A97, A98, A99, A100, B8, B15, B22, B29, B36, B43, B50, B57, B58, B61, B62, B65, B66, B69, B70, B73, B74, B77, B78, B81, B82, B85, B86, B89, B90, B93, B94, B97, B98 C8, C15, C22, C29, C36, C43, C50, C57, C58, C59, C60, C61, C62, C65, C66, C69, C70, C73, C74, C77, C78, C81, C82, C85, C86, C89, C90,C93,C94,C95 C96,C97,C98,C99,C100, D8, D15, D22, D29, D36, D43, D50, D57, D58, D59, D60, D61, D62, D65, D66, D69, D70, D73, D74, D77, D78, D81, D82, D85, D86, D89, D90, D93, D94, D95, D96, D97, D98,	GND	NA	NA	NA	Power	Ground.

2.9 Board to Board Connector2

The Zynq Ultrascale+ RFSoC SOM Board to Board connector2 pinout is provided in the below table and the interfaces which are available at Board-to-Board Connector2 are explained in the following sections. The Board-to-Board Connector2 (J5) is physically located on bottom side of the SOM as shown below.

Number of Pins - 400

Connector Part Number - ASP-209946-01 from Samtech

Mating Connector - ASP-214802-01 from Samtech

Staking Height - 5mm

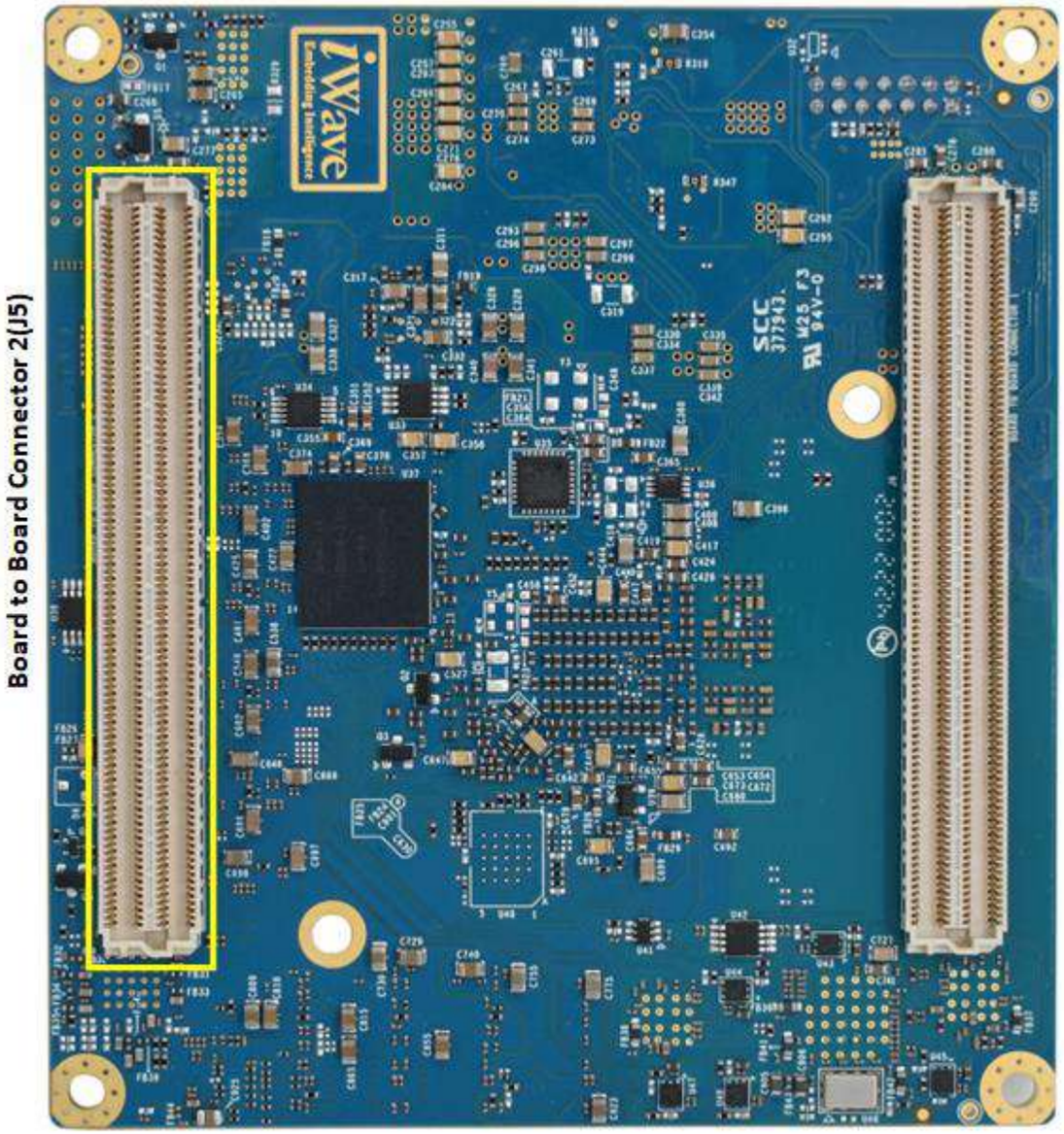


Figure 9: Board to Board Connector2

Table 12: Board to Board Connector2 Pinout

B2B-2 Pin	Signal Name	B2B-2 Pin	Signal Name	B2B-2 Pin	Signal Name	B2B-2 Pin	Signal Name
A1	VCC_12V	B1	VCC_12V	C1	VCC_12V	D1	VCC_12V
A2	VCC_12V	B2	VCC_12V	C2	VCC_12V	D2	VCC_12V
A3	VCC_12V	B3	VCC_12V	C3	VCC_12V	D3	VCC_12V
A4	VCC_12V	B4	VCC_12V	C4	VCC_12V	D4	VCC_12V
A5	VCC_12V	B5	VCC_12V	C5	VCC_12V	D5	VCC_12V
A6	VCC_12V	B6	VCC_12V	C6	VCC_12V	D6	VCC_12V
A7	VCC_12V	B7	VCC_12V	C7	VCC_12V	D7	VCC_12V
A8	VCC_12V	B8	VCC_12V	C8	VCC_12V	D8	VCC_12V
A9	GND	B9	GND	C9	GND	D9	GND
A10	GND	B10	GND	C10	GND	D10	GND
A11	NC	B11	SOMPWR_EN	C11	NC	D11	10MHz_EX_OUT
A12	PS_JTAG_TCK	B12	SOM_PWR_OK	C12	VRTC_3V0	D12	1PPS_EX_OUT
A13	PS_JTAG_TMS	B13	GPIO_PS_RST_OUT (PS_MIO42_501)	C13	PS_MODE0	D13	GND
A14	PS_JTAG_TDO	B14	RESET_SW_IN	C14	PS_MODE1	D14	PS_MIO41_501
A15	PS_JTAG_TDI	B15	FPGA_CONFIG_DONE	C15	PS_MODE2	D15	NC
A16	GND	B16	GND	C16	GND	D16	GND
A17	SD1_CLK(PS_MIO51_501)	B17	NC	C17	GEM3_TX_CLK/USB1_CLK(PS_MIO64_502)	D17	GEM3_RX_CLK/USB1_STP(PS_MIO70_502)
A18	SD1_CMD(PS_MIO50_501)	B18	NC	C18	GEM3_TXD0/USB1_DIR(PS_MIO65_502)	D18	GEM3_RXD0/USB1_DATA3(PS_MIO71_502)
A19	SD1_DATA0(PS_MIO46_501)	B19	NC	C19	GEM3_TXD1/USB1_DATA2(PS_MIO66_502)	D19	GEM3_RXD1/USB1_DATA4(PS_MIO72_502)
A20	SD1_DATA1(PS_MIO47_501)	B20	NC	C20	GEM3_TXD2/USB1_NXT(PS_MIO67_502)	D20	GEM3_RXD2/USB1_DATA5(PS_MIO73_502)
A21	SD1_DATA2(PS_MIO48_501)	B21	NC	C21	GEM3_TXD3/USB1_DATA0(PS_MIO68_502)	D21	GEM3_RXD3/USB1_DATA6(PS_MIO74_502)
A22	SD1_DATA3(PS_MIO49_501)	B22	NC	C22	GEM3_TX_CTL/USB1_DATA1 (PS_MIO69_502)	D22	GEM3_RX_CTL/USB1_DATA7(PS_MIO75_502)
A23	GND	B23	GND	C23	GND	D23	GND

B2B-2 Pin	Signal Name	B2B-2 Pin	Signal Name	B2B-2 Pin	Signal Name	B2B-2 Pin	Signal Name
A24	SD1_CD(PS_MIO45_501)	B24	SD1_WP(PS_MIO44_501)	C24	GEM0_MDC(PS_MIO76_502)	D24	CAN0_RX(PS_MIO38_501)
A25	SD1_PWR(PS_MIO43_501)	B25	10MHz_EX_IN	C25	GEM0_MDIO(PS_MIO77_502)	D25	CAN0_TX(PS_MIO39_501)
A26	I2C0_SCL(PS_MIO10_500)	B26	1PPS_EX_IN	C26	B_PCIe_RSTn	D26	NC
A27	I2C0_SDA(PS_MIO11_500)	B27	UART1_TX(PS_MIO08_500)	C27	PS_MIO40_501	D27	NC
A28	I2C1_SCL(PS_MIO24_500)	B28	UART1_RX(PS_MIO09_500)	C28	GND	D28	GND
A29	I2C1_SDA(PS_MIO25_500)	B29	NC	C29	PS_MGTRTXP0_505	D29	PS_MGTRRXP0_505
A30	UART0_TX(PS_MIO07_500)	B30	NC	C30	PS_MGTRTXN0_505	D30	PS_MGTRRXN0_505
A31	UART0_RX(PS_MIO06_500)	B31	VBUS_USB	C31	GND	D31	GND
A32	GPHY_ACTIVITY_LED1	B32	USB_PWR_EN	C32	PS_MGTRTXP1_505	D32	PS_MGTRRXP1_505
A33	GPHY_LINK_LED2	B33	USB_OTG_ID	C33	PS_MGTRTXN1_505	D33	PS_MGTRRXN1_505
A34	GND	B34	GND	C34	GND	D34	GND
A35	GPHY_DTXRXM	B35	USB_OTG_DM	C35	PS_MGTRTXP2_505	D35	PS_MGTRRXP2_505
A36	GPHY_DTXRXP	B36	USB_OTG_DP	C36	PS_MGTRTXN2_505	D36	PS_MGTRRXN2_505
A37	GND	B37	GND	C37	GND	D37	GND
A38	GPHY_CTXRXM	B38	NC	C38	PS_MGTRTXP3_505	D38	PS_MGTRRXP3_505
A39	GPHY_CTXRXP	B39	NC	C39	PS_MGTRTXN3_505	D39	PS_MGTRRXN3_505
A40	GND	B40	GND	C40	GND	D40	GND
A41	GPHY_BTXRXM	B41	SYS_SYNC_CLK_OUTp	C41	PS_MGTREFCLK0P_505	D41	PS_MGTREFCLK1P_505
A42	GPHY_BTXRXP	B42	SYS_SYNC_CLK_OUTn	C42	PS_MGTREFCLK0N_505	D42	PS_MGTREFCLK1N_505
A43	GND	B43	GND	C43	GND	D43	GND
A44	GPHY_ATXRXM	B44	SYS_SYNC_CLK_INp	C44	B2B_PS_MGTREFCLK2P_505	D44	PS_MGTREFCLK3P_505
A45	GPHY_ATXRXP	B45	SYS_SYNC_CLK_INn	C45	B2B_PS_MGTREFCLK2N_505	D45	PS_MGTREFCLK3N_505
A46	GND	B46	GND	C46	GND	D46	GND
A47	GTYTXP0_130	B47	GTYRXP0_130	C47	GTYTXP0_131	D47	GTYRXP0_131
A48	GTYTXN0_130	B48	GTYRXN0_130	C48	GTYTXN0_131	D48	GTYRXN0_131
A49	GND	B49	GND	C49	GND	D49	GND
A50	GTYTXP1_130	B50	GTYRXP1_130	C50	GTYTXP1_131	D50	GTYRXP1_131
A51	GTYTXN1_130	B51	GTYRXN1_130	C51	GTYTXN1_131	D51	GTYRXN1_131
A52	GND	B52	GND	C52	GND	D52	GND

B2B-2 Pin	Signal Name	B2B-2 Pin	Signal Name	B2B-2 Pin	Signal Name	B2B-2 Pin	Signal Name
A53	GTYTXP2_130	B53	GTYRXP2_130	C53	GTYTXP2_131	D53	GTYRXP2_131
A54	GTYTXN2_130	B54	GTYRXN2_130	C54	GTYTXN2_131	D54	GTYRXN2_131
A55	GND	B55	GND	C55	GND	D55	GND
A56	GTYTXP3_130	B56	GTYRXP3_130	C56	GTYTXP3_131	D56	GTYRXP3_131
A57	GTYTXN3_130	B57	GTYRXN3_130	C57	GTYTXN3_131	D57	GTYRXN3_131
A58	GND	B58	GND	C58	GND	D58	GND
A59	GTREFCLK0P_130	B59	B2B_GTREFCLK1P_130	C59	GTREFCLK0P_131	D59	B2B_GTREFCLK1P_131
A60	GTREFCLK0N_130	B60	B2B_GTREFCLK1N_130	C60	GTREFCLK0N_131	D60	B2B_GTREFCLK1N_131
A61	GND	B61	GND	C61	GND	D61	GND
A62	GTYTXP0_128	B62	GTYRXP0_128	C62	GTYTXP0_129	D62	GTYRXP0_129
A63	GTYTXN0_128	B63	GTYRXN0_128	C63	GTYTXN0_129	D63	GTYRXN0_129
A64	GND	B64	GND	C64	GND	D64	GND
A65	GTYTXP1_128	B65	GTYRXP1_128	C65	GTYTXP1_129	D65	GTYRXP1_129
A66	GTYTXN1_128	B66	GTYRXN1_128	C66	GTYTXN1_129	D66	GTYRXN1_129
A67	GND	B67	GND	C67	GND	D67	GND
A68	GTYTXP2_128	B68	GTYRXP2_128	C68	GTYTXP2_129	D68	GTYRXP2_129
A69	GTYTXN2_128	B69	GTYRXN2_128	C69	GTYTXN2_129	D69	GTYRXN2_129
A70	GND	B70	GND	C70	GND	D70	GND
A71	GTYTXP3_128	B71	GTYRXP3_128	C71	GTYTXP3_129	D71	GTYRXP3_129
A72	GTYTXN3_128	B72	GTYRXN3_128	C72	GTYTXN3_129	D72	GTYRXN3_129
A73	GND	B73	GND	C73	GND	D73	GND
A74	GTREFCLK0P_128	B74	B2B_GTREFCLK1P_128	C74	GTREFCLK0P_129	D74	B2B_GTREFCLK1P_129
A75	GTREFCLK0N_128	B75	B2B_GTREFCLK1N_128	C75	GTREFCLK0N_129	D75	B2B_GTREFCLK1N_129
A76	GND	B76	GND	C76	GND	D76	GND
A77	NC	B77	NC	C77	NC	D77	NC
A78	NC	B78	NC	C78	NC	D78	NC
A79	GND	B79	GND	C79	GND	D79	GND
A80	NC	B80	NC	C80	NC	D80	NC
A81	NC	B81	NC	C81	NC	D81	NC
A82	GND	B82	GND	C82	GND	D82	GND
A83	NC	B83	NC	C83	NC	D83	NC

B2B-2 Pin	Signal Name	B2B-2 Pin	Signal Name	B2B-2 Pin	Signal Name	B2B-2 Pin	Signal Name
A84	NC	**B84**	NC	**C84**	NC	**D84**	NC
A85	GND	**B85**	GND	**C85**	GND	**D85**	GND
A86	NC	**B86**	NC	**C86**	NC	**D86**	NC
A87	NC	**B87**	NC	**C87**	NC	**D87**	NC
A88	GND	**B88**	GND	**C88**	GND	**D88**	GND
A89	NC	**B89**	NC	**C89**	NC	**D89**	NC
A90	NC	**B90**	NC	**C90**	NC	**D90**	NC
A91	GND	**B91**	GND	**C91**	GND	**D91**	GND
A92	NC	**B92**	NC	**C92**	NC	**D92**	NC
A93	NC	**B93**	NC	**C93**	NC	**D93**	NC
A94	GND	**B94**	GND	**C94**	GND	**D94**	GND
A95	NC	**B95**	NC	**C95**	NC	**D95**	NC
A96	NC	**B96**	NC	**C96**	NC	**D96**	NC
A97	GND	**B97**	GND	**C97**	GND	**D97**	GND
A98	NC	**B98**	NC	**C98**	NC	**D98**	NC
A99	NC	**B99**	NC	**C99**	NC	**D99**	NC
A100	GND	**B100**	GND	**C100**	GND	**D100**	GND

- RED: Power Rails
- Purple: Clock signals
- Brown: Optional signals

2.9.1 PS Interfaces

The interfaces which are supported in Board-to-Board Conenector2 from Zynq Ultrascale+ RFSoC's PS is explained in the following section.

2.9.1.1 PS-GTR Transceivers

The Zynq Ultrascale+ RFSoC supports four Multi-Gigabit PS-GTR transceivers with data rate from 1.25Gbps to 6.0Gbps. This PS-GTR transceiver lanes provide I/O path for RFSoC MAC controllers and their link partner outside. At any given time, these four lanes can be used for any of below mentioned peripheral standards.

- x1, x2, or x4 lane of PCIe at Gen1 (2.5Gb/s) or Gen2 (5.0Gb/s) rates
- 1 or 2 lanes of DisplayPort (TX only) at 1.62Gb/s, 2.7Gb/s, or 5.4Gb/s
- 1 or 2 SATA channels at 1.5Gb/s, 3.0Gb/s, or 6.0Gb/s
- 1 or 2 USB3.0 channels at 5.0Gb/s
- 1-4 Ethernet SGMII channels at 1.25Gb/s

The available peripheral standard option for each PS-GTR transceiver lane in Zynq Ultrascale+ RFSoC is shown below. This is user programmable via the high-speed I/O multiplexer (HS-MIO) of RFSoC.

PS Peripheral Interface	Lane0	Lane1	Lane2	Lane3
PCIe (x1, x2 or x4)	PCIe0	PCIe1	PCIe2	PCIe3
SATA (1 or 2 channels)	SATA0	SATA1	SATA0	SATA1
DisplayPort (TX only)	DP1	DP0	DP1	DP0
USB0	USB0	USB0	USB0	-
USB1	-	-	-	USB1
SGMII0	SGMII0	-	-	-
SGMII1	-	SGMII1	-	-
SGMII2	-	-	SGMII2	-
SGMII3	-	-	-	SGMII3

The Zynq Ultrascale+ RFSoC SOM supports four PS GTR transceivers (Lane0, Lane1, Lane3 & Lane4) on Board-to-Board Connector2. Each PS GTR transceiver lane supports one dedicated reference clock input pair with the ability to share reference clocks between lanes.

In Zynq Ultrascale+ RFSoC SOM, the end user is responsible for sourcing the reference clocks to the PS-GTR lanes through Board-to-Board Connector2. This gives full flexibility to end user to select the required peripheral standards on PS-GTR lanes.

For more details on PS-GTR transceiver pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination	Description
PS-GTR Lane0 Pins						
C29	PS_MGTRTXP0_505	PS_MGTRTXP0_505	505	AH35	O, DIFF	PS-GTR Lane0 High speed differential transmitter positive.
C30	PS_MGTRTXN0_505	PS_MGTRTXN0_505	505	AH36	O, DIFF	PS-GTR Lane0 High speed differential transmitter negative.
D29	PS_MGTRRXP0_505	PS_MGTRRXP0_505	505	AJ41	I, DIFF	PS-GTR Lane0 High speed differential receiver positive.
D30	PS_MGTRRXN0_505	PS_MGTRRXN0_505	505	AJ42	I, DIFF	PS-GTR Lane0 High speed differential receiver negative.
C41	PS_MGTREFCLK0P_505	PS_MGTREFCLK0P_505	505	AF34	I, DIFF	PS-GTR Lane0 differential reference clock positive.
C42	PS_MGTREFCLK0N_505	PS_MGTREFCLK0N_505	505	AF35	I, DIFF	PS-GTR Lane0 differential reference clock negative.
PS-GTR Lane1 Pins						
C32	PS_MGTRTXP1_505	PS_MGTRTXP1_505	505	AG37	O, DIFF	PS-GTR Lane1 High speed differential transmitter positive.
C33	PS_MGTRTXN1_505	PS_MGTRTXN1_505	505	AG38	O, DIFF	PS-GTR Lane1 High speed differential transmitter negative.
D32	PS_MGTRRXP1_505	PS_MGTRRXP1_505	505	AH39	I, DIFF	PS-GTR Lane1 High speed differential receiver positive.
D33	PS_MGTRRXN1_505	PS_MGTRRXN1_505	505	AH40	I, DIFF	PS-GTR Lane1 High speed differential receiver negative.
D41	PS_MGTREFCLK1P_505	PS_MGTREFCLK1P_505	505	AD34	I, DIFF	PS-GTR Lane1 differential reference clock positive.
D42	PS_MGTREFCLK1N_505	PS_MGTREFCLK1N_505	505	AD35	I, DIFF	PS-GTR Lane1 differential reference clock negative.
PS-GTR Lane2 Pins						
C35	PS_MGTRTXP2_505	PS_MGTRTXP2_505	505	AF39	O, DIFF	PS-GTR Lane2 High speed differential transmitter positive.
C36	PS_MGTRTXN2_505	PS_MGTRTXN2_505	505	AF40	O, DIFF	PS-GTR Lane2 High speed differential transmitter negative.
D35	PS_MGTRRXP2_505	PS_MGTRRXP2_505	505	AG41	I, DIFF	PS-GTR Lane2 High speed differential receiver positive.
D36	PS_MGTRRXN2_505	PS_MGTRRXN2_505	505	AG42	I, DIFF	PS-GTR Lane2 High speed differential receiver negative.
C44	B2B_PS_MGTREFCLK2P_505	PS_MGTREFCLK2P_505	505	AC36	I, DIFF	NC *Optionally connected to PS-GTR Lane2 differential reference clock positive through Zero Ohm resistors*.

B2B-2 Pin No	B2B Connector2 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination	Description
C45	B2B_PS_MGTREFCLK2N_505	PS_MGTREFCLK2N_505	505	AC37	I, DIFF	NC *Optionally connected to PS-GTR Lane2 differential reference clock negative. through Zero Ohm resistors*.
PS-GTR Lane3 Pins						
C38	PS_MGTRTXP3_505	PS_MGTRTXP3_505	505	AE37	O, DIFF	PS-GTR Lane3 High speed differential transmitter positive.
C39	PS_MGTRTXN3_505	PS_MGTRTXN3_505	505	AE38	O, DIFF	PS-GTR Lane3 High speed differential transmitter negative.
D38	PS_MGTRRXP3_505	PS_MGTRRXP3_505	505	AE41	I, DIFF	PS-GTR Lane3 High speed differential receiver positive.
D39	PS_MGTRRXN3_505	PS_MGTRRXN3_505	505	AE42	I, DIFF	PS-GTR Lane3 High speed differential receiver negative.
D44	PS_MGTREFCLK3P_505	PS_MGTREFCLK3P_505	505	AB34	I, DIFF	PS-GTR Lane3 differential reference clock positive.
D45	PS_MGTREFCLK3N_505	PS_MGTREFCLK3N_505	505	AB35	I, DIFF	PS-GTR Lane3 differential reference clock negative.

2.9.1.2 Gigabit Ethernet Interface

The Zynq Ultrascale+ RFSoC SOM supports one 10/100/1000 Mbps Ethernet interface on Board-to-Board Connector2.The MAC is integrated in the Zynq Ultrascale+ RFSoC PS and connected to the external Gigabit Ethernet PHY "RTL8211FI-VD-CG" on SOM. This Gigabit Ethernet PHY is interfaced with GEM0 interface of RFSoC's PS through MIO pins and works at 1.8V IO voltage level.

In Zynq Ultrascale+ RFSoC SOM, PS GPIO "PS_MIO42_501" is used for Ethernet PHY reset and also shared with USB ULPI PHY reset. Also, SOM supports Ethernet PHY interrupt through PS GPIO "PS_MIO12_500". This PHY supports active high Link and Activity LED indication signals and available on Board-to-Board Connector2. Since MAC and PHY are supported on SOM itself, only Magnetics is required on the carrier board.

For more details on Gigabit Ethernet Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination	Description
A35	GPHY_DTXRXM	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 4 negative.
A36	GPHY_DTXRXP	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 4 positive.
A38	GPHY_CTXRXM	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 3 negative.
A39	GPHY_CTXRXP	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 3 positive.

B2B-2 Pin No	B2B Connector2 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination	Description
A41	GPHY_BTXRXM	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 2 negative.
A42	GPHY_BTXRXP	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 2 positive.
A44	GPHY_ATXRXM	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 1 negative.
A45	GPHY_ATXRXP	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 1 positive.
A32	GPHY_ACTIVITY_LED1	NA	NA	NA	O, GBE	Gigabit Ethernet Activity LED (Active High).
A33	GPHY_LINK_LED2	NA	NA	NA	O, GBE	Gigabit Ethernet 1000Mbps Link status LED (Active High).

2.9.1.3 USB2.0 OTG Interface

The Zynq Ultrascale+ RFSoC SOM supports one USB2.0 OTG interface on Board-to-Board Connector2. USB0 OTG controller of Zynq Ultrascale+ RFSoC PS is used for USB2.0 OTG interface. The USB OTG controller is capable of fulfilling a wide range of applications for USB2.0 implementations as a host, a device or On-the-Go. Also, this controller supports all high-speed, full-speed and low-speed transfers in both device and host modes. While using USB3.0 interface through PS-GTR, this USB2.0 OTG interface will co-work with USB3.0 interface.

The USB OTG controller uses the ULPI protocol to connect external ULPI PHY via the MIO pins. The Zynq Ultrascale+ RFSoC SOM supports “USB3320” ULPI transceiver from Microchip and works at 1.8V IO voltage level. In Zynq Ultrascale+ RFSoC SOM, PS GPIO “PS_MIO42_501” is used for USB ULPI PHY reset and also shared with Gigabit Ethernet PHY reset. It supports active high power enable signal on Board-to-Board Connector2 from USB PHY for external VBUS power control.

Also, Zynq Ultrascale+ RFSoC SOM supports USB ID & USB VBUS inputs from Board-to-Board Connector2 and connected to USB PHY for USB Host/Device detection & VBUS monitoring respectively. If USB ID pin is grounded, then USB Host is detected and if it is floated, USB device is detected.

For more details on USB2.0 OTG Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination	Description
B35	USB_OTG_DM	NA	NA	NA	IO, USB	USB OTG data negative.
B36	USB_OTG_DP	NA	NA	NA	IO, USB	USB OTG data positive.
B32	USB_PWR_EN	NA	NA	NA	O,3.3V CMOS	USB active high power enable output to control external USB Vbus.
B33	USB_OTG_ID	NA	NA	NA	I, 3.3V CMOS	USB OTG ID input for USB host or device detection.
B31	VBUS_USB	NA	NA	NA	I, 5V Power	USB VBUS for VBUS monitoring.

2.9.1.4 RGMII/ULPI Interface

The Zynq Ultrascale+ RFSoC SOM supports RGMII or ULPI interface on Board-to-Board Connector2. In Zynq Ultrascale+ RFSoC PS, GEM3 RGMII interface and USB1 ULPI interface are multiplexed on the same pins. So, either one interface only can be used at a time. In Zynq Ultrascale+ RFSoC SOM, these MIO pins are directly connected from RFSoC to Board-to-Board conenctor2. If RGMII/ULPI interface is not required on these pins, the same pins can be used as GPIOs or other alternate functions. Please refer PS Min Multiplexing section **2.10** for available alternate functions.

The Zynq Ultrascale+ RFSoC gigabit Ethernet controller (GEM) implements a 10/100/1000 Mb/s Ethernet MAC that is compatible with the IEEE Standard for Ethernet (IEEE Std 802.3-2008). GEM controller supports MDIO interface for external PHY Management and it can be used through any PL Bank IOs through EMIO interface in SOM.

The Zynq Ultrascale+ RFSoC USB2.0 OTG controller is capable for USB2.0 implementations as a host, a device, or On-the-Go. This controller uses the ULPI protocol to connect external ULPI PHY. Also, this controller supports all high-speed, full-speed and low-speed transfers in both device and host modes.

For more details on RGMII/ULPI Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-1 Pin No	B2B Connector2 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type*/ Termination	Description
C17	GEM3_TX_CLK/USB1_CLK(PS_MIO64_502)	PS_MIO64_502	502	U30	O, 1.8V LVCMOS	GEM3 RGMII Transmit Clock. Or USB1 ULPI Clock.
C18	GEM3_TXD0/USB1_DIR (PS_MIO65_502)	PS_MIO65_502	502	V30	O, 1.8V LVCMOS	GEM3 RGMII Transmit DATA0. Or USB1 ULPI Direction Control.
C19	GEM3_TXD1/USB1_DATA2(PS_MIO66_502)	PS_MIO66_502	502	V29	O, 1.8V LVCMOS	GEM3 RGMII Transmit DATA1. Or USB1 ULPI Bi-Directional Data2.
C20	GEM3_TXD2/USB1_NXT(PS_MIO67_502)	PS_MIO67_502	502	W28	O, 1.8V LVCMOS	GEM3 RGMII Transmit DATA2. Or USB1 ULPI NXT.
C21	GEM3_TXD3/USB1_DATA0(PS_MIO68_502)	PS_MIO68_502	502	Y29	O, 1.8V LVCMOS	GEM3 RGMII Transmit DATA3. Or USB1 ULPI Bi-Directional Data0.
C22	GEM3_TX_CTL/USB1_DATA1(PS_MIO69_502)	PS_MIO69_502	502	W29	O, 1.8V LVCMOS	GEM3 RGMII Transmit Control. Or USB1 ULPI Bi-Directional Data1.
D17	GEM3_RX_CLK/USB1_STP(PS_MIO70_502)	PS_MIO70_502	502	AA28	I, 1.8V LVCMOS	GEM3 RGMII Receive Clock. Or USB1 ULPI STP.
D18	GEM3_RXD0/USB1_DATA3(PS_MIO71_502)	PS_MIO71_502	502	AB28	I, 1.8V LVCMOS	GEM3 RGMII Receive DATA0. Or USB1 ULPI Bi-Directional Data3.

B2B-1 Pin No	B2B Connector2 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type*/ Termination	Description
D19	GEM3_RXD1/USB1_DATA4(PS_MIO72_502)	PS_MIO72_502	502	AC28	I, 1.8V LVCMOS	GEM3 RGMII Receive DATA1. Or USB1 ULPI Bi-Directional Data4.
D20	GEM3_RXD2/USB1_DATA5(PS_MIO73_502)	PS_MIO73_502	502	AA29	I, 1.8V LVCMOS	GEM3 RGMII Receive DATA2. Or USB1 ULPI Bi-Directional Data5.
D21	GEM3_RXD3/USB1_DATA6(PS_MIO74_502)	PS_MIO74_502	502	Y30	I, 1.8V LVCMOS	GEM3 RGMII Receive DATA3. Or USB1 ULPI Bi-Directional Data6.
D22	GEM3_RX_CTL/USB1_DATA7(PS_MIO75_502)	PS_MIO75_502	502	AC29	I, 1.8V LVCMOS	GEM3 RGMII Receive control. Or USB1 ULPI Bi-Directional Data7.
C24	GEM0_MDC(PS_MIO76_502)	PS_MIO76_502	502	AB30	O, 1.8V LVCMOS	GEM0 MDC. *Same MDC signal is shared to on SOM GEM0 Ethernet PHY.*
C25	GEM0_MDIO(PS_MIO77_502)	PS_MIO77_502	502	AA30	IO, 1.8V LVCMOS	GEM0 MDIO. *Same MDIO signal is shared to on SOM GEM0 Ethernet PHY.*

** Signal direction is mentioned with respect to GEM3 Interface.*

2.9.1.5 CAN Interface

The Zynq Ultrascale+ RFSoC SOM supports one CAN interfaces on Board-to-Board Connector2. The CAN0 controller of RFSoC's PS is used for CAN interface through MIO pins. This CAN controller is compatible with the ISO 11898-1, CAN 2.0A, and CAN 2.0B standards. And it supports bit rates up to 1Mb/s.

If CAN interface is not required on these pins, the same pins can be used as GPIOs or other alternate functions. Please refer PS Min Multiplexing section **2.10** for available alternate functions.

For more details on CAN Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-1 Pin No	B2B Connector1 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination	Description
D24	CAN0_RX(PS_MIO38_501)	PS_MIO38_501	501	G32	I, 1.8V LVCMOS	CAN0 Receive data.
D25	CAN0_TX(PS_MIO39_501)	PS_MIO39_501	501	J32	O,1.8V LVCMOS	CAN0 Transmit data.

2.9.1.6 SD/SDIO Interface

The Zynq Ultrascale+ RFSoC SOM supports SD/SDIO interface on Board-to-Board Connector2. The SD1 controller of RFSoC's PS is used for SD/SDIO interface through MIO pins. This SD/SDIO controller is compatible with the standard SD Host Controller Specification Version 3.0. It supports different speed mode like Standard mode (19Mhz), High Speed mode (50Mhz), SDR12 (25Mhz), SDR25 (25Mhz), SDR50 (100Mhz), SDR104 (200Mhz) & DDR50 mode (50Mhz). Also in SD mode, data transfers in 1-bit and 4-bit modes.

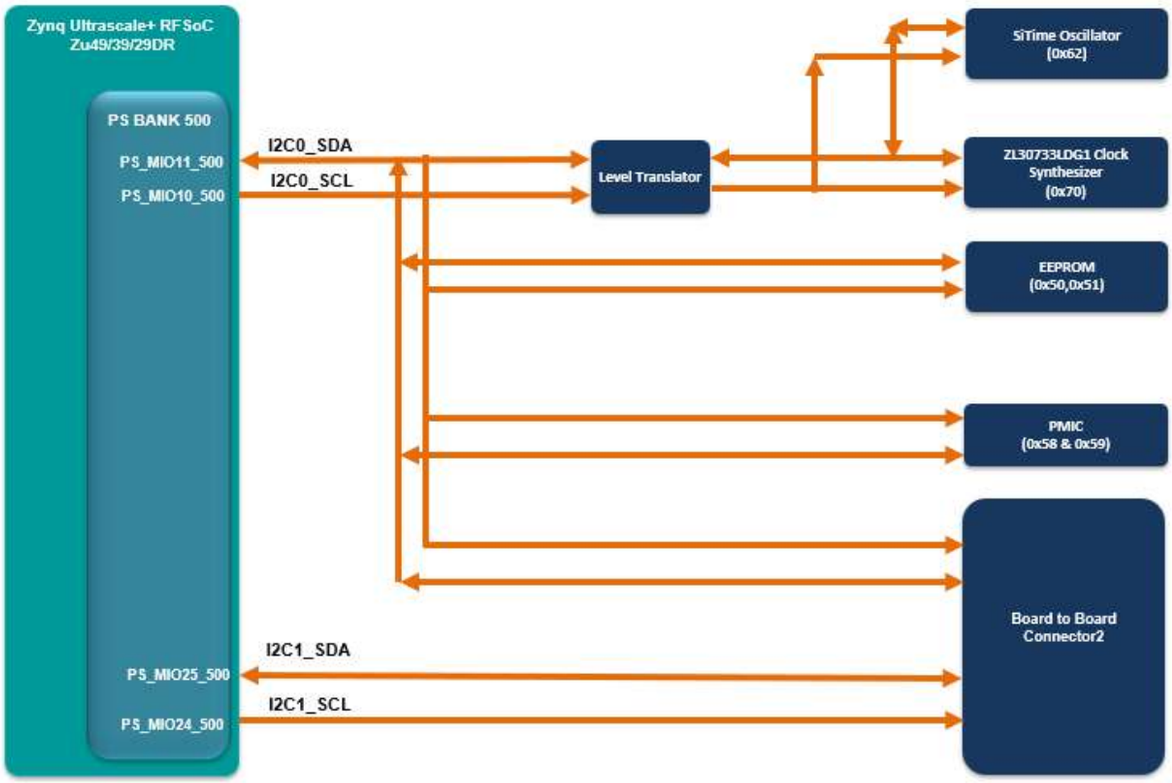
The Zynq Ultrascale+ RFSoC SOM supports Card Detect, Write Protect & Power Enable/Voltage Select pins through MIO pins.

For more details on SD/SDIO Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination	Description
A17	SD1_CLK(PS_MIO51_501)	PS_MIO51_501	501	M31	O, 1.8V LVCMOS/ 10K PU	SD1 Clock.
A18	SD1_CMD(PS_MIO50_501)	PS_MIO50_501	501	M30	IO, 1.8V LVCMOS/ 10K PU	SD1 Command.
A19	SD1_DATA0(PS_MIO46_501)	PS_MIO46_501	501	J31	IO, 1.8V LVCMOS/ 10K PU	SD1 DATA0.
A20	SD1_DATA1(PS_MIO47_501)	PS_MIO47_501	501	L32	IO, 1.8V LVCMOS/ 10K PU	SD1 DATA1.
A21	SD1_DATA2(PS_MIO48_501)	PS_MIO48_501	501	M32	IO, 1.8V LVCMOS/ 10K PU	SD1 DATA2.
A22	SD1_DATA3(PS_MIO49_501)	PS_MIO49_501	501	K31	IO, 1.8V LVCMOS/ 10K PU	SD1 DATA3.
A24	SD1_CD(PS_MIO45_501)	PS_MIO45_501	501	L30	I, 1.8V LVCMOS/ 4.7K PU	SD1 Card Detect.
A25	SD1_PWR(PS_MIO43_501)	PS_MIO43_501	501	G31	O, 1.8V LVCMOS	SD1 Power Enable/Voltage select through PS GPIO.
B24	SD1_WP(PS_MIO44_501)	PS_MIO44_501	501	K30	I, 1.8V LVCMOS/ 4.7K PU	SD1 Write Protect.

2.9.1.7 I2C Interface

The Zynq Ultrascale+ RFSoC SOM supports two I2C interface on Board-to-Board Connector2. The I2C0 & 1 module of RFSoC's PS is used for I2C interface through MIO pins and compatible with the standard NXP I2C bus protocol. It supports standard mode with data transfer rates up to 100kbps and Fast mode with data transfer rates up to 400kbps. It can function as a master or a slave in a multi-master design. The master can be programmed to use both normal (7-bit) addressing and extended (10-bit) addressing modes. Since flexible I2C standard allows multiple devices to be connected to the single bus, I2C0 interface is also connected to On-SOM interfaces in the Zynq Ultrascale+ RFSoC SOM.



For more details on I2C Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination	Description
A26	I2C0_SCL(PS_MIO10_500)	PS_MIO10_500	500	AV26	O, 1.8V OD/ 4.7K PU	I2C0 clock.
A27	I2C0_SDA(PS_MIO11_500)	PS_MIO11_500	500	AW28	IO, 1.8V OD/ 4.7K PU	I2C0 data.
A28	I2C1_SCL(PS_MIO24_500)	PS_MIO24_500	500	AL28	O, 1.8V OD/ 4.7K PU	I2C1 clock.
A29	I2C1_SDA(PS_MIO25_500)	PS_MIO25_500	500	AM28	IO, 1.8V OD/ 4.7K PU	I2C1 data.

2.9.1.8 Debug UART Interface

The Zynq Ultrascale+ RFSoC SOM supports one Debug UART interface on Board-to-Board Connector2. The UART0 controller of RFSoC's PS is used for Debug UART interface through MIO pins. This controller supports full-duplex asynchronous receiver and transmitter.

For more details on Debug UART pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination	Description
A30	UART0_TX(PS_MIO 07_500)	PS_MIO7_500	500	AY27	O, 1.8V LVCMOS	UART0 Transmit data line for Debug.
A31	UART0_RX(PS_MIO 06_500)	PS_MIO6_500	500	AY26	I, 1.8V LVCMOS	UART0 Receive data line for Debug.

2.9.1.9 Data UART Interface

The Zynq Ultrascale+ RFSoC SOM supports one DATA UART interface on Board-to-Board Connector2. The UART1 controller of RFSoC's PS is used for Data UART interface through MIO pins. This controller supports full-duplex asynchronous receiver and transmitter path with programmable baud rates. Each path includes a 64- Byte FIFIO.

For more details on Data UART pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination	Description
B27	UART1_TX(PS_MIO 08_500)	PS_MIO8_500	500	AW27	O, 1.8V LVCMOS	UART1 Transmit data line.
B28	UART1_RX(PS_MIO 09_500)	PS_MIO9_500	500	AW26	I, 1.8V LVCMOS	UART1 Receive data line.

2.9.1.10 JTAG Interface

The Zynq Ultrascale+ RFSoC SOM supports JTAG interface on Board-to-Board Connector2. The Zynq Ultrascale+ RFSoC's PS and PL share a common set of JTAG pins and each have their own TAP controller which are chained together inside the Zynq Ultrascale RFSoC. These JTAG interface signals are also connected to on-board JTAG connector.

For more details on JTAG Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination	Description
A12	PS_JTAG_TCK	PS_JTAG_TCK	503	T32	I, 1.8V LVCMOS/ 4.7K	JTAG Test Clock.
A13	PS_JTAG_TMS	PS_JTAG_TMS	503	W31	I, 1.8V LVCMOS/ 4.7K	JTAG Test Mode Select.
A14	PS_JTAG_TDO	PS_JTAG_TDO	503	V31	O, 1.8V LVCMOS	JTAG Test Data Output.
A15	PS_JTAG_TDI	PS_JTAG_TDI	503	U31	I, 1.8V LVCMOS/ 4.7K	JTAG Test Data Input.

2.9.2 PL Interfaces

The interfaces which are supported in Board to Board Connector2 from Zynq Ultrascale+ RFSoC's PL is explained in the following section.

2.9.2.1 GTY High Speed Transceivers

The Zynq Ultrascale+ RFSoC supports 16 GTY transceivers through Four transceiver Quad (Bank 128, 129, 130, & 131) with line rate from 500Mbps to 28.21Gbps based on the speed grade of the RFSoC. These transceivers can be used to interface to multiple high-speed interface protocols. Each GTY transceiver quad supports two dedicated reference clock input pairs.

Zynq Ultrascale+ RFSoC Speed Grade	GTY Transceiver line rate (min)	GTY Transceiver line rate (max)
-1L Speed Grade	0.5 Gbps	12.50 Gbps
-2L Speed Grade	0.5 Gbps	28.21 Gbps
-1 Speed Grade	0.5 Gbps	25.78 Gbps
-2 Speed Grade	0.5 Gbps	28.21 Gbps

Note: For Backplane application, the transceiver maximum line rate may come down.

The Zynq Ultrascale+ RFSoC (ZU29/39/49DR) is capable of supporting the requirements for the different speed and temperature grade as shown below.

Zynq Ultrascale+ RFSoC Speed Grade	VCCINT	VCC_PSINTLP	VCC_PSINTFP	VCC_PSINTFP_DDR	Units
-2E	0.85	0.85	0.85	0.85	V
-2I	0.85	0.85	0.85	0.85	V
-2LE	0.72	0.85	0.85	0.85	V
-1E	0.85	0.85	0.85	0.85	V
-1I	0.85	0.85	0.85	0.85	V
-2LI	0.72	0.85	0.85	0.85	V
-1LI	0.72	0.85	0.85	0.85	V

Zynq Ultrascale+ RFSoC (ZU29/39/49DR) VCC_PSINTLP, VCC_PSINTFP, VCC_PSINTFP_DDR, VCCINT_IO, Voltages are sourced from the single regulator and VCCINT sourced from single regulator. By default, Zynq Ultrascale+ RFSoC (ZU29/39/49DR) VCCINT is 0.72V and other voltages are 0.85V.

The Zynq Ultrascale+ RFSoC SOM Supports 16 GTY transceivers along with the reference clock inputs (Bank 128, 129, 130, & 131) on Board-to-Board Conenctor2.

In Zynq Ultrascale+ RFSoC SOM, On each on board reference clock1 to the GTY transceiver quad is provided. This is fed from the on-SOM clock synthesizer. On board reference clock 0 to the GTY transceiver quad is not supported. This must be fed from the carrier board based on the peripheral standards used on GTY transceivers. This gives full flexibility to end user to select the required peripheral standards on GTY transceivers.

For more details on GTY transceiver pinouts on Board-to-Board Connector2, refer the below table.

B2B-3 Pin No	B2B Connector2 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination	Description
Bank128 Transceiver Quad Pins						
A62	GTYTXP0_128	MGTYTXP0_128	128	V38	O, DIFF	GTY Bank128 channel0 High speed differential transmitter positive.
A63	GTYTXN0_128	MGTYTXN0_128	128	V39	O, DIFF	GTY Bank128 channel0 High speed differential transmitter negative.
B62	GTYRXP0_128	MGTYRXP0_128	128	AC41	I, DIFF	GTY Bank128 channel0 High speed differential receiver positive.
B63	GTYRXN0_128	MGTYRXN0_128	128	AC42	I, DIFF	GTY Bank128 channel0 High speed differential receiver negative.
A65	GTYTXP1_128	MGTYTXP1_128	128	U36	O, DIFF	GTY Bank128 channel1 High speed differential transmitter positive.
A66	GTYTXN1_128	MGTYTXN1_128	128	U37	O, DIFF	GTY Bank128 channel1 High speed differential transmitter negative.
B65	GTYRXP1_128	MGTYRXP1_128	128	AB39	I, DIFF	GTY Bank128 channel1 High speed differential receiver positive.
B66	GTYRXN1_128	MGTYRXN1_128	128	AB40	I, DIFF	GTY Bank128 channel1 High speed differential receiver negative.
A68	GTYTXP2_128	MGTYTXP2_128	128	T38	O, DIFF	GTY Bank128 channel2 High speed differential transmitter positive.
A69	GTYTXN2_128	MGTYTXN2_128	128	T39	O, DIFF	GTY Bank128 channel2 High speed differential transmitter negative.
B68	GTYRXP2_128	MGTYRXP2_128	128	AA41	I, DIFF	GTY Bank128 channel2 High speed differential receiver positive.
B69	GTYRXN2_128	MGTYRXN2_128	128	AA42	I, DIFF	GTY Bank128 channel2 High speed differential receiver negative.
A71	GTYTXP3_128	MGTYTXP3_128	128	R36	O, DIFF	GTY Bank128 channel3 High speed differential transmitter positive.
A72	GTYTXN3_128	MGTYTXN3_128	128	R37	O, DIFF	GTY Bank128 channel3 High speed differential transmitter negative.
B71	GTYRXP3_128	MGTYRXP3_128	128	Y39	I, DIFF	GTY Bank128 channel3 High speed differential receiver positive.

B2B-3 Pin No	B2B Connector2 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination	Description
B72	GTYRXN3_128	MGTYRXN3_128	128	Y40	I, DIFF	GTY Bank128 channel3 High speed differential receiver negative.
A74	GTREFCLK0P_128	MGTREFCLK0P_128	128	AA36	I, DIFF	GTY Bank128 channel0 High speed differential reference clock0 positive.
A75	GTREFCLK0N_128	MGTREFCLK0N_128	128	AA37	I, DIFF	GTY Bank128 channel0 High speed differential reference clock0 negative.
B74	B2B_GTREFCLK1P_128	MGTREFCLK1P_128	128	Y34	I, DIFF	NC *Optionally connected to High-speed differential reference clock1 positive.*
B75	B2B_GTREFCLK1N_128	MGTREFCLK1N_128	128	Y35	I, DIFF	NC *Optionally connected to High-speed differential reference clock1 negative.*
Bank129 Transceiver Quad Pins						
C62	GTYTXP0_129	MGTYTXP0_129	129	P38	O, DIFF	GTY Bank129 channel0 High speed differential transmitter positive.
C63	GTYTXN0_129	MGTYTXN0_129	129	P39	O, DIFF	GTY Bank129 channel0 High speed differential transmitter negative.
D62	GTYRXP0_129	MGTYRXP0_129	129	W41	I, DIFF	GTY Bank129 channel0 High speed differential receiver positive.
D63	GTYRXN0_129	MGTYRXN0_129	129	W42	I, DIFF	GTY Bank129 channel0 High speed differential receiver negative.
C65	GTYTXP1_129	MGTYTXP1_129	129	N36	O, DIFF	GTY Bank129 channel1 High speed differential transmitter positive.
C66	GTYTXN1_129	MGTYTXN1_129	129	N37	O, DIFF	GTY Bank129 channel1 High speed differential transmitter negative.
D65	GTYRXP1_129	MGTYRXP1_129	129	U41	I, DIFF	GTY Bank129 channel1 High speed differential receiver positive.
D66	GTYRXN1_129	MGTYRXN1_129	129	U42	I, DIFF	GTY Bank129 channel1 High speed differential receiver negative.
C68	GTYTXP2_129	MGTYTXP2_129	129	M38	O, DIFF	GTY Bank129 channel2 High speed differential transmitter positive.
C69	GTYTXN2_129	MGTYTXN2_129	129	M39	O, DIFF	GTY Bank129 channel2 High speed differential transmitter negative.
D68	GTYRXP2_129	MGTYRXP2_129	129	R41	I, DIFF	GTY Bank129 channel2 High speed differential receiver positive.
D69	GTYRXN2_129	MGTYRXN2_129	129	R42	I, DIFF	GTY Bank129 channel2 High speed differential receiver negative.
C71	GTYTXP3_129	MGTYTXP3_129	129	L36	O, DIFF	GTY Bank129 channel3 High speed differential transmitter positive.
C72	GTYTXN3_129	MGTYTXN3_129	129	L37	O, DIFF	GTY Bank129 channel3 High speed differential transmitter negative.

B2B-3 Pin No	B2B Connector2 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination	Description
D71	GTYRXP3_129	MGTYRXP3_129	129	N41	I, DIFF	GTY Bank129 channel3 High speed differential receiver positive.
D72	GTYRXN3_129	MGTYRXN3_129	129	N42	I, DIFF	GTY Bank129 channel3 High speed differential receiver negative.
C74	GTREFCLK0P_129	MGTREFCLK0P_129	129	V34	I, DIFF	GTY Bank129 channel0 High speed differential reference clock0 positive.
C75	GTREFCLK0N_129	MGTREFCLK0N_129	129	V35	I, DIFF	GTY Bank129 channel0 High speed differential reference clock0 negative.
D74	B2B_GTREFCLK1P_129	MGTREFCLK1P_129	129	T34	I, DIFF	NC *Optionally connected to High-speed differential reference clock1 positive.*
D75	B2B_GTREFCLK1N_129	MGTREFCLK1N_129	129	T35	I, DIFF	NC *Optionally connected to High-speed differential reference clock1 negative.*
Bank130 Transceiver Quad Pins						
A47	GTYTXP0_130	MGTYTXP0_130	130	K38	O, DIFF	GTY Bank130 channel0 High speed differential transmitter positive.
A48	GTYTXN0_130	MGTYTXN0_130	130	K39	O, DIFF	GTY Bank130 channel0 High speed differential transmitter negative.
B47	GTYRXP0_130	MGTYRXP0_130	130	L41	I, DIFF	GTY Bank130 channel0 High speed differential receiver positive.
B48	GTYRXN0_130	MGTYRXN0_130	130	L42	I, DIFF	GTY Bank130 channel0 High speed differential receiver negative.
A50	GTYTXP1_130	MGTYTXP1_130	130	J36	O, DIFF	GTY Bank130 channel1 High speed differential transmitter positive.
A51	GTYTXN1_130	MGTYTXN1_130	130	J37	O, DIFF	GTY Bank130 channel1 High speed differential transmitter negative.
B50	GTYRXP1_130	MGTYRXP1_130	130	J41	I, DIFF	GTY Bank130 channel1 High speed differential receiver positive.
B51	GTYRXN1_130	MGTYRXN1_130	130	J42	I, DIFF	GTY Bank130 channel1 High speed differential receiver negative.
A53	GTYTXP2_130	MGTYTXP2_130	130	H38	O, DIFF	GTY Bank130 channel2 High speed differential transmitter positive.
A54	GTYTXN2_130	MGTYTXN2_130	130	H39	O, DIFF	GTY Bank130 channel2 High speed differential transmitter negative.
B53	GTYRXP2_130	MGTYRXP2_130	130	G41	I, DIFF	GTY Bank130 channel2 High speed differential receiver positive.
B54	GTYRXN2_130	MGTYRXN2_130	130	G42	I, DIFF	GTY Bank130 channel2 High speed differential receiver negative.
A56	GTYTXP3_130	MGTYTXP3_130	130	G36	O, DIFF	GTY Bank130 channel3 High speed differential transmitter positive.

B2B-3 Pin No	B2B Connector2 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination	Description
A57	GTYTXN3_130	MGTYTXN3_130	130	G37	O, DIFF	GTY Bank130 channel3 High speed differential transmitter negative.
B56	GTYRXP3_130	MGTYRXP3_130	130	F39	I, DIFF	GTY Bank130 channel3 High speed differential receiver positive.
B57	GTYRXN3_130	MGTYRXN3_130	130	F40	I, DIFF	GTY Bank130 channel3 High speed differential receiver negative.
A59	GTREFCLK0P_ 130	MGTREFCLK0P_ 130	130	P34	I, DIFF	GTY Bank130 channel0 High speed differential reference clock0 positive.
A60	GTREFCLK0N_ 130	MGTREFCLK0N_ 130	130	P35	I, DIFF	GTY Bank130 channel0 High speed differential reference clock0 negative.
B59	GTREFCLK1P_ 130	MGTREFCLK1P_1 30	130	M34	I, DIFF	NC *Optionally connected to High-speed differential reference clock1 positive.*
B60	GTREFCLK1N_ 130	MGTREFCLK1N_ 130	130	M35	I, DIFF	NC *Optionally connected to High-speed differential reference clock1 negative.*
Bank131 Transceiver Quad Pins						
C47	GTYTXP0_131	MGTYTXP0_131	131	F34	O, DIFF	GTY Bank131 channel0 High speed differential transmitter positive.
C48	GTYTXN0_131	MGTYTXN0_131	131	F35	O, DIFF	GTY Bank131 channel0 High speed differential transmitter negative.
D47	GTYRXP0_131	MGTYRXP0_131	131	E41	I, DIFF	GTY Bank131 channel0 High speed differential receiver positive.
D48	GTYRXN0_131	MGTYRXN0_131	131	E42	I, DIFF	GTY Bank131 channel0 High speed differential receiver negative.
C50	GTYTXP1_131	MGTYTXP1_131	131	E36	O, DIFF	GTY Bank131 channel1 High speed differential transmitter positive.
C51	GTYTXN1_131	MGTYTXN1_131	131	E37	O, DIFF	GTY Bank131 channel1 High speed differential transmitter negative.
D50	GTYRXP1_131	MGTYRXP1_131	131	D39	I, DIFF	GTY Bank131 channel1 High speed differential receiver positive.
D51	GTYRXN1_131	MGTYRXN1_131	131	D40	I, DIFF	GTY Bank131 channel1 High speed differential receiver negative.
C53	GTYTXP2_131	MGTYTXP2_131	131	C36	O, DIFF	GTY Bank131 channel2 High speed differential transmitter positive.
C54	GTYTXN2_131	MGTYTXN2_131	131	C37	O, DIFF	GTY Bank131 channel2 High speed differential transmitter negative.
D53	GTYRXP2_131	MGTYRXP2_131	131	C41	I, DIFF	GTY Bank131 channel2 High speed differential receiver positive.
D54	GTYRXN2_131	MGTYRXN2_131	131	C42	I, DIFF	GTY Bank131 channel2 High speed differential receiver negative.

B2B-3 Pin No	B2B Connector2 Signal Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination	Description
C56	GTYTXP3_131	MGTYTXP3_131	131	A36	O, DIFF	GTY Bank131 channel3 High speed differential transmitter positive.
C57	GTYTXN3_131	MGTYTXN3_131	131	A37	O, DIFF	GTY Bank131 channel3 High speed differential transmitter negative.
D56	GTYRXP3_131	MGTYRXP3_131	131	B39	I, DIFF	GTY Bank131 channel3 High speed differential receiver positive.
D57	GTYRXN3_131	MGTYRXN3_131	131	B40	I, DIFF	GTY Bank131 channel3 High speed differential receiver negative.
C59	GTREFCLK0P_ 131	MGTREFCLK0P_ 131	131	K34	I, DIFF	GTY Bank131 channel0 High speed differential reference clock0 positive.
C60	GTREFCLK0N_ 131	MGTREFCLK0N_ 131	131	K35	I, DIFF	GTY Bank131 channel0 High speed differential reference clock0 negative.
D59	B2B_GTREFCLK1 P_131	MGTREFCLK1P_1 31	131	H34	I, DIFF	NC *Optionally connected to High-speed differential reference clock1 positive.*
D60	B2B_GTREFCLK1 N_131	MGTREFCLK1N_ 131	131	H35	I, DIFF	NC *Optionally connected to High-speed differential reference clock1 negative.*

2.9.3 Power, Reset & Control Signals

The Zynq Ultrascale+ RFSoC SOM works with 12V power input (VCC) from Board-to-Board Connector2 and generates all other required powers internally On-SOM itself. SOM power can be enabled/disabled from the carrier board through SOM Power enable pin (B11) in Board-to-Board Connector2. Also, in Board-to-Board Connector2, Ground pins are distributed throughout the connector for better performance.

The Zynq Ultrascale+ RFSoC SOM supports VCC_RTC coin cell power input from Board-to-Board Connector2 and connected to PMIC's VBBAT pin for real time clock backup voltage. Also, it supports warm reset input from Board-to-Board Connector2 and connected to PS_SRST_B pin of RFSoC.

The Zynq Ultrascale+ RFSoC supports synchronous clock input to and from the on-SOM clock synthesizer connected to Board-to-Board connetcor2 pins B44, B45, B41 & B42.

The Zynq Ultrascale+ RFSoC supports syncE & PTP network synchronization through 1PPS & 10MHz clocks to and from the on-SOM clock synthesizer connected to Board-to-Board Connector2 pins B26, D12, D11, & B25.

For more details on Power pins on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Pin Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination	Description
B11	SOMPWR_EN	NA	NA	NA	I, 12V	Active High SOM power enable. *Important Note: High – SOM power ON Low – SOM Power OFF*
B12	SOM_PWR_OK	NA	NA	NA	O, 1.8V	Active High SOM Power OK. *High – Carrier Board Power On Low – Carrier Board Power OFF.*
B13	GPIO_PS_RST_OUT (PS_MIO42_501)	PS_MIO42_501	501	H31	O, 1.8V LVCMOS	Common Reset Out.
B14	RESET_SW_IN	PS_SRST_B	503	R31	I, 1.8V LVCMOS/ 4.7K PU	Active low reset input.

B2B-2 Pin No	B2B Connector2 Pin Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination	Description
B15	FPGA_CONFIG_ DONE	PS_DONE	503	N31	O, 1.8V LVCMOS/ 4.7K PU	Configuration done pin.
A1, A2, A3, A4, A5, A6, A7, A8, B1, B2, B3, B4, B5, B6, B7, B8, C1, C2, C3, C4, C5, C6, C7, C8, D1, D2, D3, D4, D5, D6, D7, D8,	VCC_12V	NA	NA	NA	I, 12V	Supply Voltage.
C12	VRTC_3V0	NA	NA	NA	I, 3V Power	3V backup coin cell input for RTC.
C26	B_PCIe_RSTn	NA	NA	AL20	IO, 1.8V LVCMOS	PL PCIe Reset Root port mode as an output. End port mode as an input
C27	PS_MIO40_501	PS_MIO40_501	501	F32	IO, 1.8V LVCMOS	PS PCIe Reset Root port as an output. End port as an input
D14	PS_MIO41_501	PS_MIO41_501	501	K32	I, 1.8V LVCMOS	Dedicated Interrupt Input

B2B-2 Pin No	B2B Connector2 Pin Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination	Description
A9, A10, A16, A23, A34, A37, A40, A43, A46, A49, A52, A55, A58, A61, A64, A67, A70, A73, A76, A79, A82, A85, A88, A91, A94, A97, A100, B9, B10, B16, B23, B34, B37, B40, B43, B46, B49, B52, B55, B58, B61, B64, B67, B70, B73, B76, B79, B82, B85, B88, B91, B94, B97, B100, C9, C10, C16, C23, C28, C31, C34, C37, C40, C43, C46, C49, C52, C55, C58, C61, C64, C67, C70, C73, C76, C79, C82, C85, C88, C91, C94, C97, C100, D9, D10, D13, D16, D23, D28, D31, D34, D37, D40, D43, D46, D49, D52, D55, D58, D61,D64, D67, D70, D73, D76, D79, D82, D85, D88, D91, D94, D97, D100	GND	NA	NA	NA	Power	Ground
B44	SYS_SYNC_CLK_INp	NA	NA	NA	I, 1.8V LVDS	Synchronous input to on SOM clock synthesizer
B45	SYS_SYNC_CLK_INn	NA	NA	NA		
B25	10MHz_EX_IN	NA	NA	NA	I, 1.8V LVCMOS	10MHz clock input to on SOM clock synthesizer
D11	10MHz_EX_OUT	NA	NA	NA	O, 1.8V LVCMOS	10MHz clock output from on SOM clock synthesizer
B26	1PPS_EX_IN	NA	NA	NA	I, 1.8V LVCMOS	1Hz clock input to on SOM clock synthesizer

B2B-2 Pin No	B2B Connector2 Pin Name	RFSoC Pin Name	RFSoC Bank	RFSoC Pin No	Signal Type/ Termination	Description
D12	1PPS_EX_OUT	NA	NA	NA	O, 1.8V LVCMOS	1Hz clock output from on SOM clock synthesizer
C13	PS_MODE0	PS_MODE0	503	AA32	I, 1.8V LVCMOS	Boot Mode0 Select pin
C14	PS_MODE1	PS_MODE1	503	AB32	I, 1.8V LVCMOS	Boot Mode1 Select pin
C15	PS_MODE2	PS_MODE2	503	AB31	I, 1.8V LVCMOS	Boot Mode2 Select pin

2.10 Zynq Ultrascale+ RFSoC PS Pin Multiplexing on Board to Board Connectors

The Zynq Ultrascale+ RFSoC PS IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement. Also, most of RFSoC PS IO pins can be configured as GPIO if required. The below table provides the details of PS pin connections on Zynq Ultrascale+ RFSoC with selected pin function (highlighted) and available alternate functions. This table has been prepared by referring PS I/O configuration in Xilinx Vivado Design Suite. To know the complete available alternate functions, refer the PS I/O configuration in the latest Vivado Design Suite

Table 13: PS IOMUX on Zynq Ultrascale+ RFSoC SOM

Interface/ Function	B2B Connector Pin Number	Zynq Ultrascale+ RFSoC Pin Name	GPIO	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 9	Function 10	Function 11	Function 12	Function 13
On SOM Features from RFSoC PS																
eMMC FLASH	NA	PS_MIO13_500	GPIO13	NFC_CE	eMMC_DATA0	-	-	CAN1_RX	-	I2C1_SDA	PJTAG_TDI	SPI0_SS2	-	-	UART1_RX	-
	NA	PS_MIO14_500	GPIO14	NFC_CLE	eMMC _DATA1	-	CAN0_RX	-	I2C0_SCL	-	PJTAG_TDO	SPI0_SS1	-	UART0_RX	-	-
	NA	PS_MIO15_500	GPIO15	NFC_ALE	eMMC _DATA2	-	CAN0_TX	-	I2C0_SDA	-	PJTAG_TMS	SPI0_SS0	-	UART0_TX	-	-
	NA	PS_MIO16_500	GPIO16	NFC_DATA0	eMMC _DATA3	-	-	CAN1_TX	-	I2C1_SCL	-	SPI0_MISO	-	-	UART1_TX	-
	NA	PS_MIO17_500	GPIO17	NFC_DATA1	eMMC _DATA4	-	-	CAN1_RX	-	I2C1_SDA	-	SPI0_MIOSI	-	-	UART1_RX	-
	NA	PS_MIO18_500	GPIO18	NFC_DATA2	eMMC _DATA5	-	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_SCLK	UART0_RX	-	-
	NA	PS_MIO19_500	GPIO19	NFC_DATA3	eMMC _DATA6	-	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_SS2	UART0_TX	-	-
	NA	PS_MIO20_500	GPIO20	NFC_DATA4	eMMC _DATA7	-	-	CAN1_TX	-	I2C1_SCL	-	-	SPI1_SS1	-	UART1_TX	-
	NA	PS_MIO21_500	GPIO21	NFC_DATA5	eMMC _CMD	-	-	CAN1_RX	-	I2C1_SDA	-	-	SPI1_SS0	-	UART1_RX	-
	NA	PS_MIO22_500	GPIO22	NFC_WE_B	eMMC _CLK	-	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_MISO	UART0_RX	-	-
	NA	PS_MIO23_500	GPIO23	NFC_DATA6	eMMC_Reset	-	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_MIOSI	UART0_TX	-	-
GEM0	NA	PS_MIO26_501	GPIO26	GEM0_TX_CLK	-	-	CAN0_RX	-	I2C0_SCL	-	PJTAG_TCK	SPI0_SCLK	-	UART0_RX	-	-
	NA	PS_MIO27_501	GPIO27	GEM0_TXD0	-	-	CAN0_TX	-	I2C0_SDA	-	PJTAG_TDI	SPI0_SS2	-	UART0_TX	-	-
	NA	PS_MIO28_501	GPIO28	GEM0_TXD1	-	-	-	CAN1_TX	-	I2C1_SCL	PJTAG_TDO	SPI0_SS1	-	-	UART1_TX	-
	NA	PS_MIO29_501	GPIO29	GEM0_TXD2	-	-	-	CAN1_RX	-	I2C1_SDA	PJTAG_TMS	SPI0_SS0	-	-	UART1_RX	-
	NA	PS_MIO30_501	GPIO30	GEM0_TXD3	-	-	CAN0_RX	-	I2C0_SCL	-	-	SPI0_MISO	-	UART0_RX	-	-
	NA	PS_MIO31_501	GPIO31	GEM0_TX_CTL	-	-	CAN0_TX	-	I2C0_SDA	-	-	SPI0_MIOSI	-	UART0_TX	-	-
	NA	PS_MIO32_501	GPIO32	GEM0_RX_CLK	-	-	-	CAN1_TX	-	I2C1_SCL	-	-	SPI1_SCLK	-	UART1_TX	-
	NA	PS_MIO33_501	GPIO33	GEM0_RXD0	-	-	-	CAN1_RX	-	I2C1_SDA	-	-	SPI1_SS2	-	UART1_RX	-
	NA	PS_MIO34_501	GPIO34	GEM0_RXD1	-	-	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_SS1	UART0_RX	-	-
	NA	PS_MIO35_501	GPIO35	GEM0_RXD2	-	-	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_SS0	UART0_TX	-	-
	NA	PS_MIO36_501	GPIO36	GEM0_RXD3	-	-	-	CAN1_TX	-	I2C1_SCL	-	-	SPI1_MISO	-	UART1_TX	-
	NA	PS_MIO37_501	GPIO37	GEM0_RX_CTL	-	-	-	CAN1_RX	-	I2C1_SDA	-	-	SPI1_MIOSI	-	UART1_RX	-
	NA	PS_MIO76_502	GPIO76	GEM0_MDC	-	SD1_CLK	-	CAN1_TX	-	I2C1_SCL	-	-	-	-	-	-
	NA	PS_MIO77_502	GPIO77	GEM0_MDIO	-	SD1_CD	-	CAN1_RX	-	I2C1_SDA	-	-	-	-	-	-
	NA	PS_MIO12_500	GPIO12	-	-	-	-	CAN1_TX	-	I2C1_SCL	PJTAG_TCK	SPI0_SCLK	-	-	UART1_TX	-
	NA	PS_MIO42_501	GPIO42	GEM1_TXD3	eMMC _DATA1	-	CAN0_RX	-	I2C0_SCL	-	-	SPI0_MISO	-	UART0_RX	-	-
USB2.0	NA	PS_MIO52_502	GPIO52	GEM2_TX_CLK	-	-	-	CAN1_TX	-	I2C1_SCL	PJTAG_TCK	SPI0_SCLK	-	-	UART1_TX	USB0_CLK
	NA	PS_MIO53_502	GPIO53	GEM2_TXD0	-	-	-	CAN1_RX	-	I2C1_SDA	PJTAG_TDI	SPI0_SS2	-	-	UART1_RX	USB0_DIR
	NA	PS_MIO54_502	GPIO54	GEM2_TXD1	-	-	CAN0_RX	-	I2C0_SCL	-	PJTAG_TDO	SPI0_SS1	-	UART0_RX	-	USB0_DATA2
	NA	PS_MIO55_502	GPIO55	GEM2_TXD2	-	-	CAN0_TX	-	I2C0_SDA	-	PJTAG_TMS	SPI0_SS0	-	UART0_TX	-	USB0_NXT
	NA	PS_MIO56_502	GPIO56	GEM2_TXD3	-	-	-	CAN1_TX	-	I2C1_SCL	-	SPI0_MISO	-		UART1_TX	USB0_DATA0
	NA	PS_MIO57_502	GPIO57	GEM2_TX_CTL	-	-	-	CAN1_RX	-	I2C1_SDA	-	SPI0_MIOSI	-		UART1_RX	USB0_DATA1
	NA	PS_MIO58_502	GPIO58	GEM2_RX_CLK	-	-	CAN0_RX	-	I2C0_SCL	-	PJTAG_TCK	-	SPI1_SCLK	UART0_RX	-	USB0_STP
	NA	PS_MIO59_502	GPIO59	GEM2_RXD0	-	-	CAN0_TX	-	I2C0_SDA	-	PJTAG_TDI	-	SPI1_SS2	UART0_TX	-	USB0_DATA3
	NA	PS_MIO60_502	GPIO60	GEM2_RXD1	-	-	-	CAN1_TX	-	I2C1_SCL	PJTAG_TDO	-	SPI1_SS1	-	UART1_TX	USB0_DATA4
	NA	PS_MIO61_502	GPIO61	GEM2_RXD2	-	-	-	CAN1_RX	-	I2C1_SDA	PJTAG_TMS	-	SPI1_SS0	-	UART1_RX	USB0_DATA5
	NA	PS_MIO62_502	GPIO62	GEM2_RXD3	-	-	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_MISO	UART0_RX	-	USB0_DATA6

Interface/ Function	B2B Connector Pin Number	Zynq Ultrascale+ RFSoC Pin Name	GPIO	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 9	Function 10	Function 11	Function 12	Function 13
	NA	PS_MIO63_502	GPIO63	GEM2_RX_CTL	-	-	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_MIOSI	UART0_TX	-	USB0_DATA7
Board to Board Connector1 Interfaces from RFSoC PS																
GEM3/USB1	C17	PS_MIO64_502	GPIO64	GEM3_TX_CLK	eMMC _CLK	-	-	CAN1_TX	-	I2C1_SCL	-	SPI0_SCLK	-	-	UART1_TX	USB1_CLK
	C18	PS_MIO65_502	GPIO65	GEM3_TXD0	-	-	-	CAN1_RX	-	I2C1_SDA	-	SPI0_SS2	-	-	UART1_RX	USB1_DIR
	C19	PS_MIO66_502	GPIO66	GEM3_TXD1	eMMC _CMD	-	CAN0_RX	-	I2C0_SCL	-	-	SPI0_SS1	-	UART0_RX	-	USB1_DATA2
	C20	PS_MIO67_502	GPIO67	GEM3_TXD2	eMMC_DATA0	-	CAN0_TX	-	I2C0_SDA	-	-	SPI0_SS0	-	UART0_TX	-	USB1_NXT
	C21	PS_MIO68_502	GPIO68	GEM3_TXD3	eMMC _DATA1	-	-	CAN1_TX	-	I2C1_SCL	-	SPI0_MISO	-	-	UART1_TX	USB1_DATA0
	C22	PS_MIO69_502	GPIO69	GEM3_TX_CTL	eMMC_DATA2	SD1_WP	-	CAN1_RX	-	I2C1_SDA	-	SPI0_MIOSI	-	-	UART1_RX	USB1_DATA1
	D17	PS_MIO70_502	GPIO70	GEM3_RX_CLK	eMMC _DATA3	SD1_PWR	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_SCLK	UART0_RX	-	USB1_STP
	D18	PS_MIO71_502	GPIO71	GEM3_RXD0	eMMC _DATA4	SD1_DATA0	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_SS2	UART0_TX	-	USB1_DATA3
	D19	PS_MIO72_502	GPIO72	GEM3_RXD1	eMMC _DATA5	SD1_DATA1	-	CAN1_TX	-	I2C1_SCL	-	-	SPI1_SS1	-	UART1_TX	USB1_DATA4
	D20	PS_MIO73_502	GPIO73	GEM3_RXD2	eMMC _DATA6	SD1_DATA2	-	CAN1_RX	-	I2C1_SDA	-	-	SPI1_SS0	-	UART1_RX	USB1_DATA5
	D21	PS_MIO74_502	GPIO74	GEM3_RXD3	eMMC _DATA7	SD1_DATA3	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_MISO	UART0_RX	-	USB1_DATA6
	D22	PS_MIO75_502	GPIO75	GEM3_RX_CTL	eMMC_Reset	SD1_CMD	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_MIOSI	UART0_TX	-	USB1_DATA7
CAN0	D24	PS_MIO38_501	GPIO38	GEM1_TX_CLK	eMMC _CLK	-	CAN0_RX	-	I2C0_SCL	-	PJTAG_TCK	SPI0_SCLK	-	UART0_RX	-	-
	D25	PS_MIO39_501	GPIO39	GEM1_TXD0	-	-	CAN0_TX	-	I2C0_SDA	-	PJTAG_TDI	SPI0_SS2	-	UART0_TX	-	-
CAN1	D26	PS_MIO40_501	GPIO40	GEM1_TXD1	eMMC _CMD	-	-	CAN1_TX	-	I2C1_SCL	PJTAG_TDO	SPI0_SS1	-	-	UART1_TX	-
	D27	PS_MIO41_501	GPIO41	GEM1_TXD2	eMMC_DATA0	-	-	CAN1_RX	-	I2C1_SDA	PJTAG_TMS	SPI0_SS0	-	-	UART1_RX	-
Board to Board Connector2 Interfaces from RFSoC PS																
SD1(4-Bit)	B24	PS_MIO44_501	GPIO44	GEM1_RX_CLK	eMMC _DATA3	SD1_WP	-	CAN1_TX	-	I2C1_SCL	-	-	SPI1_SCLK	-	UART1_TX	-
	A24	PS_MIO45_501	GPIO45	GEM1_RXD0	eMMC _DATA4	SD1_CD	-	CAN1_RX	-	I2C1_SDA	-	-	SPI1_SS2	-	UART1_RX	-
	A25	PS_MIO43_501	GPIO43	GEM1_TX_CTL	eMMC_DATA2	SD1_PWR	CAN0_TX	-	I2C0_SDA	-	-	SPI0_MIOSI	-	UART0_TX	-	-
	A19	PS_MIO46_501	GPIO46	GEM1_RXD1	eMMC _DATA5	SD1_DATA0	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_SS1	UART0_RX	-	-
	A20	PS_MIO47_501	GPIO47	GEM1_RXD2	eMMC _DATA6	SD1_DATA1	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_SS0	UART0_TX	-	-
	A21	PS_MIO48_501	GPIO48	GEM1_RXD3	eMMC _DATA7	SD1_DATA2	-	CAN1_TX	-	I2C1_SCL	-	-	SPI1_MISO	-	UART1_TX	-
	A22	PS_MIO49_501	GPIO49	GEM1_RX_CTL	eMMC_Reset	SD1_DATA3	-	CAN1_RX	-	I2C1_SDA	-	-	SPI1_MIOSI	-	UART1_RX	-
	A18	PS_MIO50_501	GPIO50	GEM1_MDC	-	SD1_CMD	CAN0_RX	-	I2C0_SCL	-	-	-	-	UART0_RX	-	-
	A17	PS_MIO51_501	GPIO51	GEM1_MDIO	-	SD1_CLK	CAN0_TX	-	I2C0_SDA	-	-	-	-	UART0_TX	-	-
SPI/QSPI	B17	PS_MIO0_500	GPIO0	QSPI_SCLK	-	-	-	CAN1_TX	-	I2C1_SCL	PJTAG_TCK	SPI0_SCLK	-	-	UART1_TX	-
	B20	PS_MIO1_500	GPIO1	QSPI_SS2	-	-	-	-	-	-	-		-	-	-	
	B21	PS_MIO2_500	GPIO2	QSPI_SS1	-	-	-	-	-	-	-		-	-	-	-
	B22	PS_MIO3_500	GPIO3	QSPI_SS0	-	-	CAN0_TX	-	I2C0_SDA	-	PJTAG_TMS	SPI0_SS0	-	UAR`T0_TX	-	-
	B19	PS_MIO4_500	GPIO4	QSPI_MISO	-	-	-	CAN1_TX	-	I2C1_SCL	-	SPI0_MISO	-	-	UART1_TX	-
	B18	PS_MIO5_500	GPIO5	QSPI_MOSI	-	-	-	CAN1_RX	-	I2C1_SDA	-	SPI0_MOSI	-	-	UART1_RX	-
Debug UART (UART0)	A30	PS_MIO07_500	-	-	-	-	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_SS2	-	UART0_TX	-
	A31	PS_MIO06_500	-	-	-	-	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_SCLK	-	UART0_RX	-
UART1	B27	PS_MIO08_500	GPIO8	-	-	-	-	CAN1_TX	-	I2C1_SCL	-	-	SPI1_SS1	-	UART1_TX	-
	B28	PS_MIO09_500	GPIO9	-	-	-	-	CAN1_RX	-	I2C1_SDA	-	-	SPI1_SS0	-	UART1_RX	-
I2C0	A27	PS_MIO11_500	GPIO11	-	-	-	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_MIOSI	UART0_TX	-	-
	A26	PS_MIO10_500	GPIO10	NFC_RB_N	-	-	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_MISO	UART0_RX	-	-
GPIOs/I2C1	A29	PS_MIO25_500	GPIO25	NFC_RE_N	-	-	-	CAN1_RX	-	I2C1_SDA	-	-	-	-	UART1_RX	-
	A28	PS_MIO24_500	GPIO24	NFC_DATA7	-	-	-	CAN1_TX	-	I2C1_SCL	-	-	-	-	UART1_TX	-
JTAG	A15	PS_JTAG_TDI	-	PS_JTAG_TDI	-	-	-	-	-	-	-	-	-	-	-	-
	A13	PS_JTAG_TMS	-	PS_JTAG_TMS	-	-	-	-	-	-	-	-	-	-	-	-
	A12	PS_JTAG_TCK	-	PS_JTAG_TCK	-	-	-	-	-	-	-	-	-	-	-	-
	A14	PS_JTAG_TDO	-	PS_JTAG_TDO	-	-	-	-	-	-	-	-	-	-	-	-

3. TECHNICAL SPECIFICATION

This section provides detailed information about the Zynq Ultrascale+ RFSoC (ZU29/39/49DR) SOM technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

3.1.1 Power Input Requirement

The below table provides the Power Input Requirement of Zynq Ultrascale+ RFSoC (ZU29/39/49DR) SOM.

Table 14: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_12V[1]	11.95V	5V	12.05V	±50mV
2	VRTC_3V0[2]	0V	3V	3.15V	±20mV

[1] Zynq Ultrascale+ RFSoC (ZU29/39/49DR) SOM is designed to work with VCC_12V input power rail from Board-to-Board Connector2.

[2] Zynq Ultrascale+ RFSoC (ZU29/39/49DR) SOM uses this voltage as backup power source to PMIC RTC when VCC_12V is off. This is an optional power and required only if RTC functionality is used.

3.1.2 Power Input Sequencing

The Zynq Ultrascale+ RFSoC (ZU29/39/49DR) SOM Power Input sequence requirement is explained below.

Power up Sequence:

- VRTC_3V0 must come up at the same time or before VCC_12V comes up.
- SOMPWR_EN signal from Board-to-Board Connector1 must be high at the same time or after VCC_12V comes up.

Power down Sequence:

- SOMPWR_EN signal from Board-to-Board Connector1 must be low at the same time or before VCC_12V goes down.
- VCC_12V must go down at the same time or before VRTC_3V0 goes down.

Table 15: Power Sequence Timing

Item	Description	Value
T1	VRTC_3V0[1] rise time to VCC_12V rise time	≥ 0 ms
T2	VCC_12V rise time to SOMPWR_EN rise time	≥ 0 ms
T3	SOMPWR_EN fall time to VCC_12V fall time	≥ 0 ms
T4	VCC_12V fall time to VRTC_3V0 fall time	≥ 0 ms

[1] VRTC_3V0 is the RTC Battery backup supply. This is an optional power.

3.1.3 Power Consumption

Table 16: Power Consumption

Task/Status	Power Rail	Current Drawn/Power Consumption
Only Booting Test (from Power-on to till Kernel)	VCC_12V	2A/24.07W
Dhrystone		2.025A/24.23W
FMC+ Loopback Transceiver test through IBERT		2.185A/26.22W
FMC+ Loopback Test		2.263A/27.15W
Ping Ethernet (Gem0) DP eMMC Read/Write or SD Read/Write or QSPI Read/Write or USB Type-C Read/Write FMC+ Loopback Test		2.37A/28.44W
16 Channels-DAC & ADC Loopback		3.343A/40.116W

For more accurate power estimation, iWave recommends to use Xilinx Power Estimator (XPE) tool and calculate the MPSoC power. Also add extra 3A for other On-SOM peripherals power.

For reference, we have calculated the Zynq Ultrascale+ RFSoC (ZU49/39/29DR) Theoretical Power Estimation by using Xilinx Power Estimator (XPE) tool with various FPGA utilisation and ambient temperature as shown below.

FPGA Utilisation (%)	SOM Theoretical Power Estimation @ 12V	
	25 C Ambient	60 C Ambient
50	6.56A/78.72W	6.87A/82.44W
80	7.77A/93.24W	8.20A/98.4W
100	8.57A/102.84	9.11A/109.32

Note: This above calculation is based on 49DR device with Typical/Maximum Process @ -1L Industrial Speed Grade

FPGA Utilisation (%)	SOM Theoretical Power Estimation @ 12V	
	25 C Ambient	60 C Ambient
50	7.22A/86.64W	7.68A/92.16W
80	8.60A/103.2W	9.27A/111.24W
100	9.56A/114.72W	10.43A/125.16W

Note: This Above calculation is based on 49DR device with Typical/Maximum Process @ -2 Industrial Speed Grade

3.2 Environmental Characteristics

3.2.1 Temperature Specification

The below table provides the Environment specification of Zynq Ultrascale+ RFSoC (ZU29/39/49DR) SOM.

Table 17: Temperature Specification

Parameters	Min	Max
Operating temperature range - Industrial[1]	-40°C	85°C
Operating temperature range - Extended[1]	0°C	85°C

[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

3.2.2 RoHS2 Compliance

iWave's Zynq Ultrascale+ RFSoC (ZU29/39/49DR) SOM is designed by using RoHS2 compliant components and manufactured on lead free production process.

3.2.3 Electrostatic Discharge

iWave's Zynq Ultrascale+ RFSoC (ZU29/39/49DR) SOM is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SOM except at an electrostatic free workstation.

3.2.4 Heat Sink

For any highly integrated System On Modules, thermal design is very important factor. As IC's size is decreasing and performance of module is increasing by rising processor frequencies, it generates high amount of heat which should be dissipated for the system to work as expected without fault.

To dissipate the heat, appropriate thermal management technique Heat sink must be used. Always remember that, if you use more effective thermal solution, you will get more performance out of the CPU.

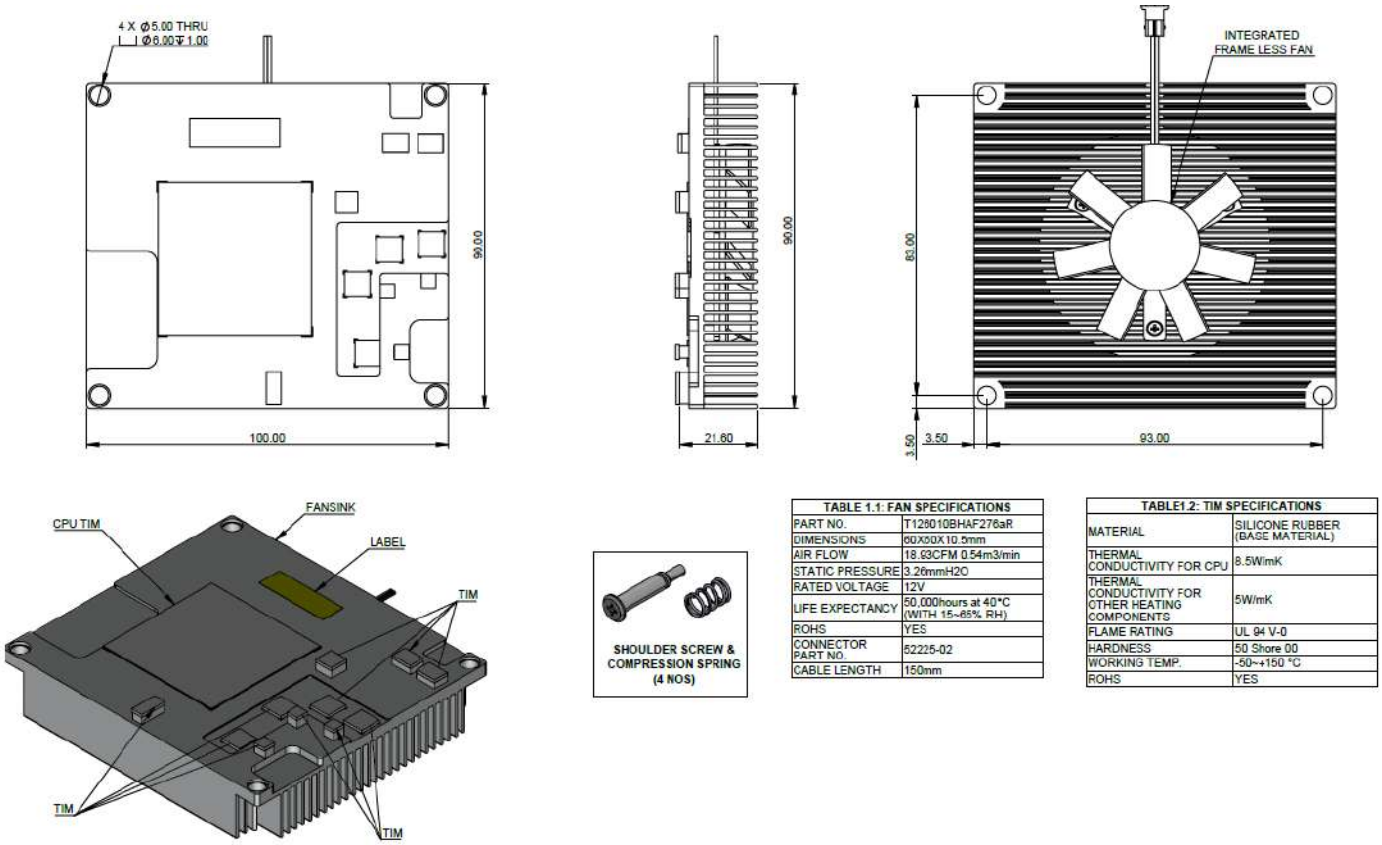


TABLE 1.1: FAN SPECIFICATIONS	
PART NO.	T128010BHAF276aR
DIMENSIONS	60X60X10.5mm
AIR FLOW	18.63CFM 0.54m3/min
STATIC PRESSURE	3.26mmH2O
RATED VOLTAGE	12V
LIFE EXPECTANCY	50,000hours at 40°C (WITH 15~65% RH)
ROHS	YES
CONNECTOR PART NO.	52225-02
CABLE LENGTH	150mm

TABLE1.2: TIM SPECIFICATIONS	
MATERIAL	SILICONE RUBBER (BASE MATERIAL)
THERMAL CONDUCTIVITY FOR CPU	8.5W/mK
THERMAL CONDUCTIVITY FOR OTHER HEATING COMPONENTS	5W/mK
FLAME RATING	UL 94 V-0
HARDNESS	50 Shore 00
WORKING TEMP.	-50~+150 °C
ROHS	YES

Figure 10: Heat Sink

3.3 MechanicalCharacteristics

3.3.1 Zynq Ultrascale+ RFSoC SOM Mechanical Dimensions

Zynq Ultrascale+ RFSoC (ZU29/39/49DR) SOM PCB size is 100mm x 90mm x 2.20mm Thickness. SOM mechanical dimension is shown below.

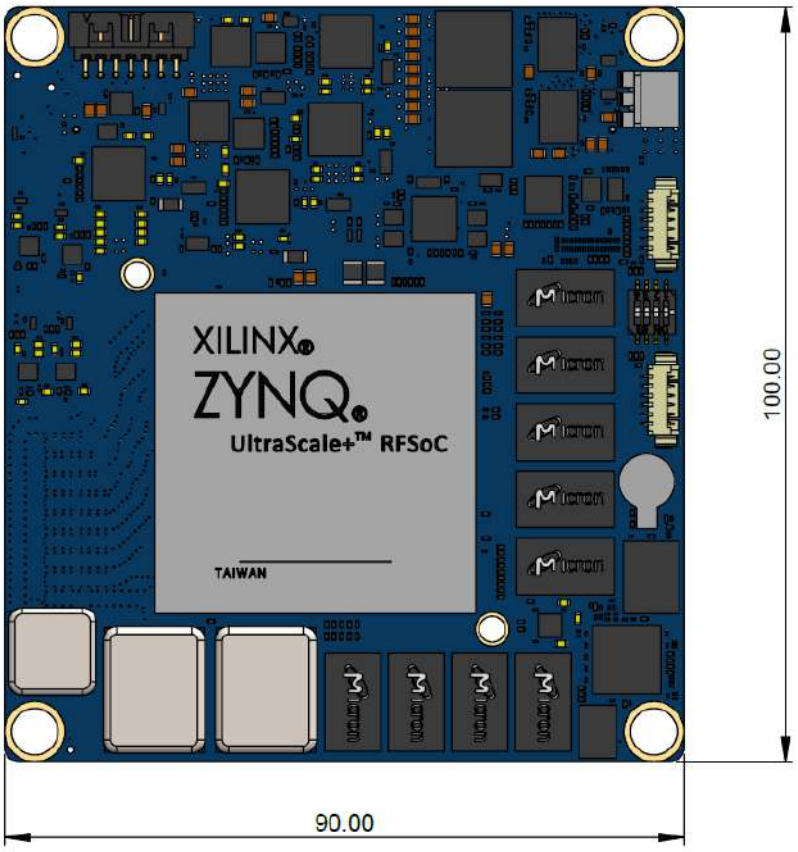


Figure 11: Mechanical dimension of Zynq Ultrascale+ RFSoC SOM - Top View

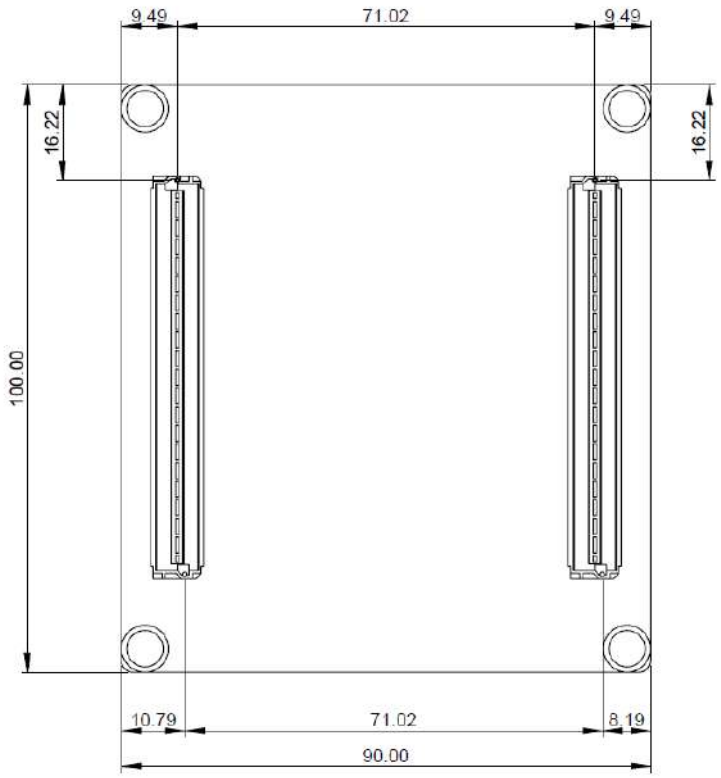


Figure 12: Mechanical dimension of Zynq Ultrascale+ RFSoC SOM - Bottom View

Zynq Ultrascale+ RFSoC (ZU29/39/49DR) PCB thickness is 2.20mm±0.1mm, top side maximum height component is JTAG Header J1 (6.30mm) and bottom side maximum height component is Board to Board connector 1 & 2 (3.6mm) Please refer the below figure which gives height details of the Zynq Ultrascale+ RFSoC SOM.

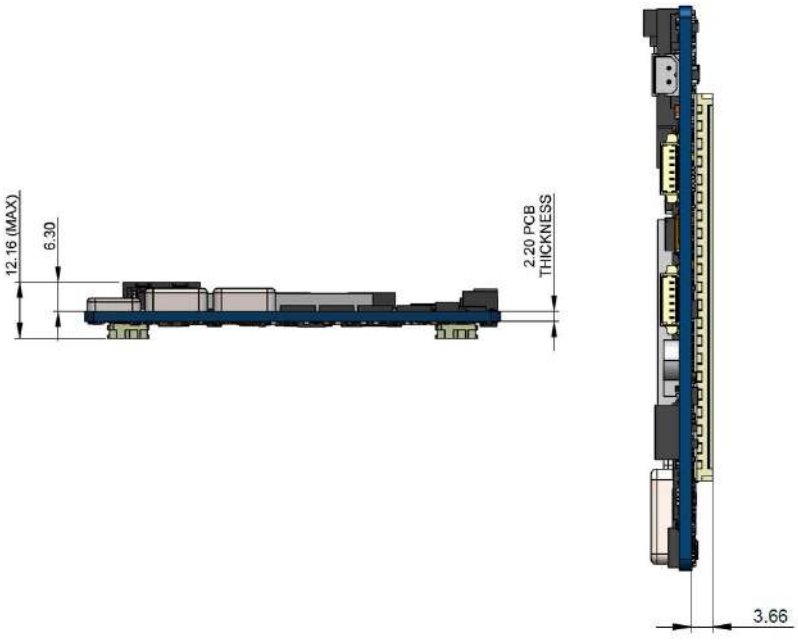


Figure 13: Mechanical dimension of Zynq Ultrascale+ RFSoC SOM - Side View

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different Zynq Ultrascale+ RFSoC (ZU29/39/49DR) SOM variations. Please contact iWave for orderable part number of higher RAM memory size or Flash memory size SOM configurations. Also, if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

Table 18: Orderable Product Part Numbers

Product Part Number	Description	Temperature
ZU49DR RFSoC based SOM		
iW-G42M-49DR-4E008G-E0032G-LIA	ZU49DR -L1 (Low Power) RFSoC with 8GB PS DDR4, 8GB FPGA DDR4, 32GB eMMC SOM with Linux	Industrial
ZU39DR RFSoC based SOM		
iW-G42M-ZU39-4E008G-E0032G-LIB	ZU39DR -1 Speed RFSoC with 8GB PS DDR4, 8GB FPGA DDR4, 32GB eMMC SOM with Linux	Industrial
ZU29DR RFSoC based SOM		
iW-G42M-29DR-4E008G-E0032G-LIB	ZU29DR -1 Speed RFSoC with 8GB PS DDR4, 8GB FPGA DDR4, 32GB eMMC SOM with Linux	Industrial

5. APPENDIX

5.1 Zynq Ultrascale+ RPSoC SOM Development Platform

iWave Systems supports iW-RainboW-G42P – Zynq Ultrascale+ RFSoC (ZU29/39/49DR) SOM PCIe Development Platform which is targeted for quick validation of Zynq Ultrascale+ RFSoC (ZU29/39/49DR) based SOM. iWave's Zynq Ultrascale+ RFSoC PCIe Development Board incorporates Zynq Ultrascale+ RFSoC (ZU29/39/49DR) SOM and PCIe Carrier board with complete BSP support.

Figure 14: Zynq Ultrascale+ RFSoC (ZU29/39/49DR) SOM Development Platform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